GLF81311

Nano-Current Power I_QSmart™ Load Switch

Product Specification

DESCRIPTION

The GLF81311 is an ultra-efficiency, 3 A rated, Load Switch with integrated slew rate control. The best-in-class efficiency makes it an ideal chose for use in IoT, mobile, and wearable electronics.

The GLF81311 features ultra-efficient I_QSmart™ technology that supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF81311 integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF slew rate control specifically limits inrush currents during turn-on to minimize voltage droop.

GLF81311 Load Switch devices support an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduce operating cost.

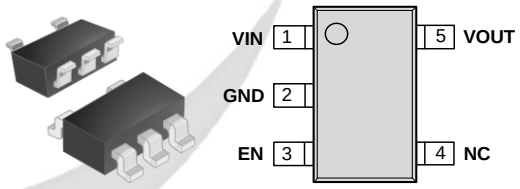
FEATURES

- Supply Voltage Range: 2.0 V to 6.5 V
  7.0 V_{Abs} max
- I_{OUT} Max: 3 A
- Low R_{ON}: 41 mΩ Typ @ 6.5 V_{IN}
- Ultra-Low I_Q: 10 nA Typ @ 6.5 V_{IN}
- Ultra-Low I_{SD}: 20 nA Typ @ 6.5 VIN
- Controlled Rise Time: 2.3 ms at 6.0 V_{IN}
- Smart Enable Pin
  I_{EN}: 3 nA Typ at $V_{EN} > V_{IH}$
  R_{EN}: 500 kΩ Typ at $V_{EN} < V_{IL}$
- Integrated Output Discharge Switch
- Wide Operating Temperature Range:
  -40 °C ~ 85 °C
- HBM: 6 kV, CDM: 2 kV

APPLICATIONS

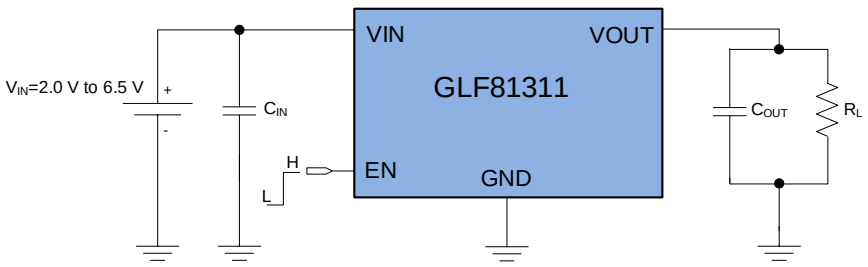
- Smart IoT Devices
- Low Power Subsystems

PACKAGE



SOT23-5L

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ.) at 6.5 V	EN Activity	Tape and Reel Packaging
GLF81311	DE	41 mΩ	High	3000 Pieces on 7 inch reel

FUNCTIONAL BLOCK DIAGRAM

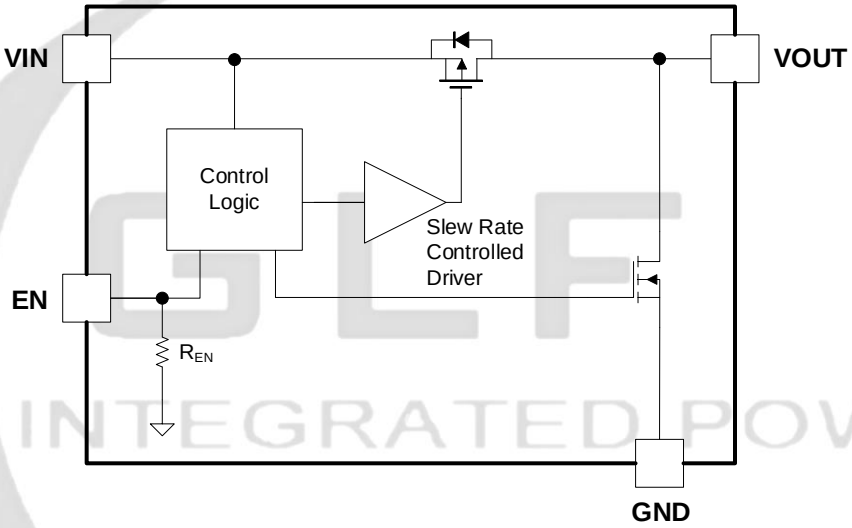


Figure 1. Functional Block Diagram

PIN CONFIGURATION

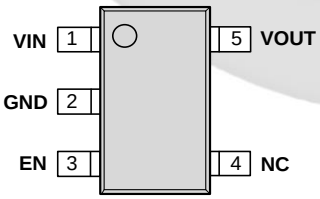


Figure 2. SOT23-5L

PIN DEFINITION

Pin #	Name	Description
1	V_{IN}	Switch Input. Supply Voltage for IC
2	GND	Ground
3	EN	Enable to control the switch.
4	NC	No connection
5	V_{OUT}	V_{OUT} pin is connected to the downstream system.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}, V_{OUT}, EN	Each Pin Voltage Range to GND	-0.3	7.0	V
I_{OUT}	Maximum Continuous Switch Current		3	A
P_D	Power Dissipation at T_A = 25°C		1.0	W
T_{STG}	Storage Junction Temperature	-65	150	°C
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	-40	85	°C
θ_{JC}	Thermal Resistance, Junction to Case		90	°C/W
θ_{JA}	Thermal Resistance, Junction to Ambient (Measured using 2S2P JEDEC std. PCB.)		180	°C/W

ESD Ratings

Symbol	Parameter		Value	Unit
HBM	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6	kV
CDM		Charged Device Model, JESD22-C101	2	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.0	6.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 2.0 V to 6.5 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
I_Q	Supply Current	EN = Enable, I_{OUT}=0 mA, V_{IN}=V_{EN} =2.0 V			4		nA
		EN = Enable, I_{OUT}=0 mA, V_{IN}=V_{EN} =3.7 V (2)			7		
		EN = Enable, I_{OUT}=0 mA, V_{IN}=V_{EN} =4.2 V (2)			8		
		EN = Enable, I_{OUT}=0 mA, V_{IN}=V_{EN} =5.0 V (2)			9		
		EN = Enable, I_{OUT}=0 mA, V_{IN}=V_{EN} =6.0 V (2)			10		
		EN = Enable, I_{OUT}=0 mA, V_{IN}=V_{EN} =6.5 V			10	30	
		EN=Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=6.5 V, Ta=85 °C (2)			17		
I_{SD}	Shutdown Current	EN = Disable, I_{OUT}=0 mA, V_{IN}=2.0 V			2		nA
		EN = Disable, I_{OUT}=0 mA, V_{IN}=3.7 V (2)			3		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=4.2 V (2)			4		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.0 V (2)			10		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=6.0 V (2)			15		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=6.5 V			20	50	
		EN = Disable, I_{OUT}=0 mA, V_{IN}=6.5 V, Ta=85 °C (2)			410		
R_{ON}	On-Resistance	V_{IN}=6.5 V I_{OUT}= 500 mA	Ta=25 °C		41	47	mΩ
			Ta=85 °C (2)		49		
		V_{IN}=6.0 V, I_{OUT}= 500 mA (2)	Ta=25 °C		42	48	
			Ta=85 °C (2)		50		
		V_{IN}=5.0 V, I_{OUT}= 500 mA (2)	Ta=25 °C		43	49	
		V_{IN}=4.2 V, I_{OUT}= 500 mA (2)	Ta=25 °C		45	51	
		V_{IN}=3.7 V, I_{OUT}= 300 mA (2)	Ta=25 °C		46	52	
		V_{IN}=3.3 V, I_{OUT}= 300 mA	Ta=25 °C		47	53	
		V_{IN}=2.5 V, I_{OUT}= 300 mA (2)	Ta=25 °C		53	60	
		V_{IN}=2.0 V, I_{OUT}= 300 mA	Ta=25 °C		60	68	
R_{DSC}	Output Discharge Resistance	E_N=Low , I_{FORCE}= 10 mA			560		Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}=2.0 V to 6.5 V		1.5			V
V_{IL}	EN Input Logic Low Voltage					0.4	V
I_{EN}	EN Current	EN Voltage > V_{IH}			3		nA
R_{EN}	EN Pulldown Resistance	V_{EN} < V_{IL}, Disabled			500		kΩ
Switching Characteristics (1), (2)							
t_{dON}	Turn-On Delay	V_{IN}=6.0 V, R_{OUT}= 150 Ω, C_{OUT}=1.0 µF			1.3		ms
t_R	V_{OUT} Rise Time				2.3		
t_{dOFF}	Turn-Off Delay				12		µs
t_F	V_{OUT} Fall Time				265		

Notes: 1. t_{ON} = t_{dON} + t_R , t_{OFF} = t_{dOFF} + t_F
2. By design; characterized, not production tested

TIMING DIAGRAM

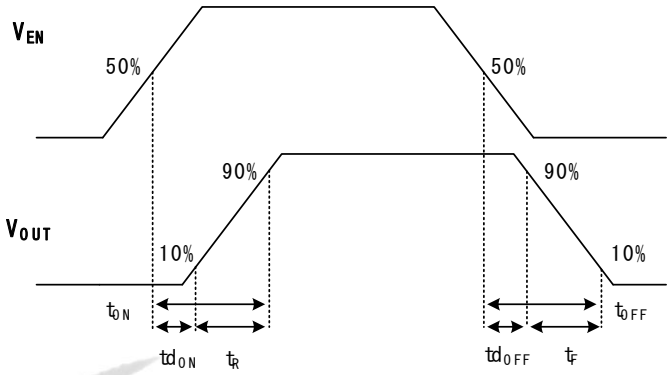


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

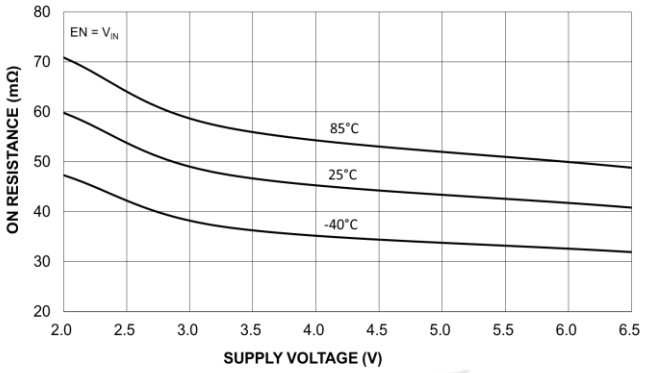


Figure 4. On-Resistance vs. Supply Voltage

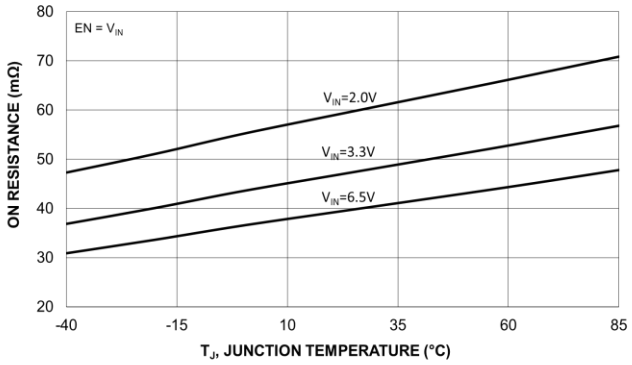


Figure 5. On-Resistance vs. Temperature

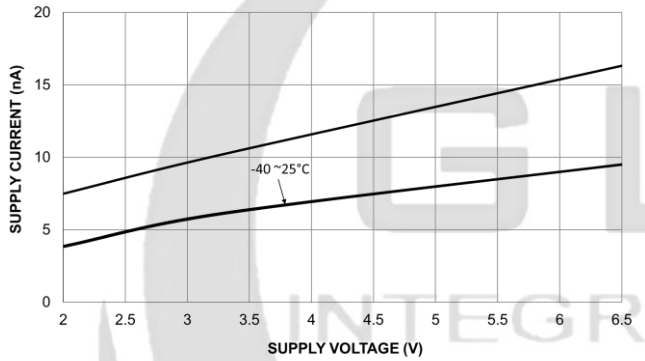


Figure 6. Quiescent Current vs. Supply Voltage

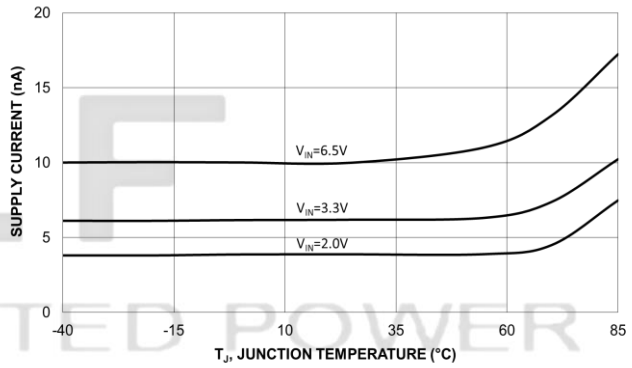


Figure 7. Quiescent Current vs. Temperature

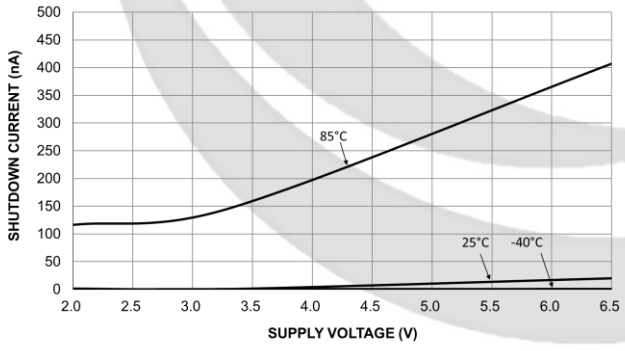


Figure 8. Shutdown Current vs. Supply Voltage

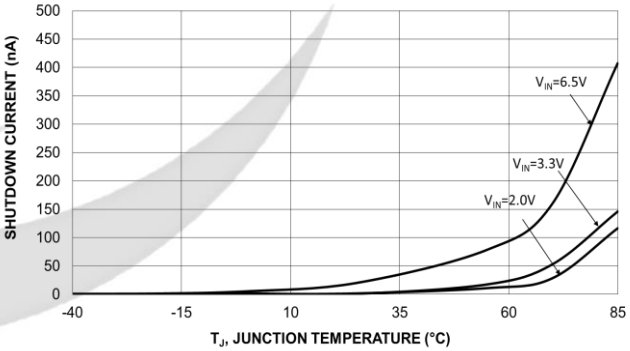


Figure 9. Shutdown Current vs. Temperature

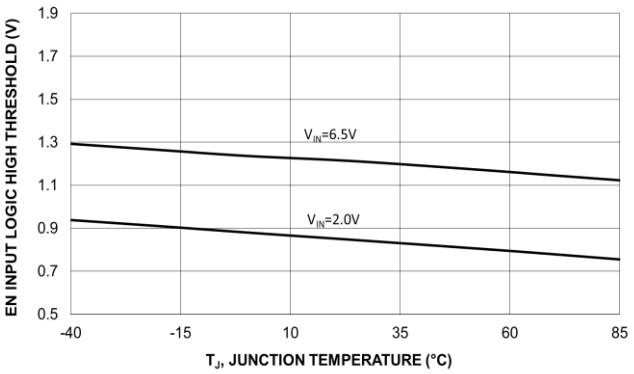


Figure 10. EN Input Logic High Threshold

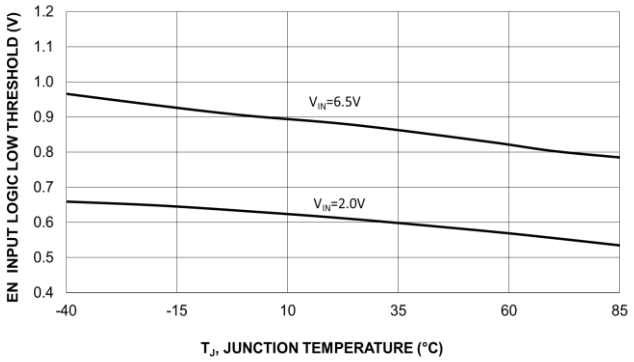


Figure 11. EN Input Logic Low Threshold

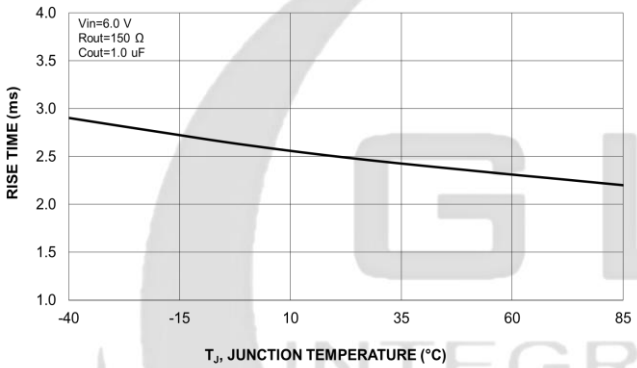


Figure 12. VOUT Rise Time vs. Temperature

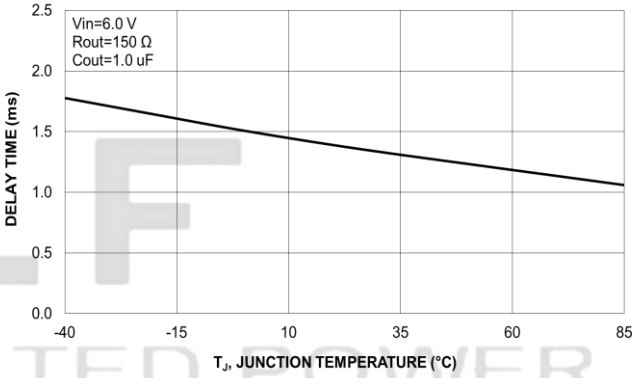


Figure 13. Turn-On Delay Time vs. Temperature

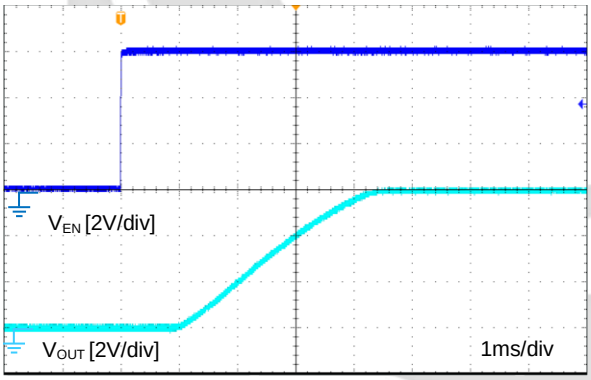


Figure 14. Turn-On Response
V_{IN}=6.0 V, C_{IN}=1.0 µF, C_{OUT}=1.0 µF, R_L=150 Ω

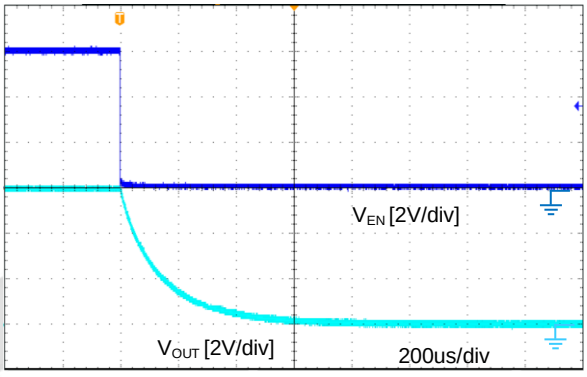


Figure 15. Turn -Off Response
V_{IN}=6.0 V, C_{IN}=1.0 µF, C_{OUT}=1.0 µF, R_L=150 Ω

APPLICATION INFORMATION

The GLF81311 is an ultra-efficient integrated 3 A I_QSmart^{TM} load switch with the slew rate control of the output voltage to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 2.0 V to 6.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power supply.

Input Capacitor

The GLF81311 requires an input capacitor to function. To reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 1uF capacitor is recommended to be placed close to V_{IN} pin. A higher input capacitor value can be used to attenuate the input voltage drop.

Output Capacitor

A 0.1uF capacitor or higher values can be able to prevent undershoot caused by parasitic inductance on board traces at switching off and improve reliability of a controlled voltage rail. The C_{OUT} should be placed close to VOUT and GND pins.

Input Voltage Spike Reduction

In steady state condition, the voltages at input pins almost equal to the input power sources. However, at the transient time when the power source is plugged in, a spike voltage will be induced at input pin. The level of the voltage spike is determined by the parasitic inductance between power source and input pin as well as the change rate of input current. The longer length between power source and input pin, the faster change rate of input current, the larger voltage spike. If the spike voltage level exceeds the absolute maximum rated input voltage, it may damage the chip permanently. Below is the waveform when a 6.0 V power source is “hot” plugged in, and the voltage spike can be up to 9.1 V. A “hot” plug-in is not recommended all the time.

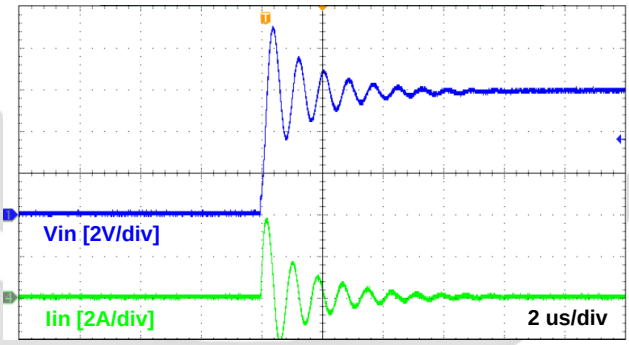


Figure 16. the voltage spike when the power source is “hot” plugged in (IC is disabled)

The voltage spikes are tested with different wire length between the power source and input pin. The results are shown in the table below.

V_{IN} (V)	Wire Length (Cm)	V_{IN}_spike (V)
6.0	1	7.0
	3	7.6
	5	9.1

To avoid unexpected voltage spike, a resistor is recommended in series with input capacitor. The circuit is shown in Figure 17.

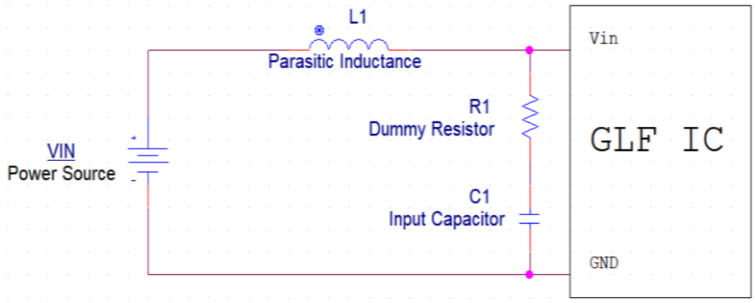


Figure 17. Reduction of voltage spike with a dummy resistor in series with input capacitor

The voltage spike is reduced from 9.1 V (Figure 16) to 6.8 V (Figure 18) by a 1 Ohm dummy resistor which is in series with the input capacitor at same external conditions, which shows a safe voltage spike less than 7 V_{Abs}.

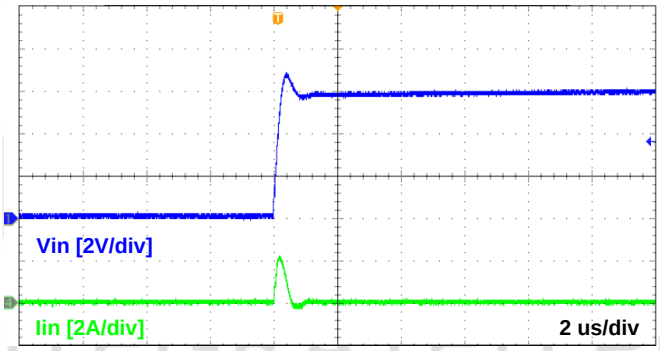


Figure 18. the voltage spike is reduced by the dummy resistor

Several combinations of wire length and dummy resistors are selected for different designs. Test results are shown in the following table. The test results show that the dump resistor can help reduce the voltage spike, and the designers can select proper value resistor in the designs based on the application conditions.

V_{IN} (V)	Dummy Resistor (Ω)	Wire Length (Cm)	V_{IN}_spike (V)
6.0	1.0	1	6.4
		3	6.5
		5	6.8
	2.2	1	6.1
		3	6.3
		5	6.4
	3.6	1	6.0
		3	6.0
		5	6.1

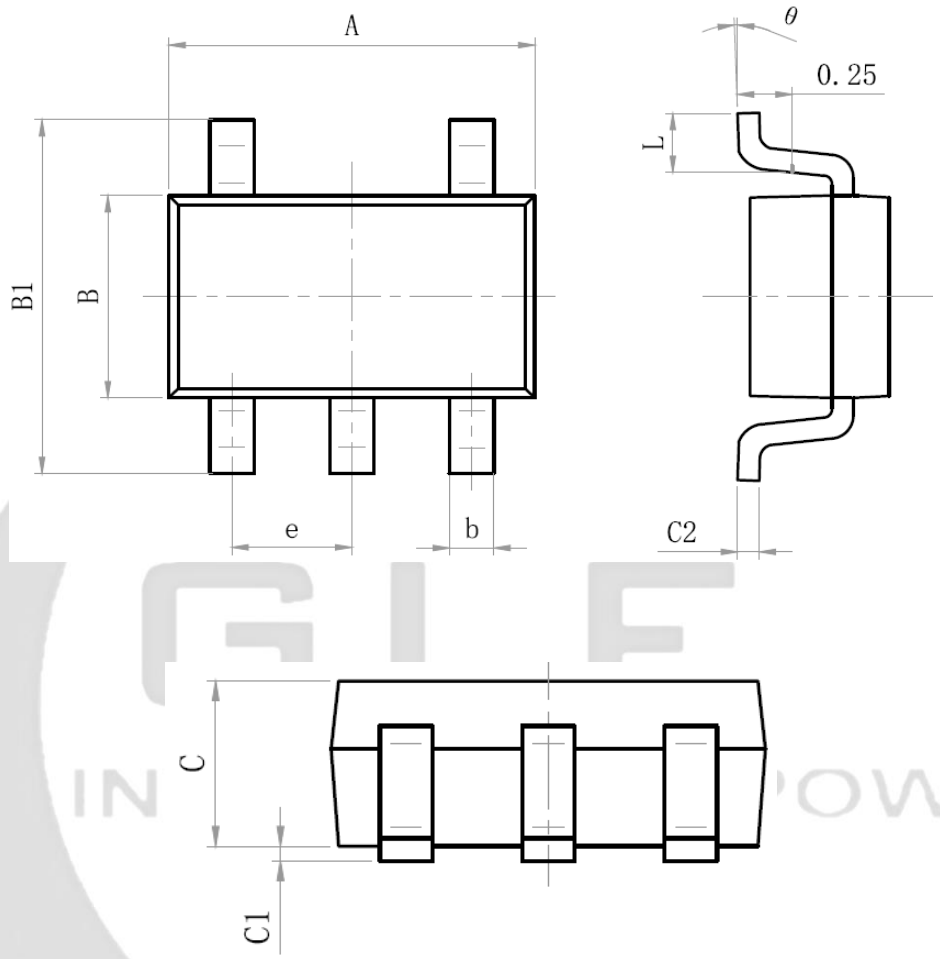
EN pin

The GLF81311 can be activated by EN pin high. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will be better to reduce parasitic effects at dynamic operations and improve thermal performance at high load current.

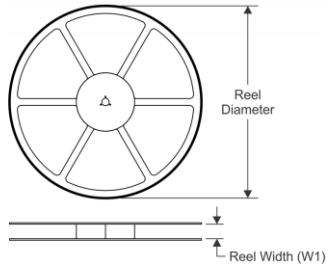
PACKAGE OUTLINE



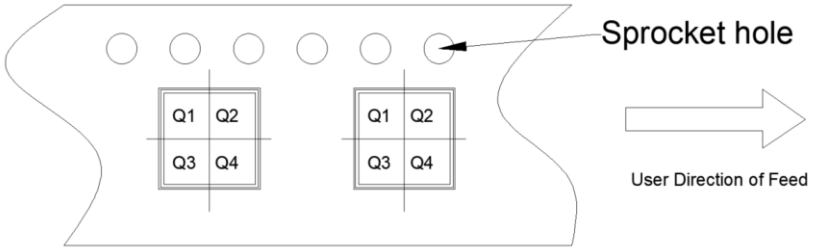
Size / Mark	Min(mm)	Max(mm)	Size / Mark	Min(mm)	Max(mm)
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°

TAPE AND REEL INFORMATION

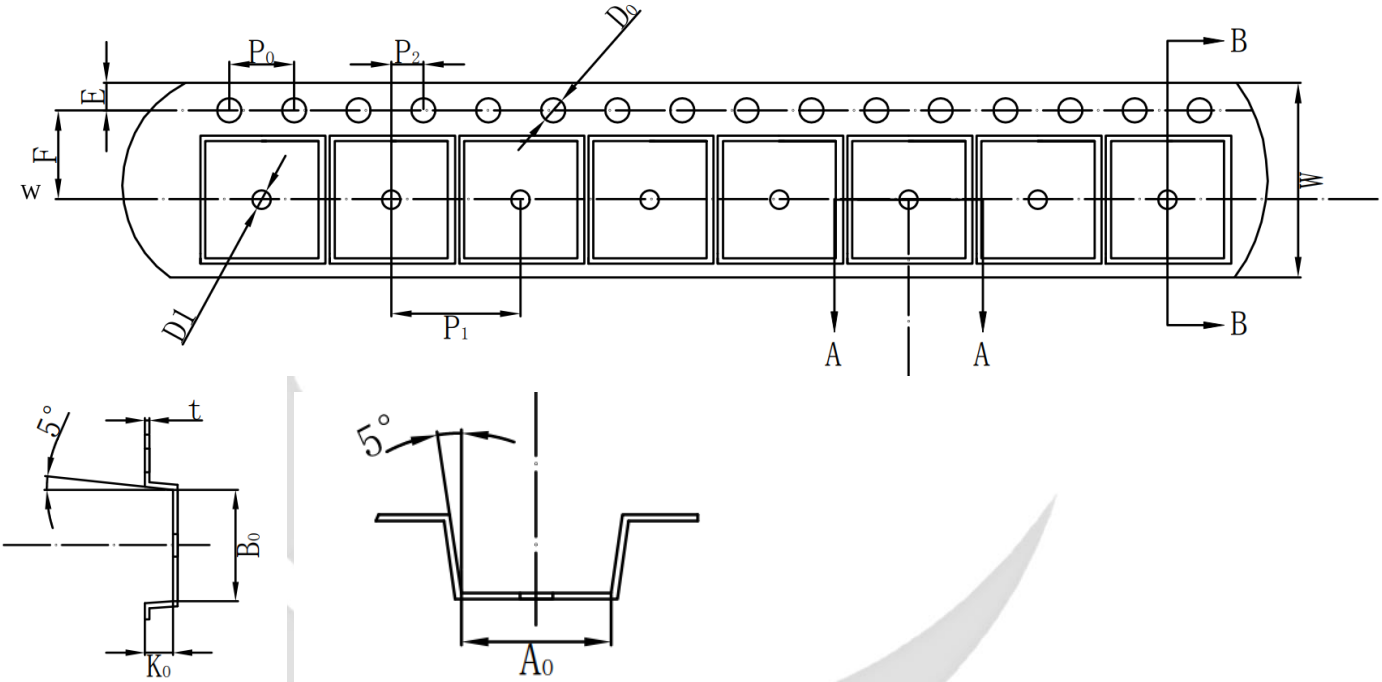
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P1	W	Pin1
GLF81311	SOT23-5	5	3000	178	9	3.25	3.30	1.38	4	8	Q3

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P1: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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