

GLF82321

I_QSmart[™] Power Load Switch with True Reverse Current Blocking

Product Specification

DESCRIPTION

The GLF82321 is an advanced technology fully integrated I_QSmart^{TM} load switch device with True Reverse Current Blocking (TRCB) technology and the slew rate control of the output voltage.

The GLF82321 offers industry leading True Reverse Current Blocking (TRCB) performance, featuring an ultra-low threshold voltage. It prevents a reverse current from Vout to Vin all the time when the output voltage exceeds the input voltage.

The GLF82321 integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF slew rate control specifically limits inrush currents during turn-on to minimize voltage droop.

The GLF82321 Load Switch devices support an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduce operating cost.

FEATURES

Supply Voltage Range: 2.0 V to 6.5 V
7.0 V_{Abs} max

• Іонт Мах: 2 A

• Low R_{ON}: 40 m Ω Typ @ 6.5 V_{IN}

 \bullet Ultra-Low $I_Q{:}~1.6~\mu A$ Typ @ 6.5 V_{IN}

• Ultra-Low I_{SD}: 20 nA Typ @ 6.5 V_{IN}

• Controlled Rise Time: 2.6 ms at 6.0 V_{IN}

• True Reverse Current Blocking

• Smart Enable Pin

 I_{EN} : 3 nA Typ at $V_{EN} > V_{IH}$ R_{EN}: 500 k Ω Typ at $V_{EN} < V_{IL}$

- Integrated Output Discharge Switch
- Wide Operating Temperature Range:

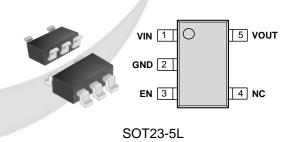
-40 °C ~ 85 °C

• HBM: 6 kV, CDM: 2 kV

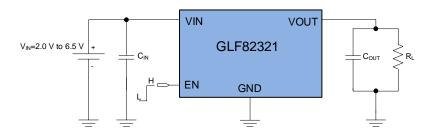
APPLICATIONS

- Smart IoT Devices
- Low Power Subsystems

PACKAGE



APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

F	Part Number	Top Mark	R _{ON} (Typ.) at 6.5 V	EN Activity	Tape and Reel Packaging
	GLF82321	DG	40 mΩ	High	3000 Pieces on 7 inch reel

FUNCTIONAL BLOCK DIAGRAM

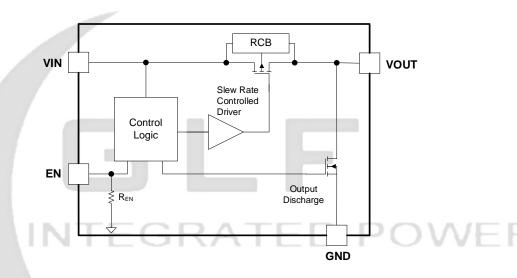


Figure 1. Functional Block Diagram

PIN CONFIGURATION

PIN DEFINITION

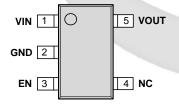


Figure 2. SOT23-5L

Pin#	Name	Description			
1	VIN	Switch Input. Supply Voltage for IC			
2	GND	Ground			
3	EN	Enable to control the switch.			
4	NC	No connection			
5	V _{OUT}	V _{OUT} pin is connected to the downstream system.			

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ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Max.	Unit
VIN, VOUT, EN	Each Pin Voltage Range to GND	-0.3	7.0	V
l _{out}	Maximum Continuous Switch Current		2	Α
PD	Power Dissipation at T _A = 25°C		1.0	W
T _{STG}	Storage Junction Temperature	-65	150	°C
TJ	Maximum Junction Temperature		150	°C
TA	Operating Temperature Range	-40	85	°C
θ_{JC}	Thermal Resistance, Junction to Case		90	°C/W
θја	Thermal Resistance, Junction to Ambient (Measured using 2S2P JEDEC std. PCB.)		180	°C/W

ESD Ratings

Symbol	Parameter			Unit
HBM	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6	kV
CDM	Electrostatic discharge Capability	Charged Device Model, JESD22-C101		ΚV

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIN	Supply Voltage	2.0	6.5	V
TA	Ambient Operating Temperature	-40	+85	°C

I_QSmart[™] Power Load Switch with True Reverse Current Blocking

ELECTRICAL CHARACTERISTICS

 V_{IN} = 2.0 V to 6.5 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Condit	tions	Min.	Тур.	Max.	Units
Basic Opera	ation						
		EN = Enable, I _{OUT} =0 mA, V _{IN} =V _{EN} =2.0 V			0.3		
		EN = Enable, I _{OUT} =0 mA, V _{IN} =V _{EN} =3.7 V			0.6		1
		EN = Enable, I _{OUT} =0 mA, V _{IN} =V _{EN} =4.2 V			0.7		
ΙQ	Supply Current	EN = Enable, I _{OUT} =0 mA, V _{IN} =V _{EN} =5.0 V			1.0		μA
		EN = Enable, I _{OUT} =0 mA, V _{IN} =V _{EN} =6.0 V			1.3		1
		EN = Enable, I _{OUT} =0 mA, V _{IN} =V _{EN} =6.5 V			1.6	2.5	
		EN=Enable, I _{OUT} =0 mA, V _{IN} =	=V _{EN} =6.5 V, Ta=85 °C ⁽²⁾		1.7		
		EN = Disable, Iout=0 mA, V	_{IN} =2.0 V		2		
		EN = Disable, Iout=0 mA, V	_{IN} =3.7 V		8		
		EN = Disable, I _{OUT} =0 mA, V _{IN} =4.2 V			12		
I_{SD}	Shutdown Current	EN = Disable, I _{OUT} =0 mA, V	_{IN} =5.0 V		14		nA
		EN = Disable, Iout=0 mA, V	IN=6.0 V		17		
		EN = Disable, I _{OUT} =0 mA, V _{IN} =6.5 V			20	50	
		EN = Disable, Iout=0 mA, V	ın=6.5 V, Та=85 °С ⁽²⁾		440		
	On-Resistance	V _{IN} = 6.5 V I _{OUT} = 500 mA	Ta=25 °C		40	48	
			Ta=85 °C		50		
		V _{IN} = 6.0 V, I _{OUT} = 500 mA	Ta=25 °C		41	49	- - mΩ
1			Ta=85 °C	<i>7 V</i>	51		
		V _{IN} = 5.0 V, I _{OUT} = 500 mA	Ta=25 °C		42		
Ron		V _{IN} = 4.2 V, I _{OUT} = 500 mA	Ta=25 °C		44		
		V _{IN} = 3.7 V, I _{OUT} = 300 mA	Ta=25 °C		46		
		V _{IN} = 3.3 V, I _{OUT} = 300 mA	Ta=25 °C		48	56	
		V _{IN} = 2.5 V, I _{OUT} = 300 mA	Ta=25 °C		54		
		V _{IN} = 2.0 V, I _{OUT} = 300 mA	Ta=25 °C		62		-
Rosc	Output Discharge Resistance	E _N =Low, I _{FORCE} = 10 mA			550		Ω
ViH	EN Input Logic High Voltage			1.5			V
V _{IL}	EN Input Logic Low Voltage	V _{IN} =2.0 to 6.5 V				0.5	V
I _{EN}	EN Current	EN Voltage > V _{IH}			3	30	nA
Ren	EN Pulldown Resistance	V _{EN} < V _{IL} , Disabled			500		kΩ
V _{RCB_TH}	RCB Protection Threshold Voltage (2)	V _{OUT} - V _{IN} , V _{IN} = 5 V			90		.,
V _{RCB_RL}	RCB Protection Release Voltage (2)	$V_{IN} - V_{OUT}$, $V_{IN} = 5 \text{ V}$			50		mV
Switching (Characteristics (1), (2)						_
t _{dON}	Turn-On Delay	V _{IN} =6.0 V, R _{OUT} = 150 Ω, C _{OUT} =1.0 μF			1.3		
t _R	V _{OUT} Rise Time				2.6		ms
tdOFF	Turn-Off Delay				21		- µs
t⊧	V _{OUT} Fall Time				360		

Notes: 1. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$ 2. By design; characterized, not production tested



TIMING DIAGRAM

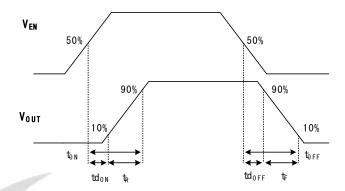
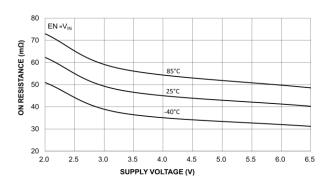


Figure 3. Timing Diagram



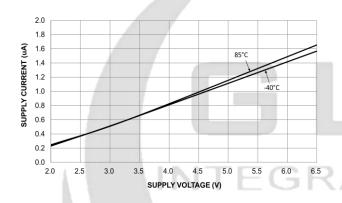
TYPICAL PERFORMANCE CHARACTERISTICS



T_J, JUNCTION TEMPERATURE (°C)

Figure 4. On-Resistance vs. Supply Voltage

Figure 5. On-Resistance vs. Temperature



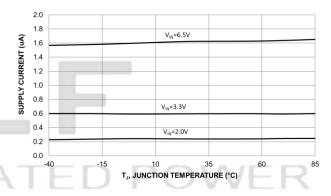
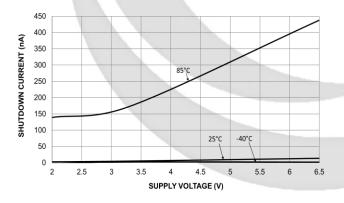


Figure 6. Quiescent Current vs. Supply Voltage

Figure 7. Quiescent Current vs. Temperature



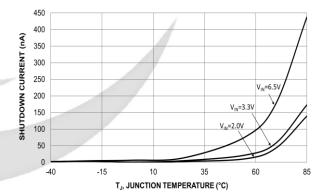
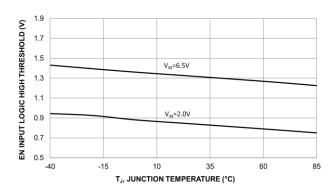


Figure 8. Shutdown Current vs. Supply Voltage

Figure 9. Shutdown Current vs. Temperature

I_QSmart[™] Power Load Switch with True Reverse Blocking



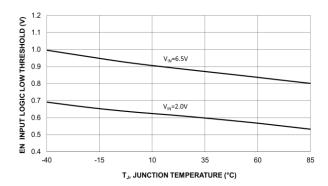


Figure 10. EN Input Logic High Threshold vs. Temperature

Figure 11. EN Input Logic High Threshold vs. Temperature

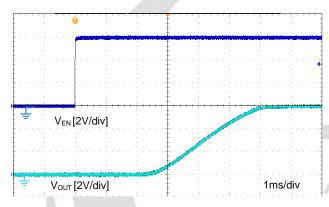


Figure 11. Turn-On Response $V_{\text{IN}}\text{=}6.0~\text{V, C}_{\text{IN}}\text{=}1.0~\mu\text{F, C}_{\text{OUT}}\text{=}1.0~\mu\text{F, R}_{\text{L}}\text{=}150~\Omega$

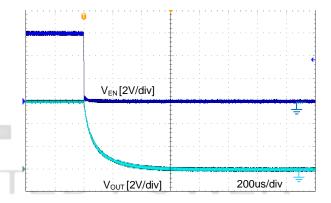


Figure 13. Turn -Off Response $\label{eq:Vin=6.0} V_{\text{IN}} = \! 6.0 \ V, \ C_{\text{IN}} = \! 1.0 \ \mu\text{F}, \ C_{\text{OUT}} = \! 1.0 \ \mu\text{F}, \ R_{\text{L}} = \! 150 \ \Omega$

IoSmart™ Power Load Switch with True Reverse Blocking

APPLICATION INFORMATION

The GLF82321 is an ultra-efficient integrated 2 A I_QSmart[™] load switch with True Reverse Current Blocking (TRCB) technology and the slew rate control of the output voltage. It is capable of operating over a wide input range from 2.0 V to 6.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power supply.

Input Capacitor

The GLF82321 requires an input capacitor to function. To reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 1µF capacitor is recommended to be placed close to V_{IN} pin. A higher input capacitor value can be used to attenuate the input voltage drop.

Output Capacitor

A 0.1uF capacitor or higher values can be able to prevent undershoot caused by parasitic inductance on board traces at switching off and improve reliability of a controlled voltage rail. The Cour should be placed close to VOUT and GND pins.

Input Voltage Spike Reduction

In steady state condition, the voltages at input pins almost equal to the input power sources. However, at the transient time when the power source is plugged in, a spike voltage will be induced at input pin. The level of the voltage spike is determined by the parasitic inductance between power source and input pin as well as the change rate of input current. The longer length between power source and input pin, the faster change rate of input current, the larger voltage spike. If the spike voltage level exceeds the absolute maximum rated input voltage, it may damage the chip permanently. Below is the waveform when a 6.0 V power source is "hot" plugged in, and the voltage spike can be up to 9.1 V. A "hot" plug-in is not recommended all the time.

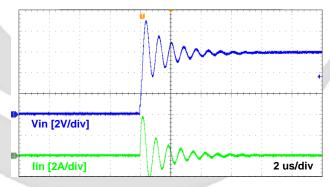


Figure 14. the voltage spike when the power source is "hot" plugged in (IC is disabled)

The voltage spikes are tested with different wire length between the power source and input pin. The results are shown in the table below.

V _{IN} (V)	Wire Length (Cm)	V _{IN} _spike (V)
	1	7.0
6.0	3	7.6
	5	9.1

To avoid unexpected voltage spike, a resistor is recommended in series with input capacitor. The circuit is shown in Figure 15.

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Figure 15. Reduction of voltage spike with a dummy resistor in series with input capacitor

The voltage spike is reduced from 9.1 V (Figure 17) to 6.8 V (Figure 19) by a 1 Ohm dummy resistor which is in series with the input capacitor at same external conditions, which shows a safe voltage spike less than 7.0 V_{Abs} .

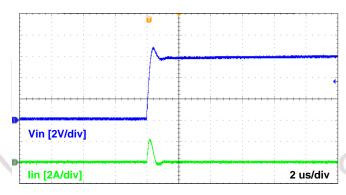


Figure 16. the voltage spike is reduced by the dummy resistor

Several combinations of wire length and dummy resistors are selected for different designs. Test results are shown in the following table. The test results show that the dump resistor can help reduce the voltage spike, and the designers can select proper value resistor in the designs based on the application conditions.

V _{IN} (V)	Dummy Resistor (Ω)	Wire Length (Cm)	V _{IN} _spike (V)		
		1	6.4		
	1.0	3	6.5		
		5	6.8		
		1	6.1		
6.0	2.2	3	6.3		
		.0	6.4		
	3.6	1	6.0		
	3.0	3	6.0		
		5	6.1		

EN pin

The GLF82321 can be activated by EN pin high. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller.



True Reverse Current Blocking

The GLF82321 has a built-in reverse current blocking protection which always monitors the output voltage level regardless of the status of EN pin to check if it is greater than the input voltage. When the output voltage goes beyond the input voltage by the RCB Protection Threshold Voltage (V_{RCB_TH}). that is the reverse current blocking protection trip voltage, the reverse current blocking function block turns off the switch. Note that some reverse current can occur until the V_{RCB} is triggered. The main switch will resume normal operation when the output voltage drops below the input source by the TRCB protection release voltage.

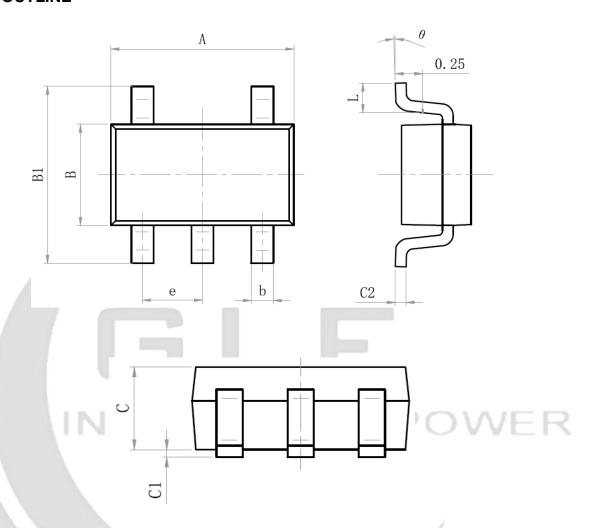
Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will be better to reduce parasitic effects at dynamic operations and improve thermal performance at high load current.





PACKAGE OUTLINE



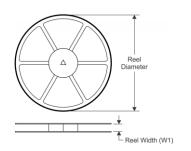
Size Mark	Min(mm)	Max(mm)	Size Mark	Min(mm)	Max(mm)
A	2.82	3.02	С	1.05	1. 15
е	0.9	95 (BSC)	C1	0.03	0.15
b	0. 28	0.45	C2	0.12	0. 23
В	1.50	1.70	L	0.35	0. 55
B1	2.60	3.00	θ	0°	8°

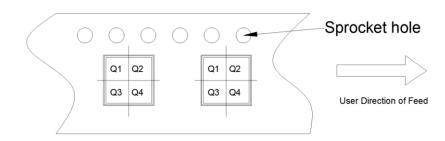


TAPE AND REEL INFORMATION

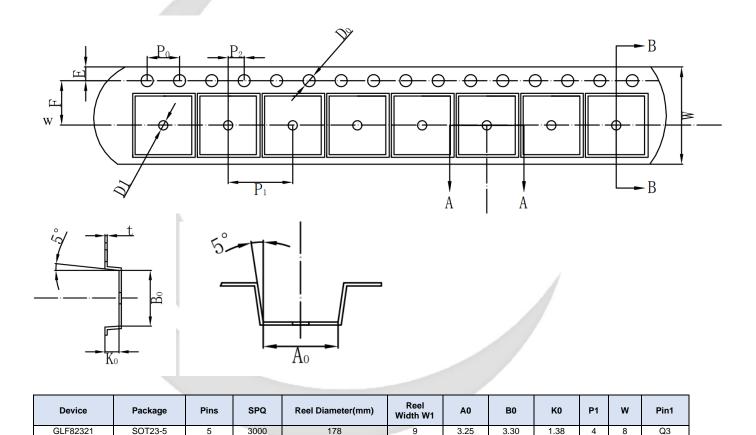
REEL DIMENSIONS

QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE





TAPE DIMENSIONS



Remark:

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- C0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

GLF82321

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status	
Target Specification			
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification	
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production	

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