GLF1531Q

2 A Power Switch with Programmable Slew Rate Control

Product Specification

DESCRIPTION

The GLF1531Q is an ultra-efficiency integrated N-channel power protection switch, with a wide input range from 0.8 V to 5.5 V.

The GLF1531Q provides the programmable output voltage (V_{OUT}) rise time by an external capacitor on the SR pin. It limits the inrush current at start up condition and helps to minimize the voltage drop. The integrated output discharge FET discharges output voltage quickly when the device is disabled.

The GLF1531Q offers the best-in-class on the size, on-resistance (R_{ON}) performance, and the wide operating temp range up to 125 °C.

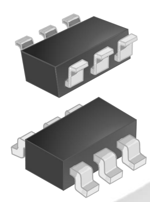
FEATURES

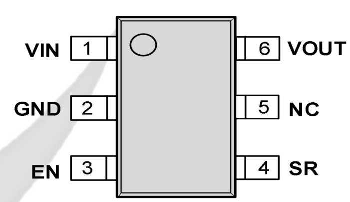
- AEC-Q100 Qualified
- Qualified for Automotive Applications:
  Temperature Grade 1:
  -40 °C to 125 °C Ambient Operating
  Temperature Range
- Supply Voltage Range: 0.8 V to 5.5 V
  6 V_{ABS} max
- Continuous Output Current: 2 A
- Low R_{ON}: 44 mΩ at 25 °C Typ. at 5 V_{IN}
- Low Quiescent Current I_Q:
  14 µA Typ. at 5 V_{IN}
  7 µA Typ. at 3.3 V_{IN}
- Low Shutdown Current I_{SD}:
  13 nA Typ. at 5 V_{IN}
  10 nA Typ. at 3.3 V_{IN}
- Programmable V_{OUT} Rising Time, SR Pin
- Quick Output Discharge
- ESD Performance per AEC-Q100
- Moisture Sensitivity Level: MSL-3 and 260 °C Peak Reflow Temp
- Lead-free, Halogen-free and Adhere to RoHS Directive

APPLICATIONS

- Automotive Electronics
- Infotainment and Cluster
- Automotive Gateway
- ADSA (Advanced Driver Assistance System)

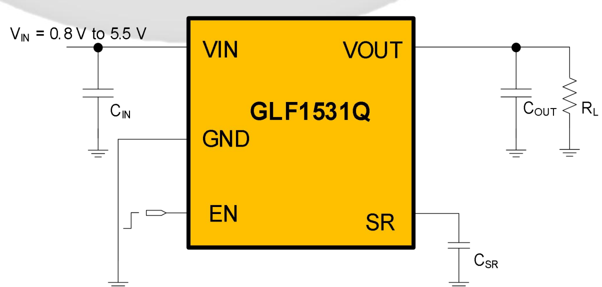
PACKAGE





SOT23 - 6L

APPLICATION DIAGRAM



DEVICE ORDERING INFORMATION

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V_{IN}	V_{OUT} Rise Time	EN Activity	Package
GLF1531Q-T2G7	HQ	44 mΩ	Programmable	High	SOT23 - 6L

FUNCTIONAL BLOCK DIAGRAM

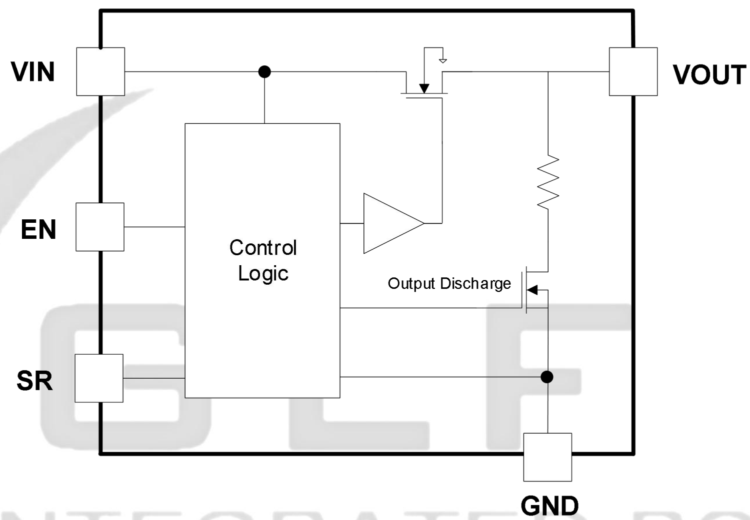


Figure 1. Functional Block Diagram

PIN CONFIGURATION

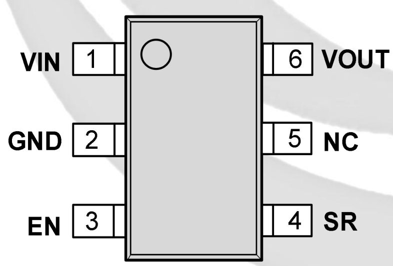


Figure 2. Package and Pin configuration

PIN DEFINITION

Pin No.	Name	Description
1	VIN	Switch Input. Supply Voltage
2	GND	Ground
3	EN	Active high signal to enable the switch
4	SR	Soft-start Pin by connecting a capacitor to control the output voltage rise time at turn-on.
5	NC	No connection. Leave this pin float or tie to GND.
6	VOUT	Switch Output

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not be function or operable above the recommended operating conditions and extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VIN, VOUT EN, SR	Voltage from each pin to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2	A
$T_{J(Max)}$	Junction Temperature			150	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			180	°C/W
θ_{JC}	Thermal Resistance, Junction to Case			130	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	±2		kV
		Charged Device Model, JESD22-C101	±1		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	0.8	5.5	V
T_A	Ambient Operating Temperature	-40	+125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.8 V to 5.5 V, typical values are at V_{IN} = 3.3 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
I_Q	Quiescent Current (1)	$V_{IN} = V_{EN}$ = 5.5 V, I_{OUT} = 0 mA		19	22	µA
		$V_{IN} = V_{EN}$ = 5.0 V, I_{OUT} = 0 mA		14	18	
		$V_{IN} = V_{EN}$ = 3.3 V, I_{OUT} = 0 mA		7	10	
		$V_{IN} = V_{EN}$ = 2.5 V, I_{OUT} = 0 mA		5		
		$V_{IN} = V_{EN}$ = 0.8 V, I_{OUT} = 0 mA		6		
		$V_{IN} = V_{EN}$ = 5 V, I_{OUT} = 0 mA, T_A = 85 °C (4)		23		
		$V_{IN} = V_{EN}$ = 5 V, I_{OUT} = 0 mA, T_A = 125 °C		70	110	
I_{SD}	Shutdown Current	V_{IN} = 5.5 V, V_{EN} = 0 V, I_{OUT} = 0 mA		15	30	nA
		V_{IN} = 5.0 V, V_{EN} = 0 V, I_{OUT} = 0 mA		13	30	
		V_{IN} = 3.3 V, V_{EN} = 0 V, I_{OUT} = 0 mA		10	25	
		V_{IN} = 2.5 V, V_{EN} = 0 V, I_{OUT} = 0 mA		9		
		V_{IN} = 0.8 V, V_{EN} = 0 V, I_{OUT} = 0 mA		7		
		V_{IN} = 5 V, V_{EN} = 0 V, I_{OUT} = 0 mA, T_A = 85 °C (4)		520		
		V_{IN} = 5 V, V_{EN} = 0 V, I_{OUT} = 0 mA, T_A = 125 °C		5	8	µA

R_{ON}	On-Resistance	V_{IN} = 0.8 V to 5.5 V I_{OUT} = 200 mA	T_A = 25 °C		44	51	mΩ
			T_A = 85 °C [4]		52		
			T_A = 125 °C		64	85	
V_{IH}	EN Input Logic High Voltage	V_{IN} = 0.8 V to 1.5 V, T_A= -40 °C to +125 °C		0.7			V
		V_{IN} = 1.5 V to 5.5 V, T_A= -40 °C to +125 °C		1.2			
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 0.8 V to 1.5 V, T_A= -40 °C to +125 °C				0.05	
		V_{IN} = 1.5 V to 5.5 V, T_A= -40 °C to +125 °C				0.15	
R_{EN}	EN Pull-down Resistor				10		MΩ
R_{DSC}	Quick Output Discharge Resistance	V_{EN} = Low, I_{FORCE} = 10 mA			21		Ω
Switching Characteristics [3], [4]							
t_{dON}	Turn-On Delay	V_{IN} = 5 V	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF, C_{SR} =1 nF, T_A = 25 °C		450		μs
t_R	V_{OUT} Rise Time				2830		
t_{dOFF}	Turn-Off Delay				0.5		
t_F	V_{OUT} Fall Time				2		
t_{dON}	Turn-On Delay	V_{IN} = 3.3 V			460		
t_R	V_{OUT} Rise Time				2230		
t_{dOFF}	Turn-On Delay				1		
t_F	V_{OUT} Fall Time				2		
t_{dON}	Turn-On Delay	V_{IN} = 1 V			620		
t_R	V_{OUT} Rise Time				1320		
t_{dOFF}	Turn-On Delay				16		
t_F	V_{OUT} Fall Time				9		

Notes:
1. I_Q does not include the current through the pulldown resistor (R_{EN}) of the EN pin
2. Output discharge switch is enabled when the device is disabled.
3. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$
4. By design; characterized, not production tested

TIMING DIAGRAM

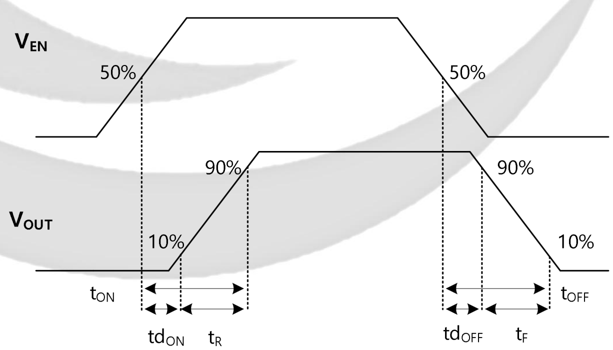


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

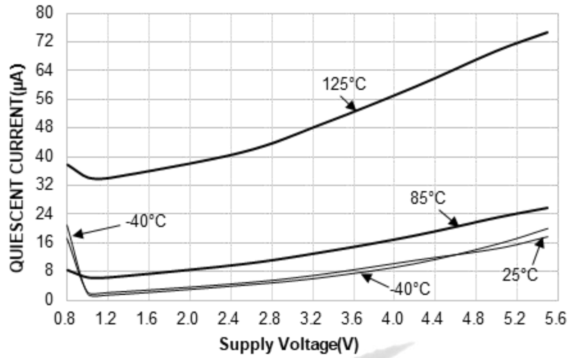


Figure 4. Quiescent Current vs. Supply Voltage

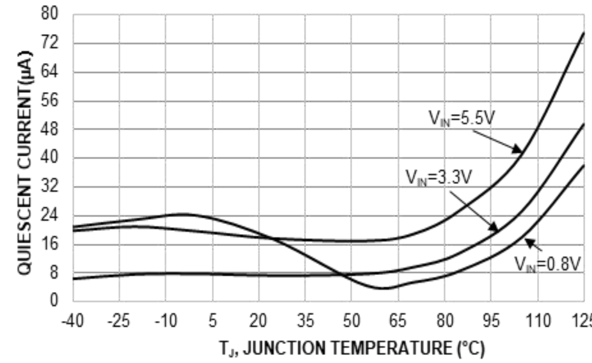


Figure 5. Quiescent Current vs. Temperature

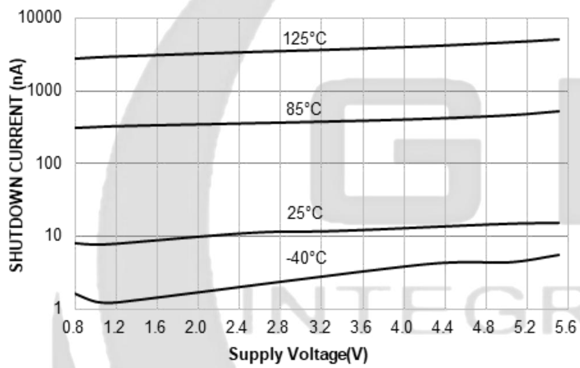


Figure 6. Shutdown Current vs. Supply Voltage

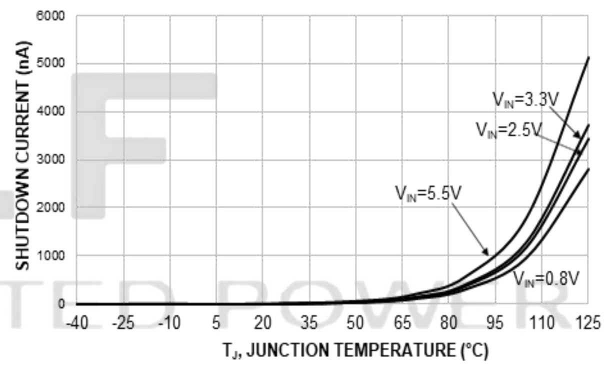


Figure 7. Shutdown Current vs. Temperature

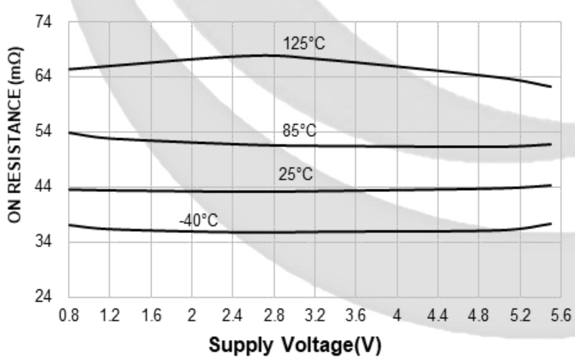


Figure 8. On-Resistance vs. Supply Voltage

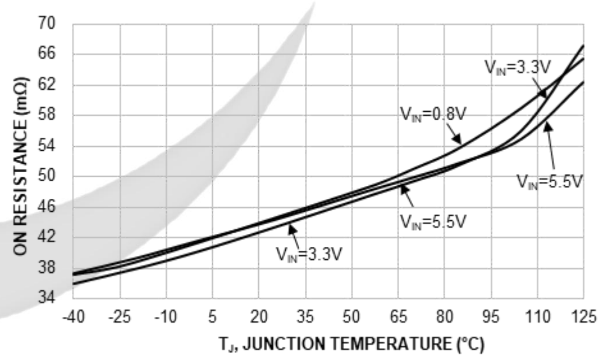


Figure 9. On-Resistance vs. Temperature

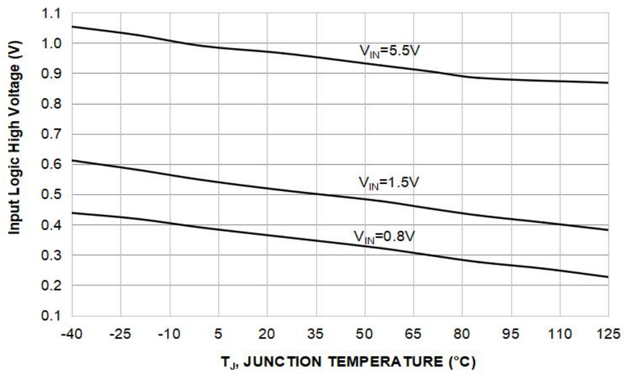


Figure 10. EN Input Logic High Threshold vs. Temperature

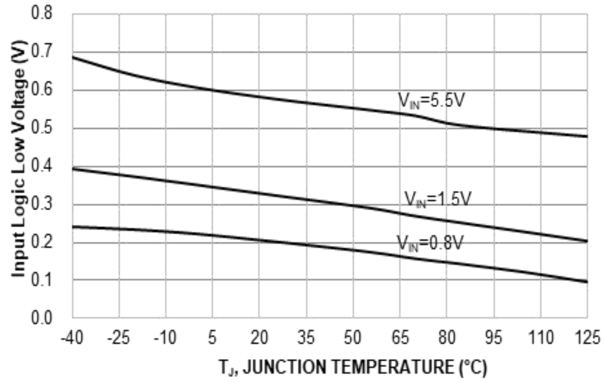


Figure 11. EN Input Logic Low Threshold vs. Temperature

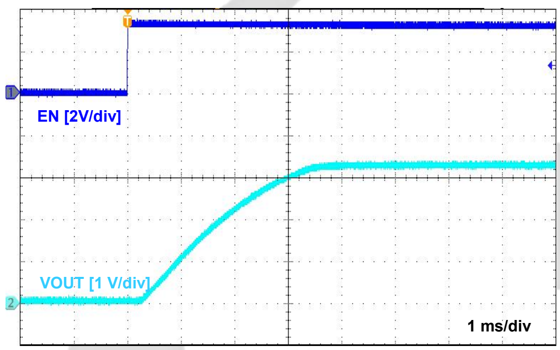


Figure 12. Turn-On Response

V_{IN}=3.3 V, C_{IN}=1 μF, C_{OUT}=0.1 μF, C_{SR}=1 nF, R_L=10 Ω

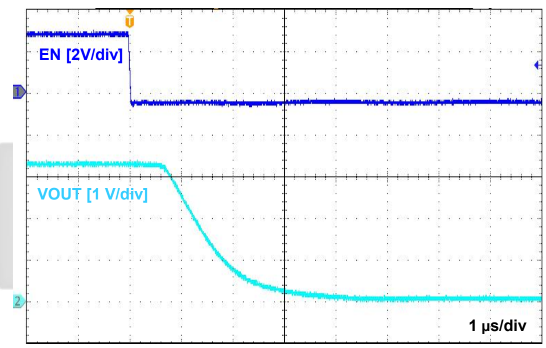


Figure 13. Turn-Off Response

V_{IN}=3.3 V, C_{IN}=1 μF, C_{OUT}=0.1 μF, C_{SR}=1 nF, R_L=10 Ω

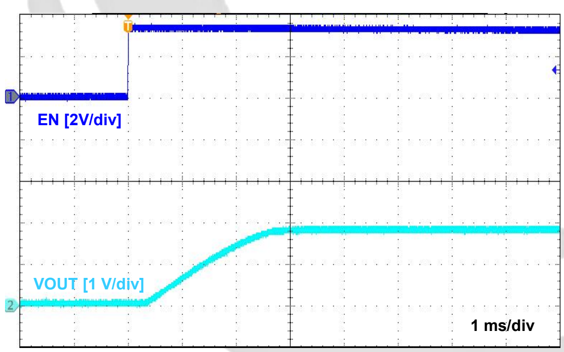


Figure 14. Turn-On Response

V_{IN}=1.8 V, C_{IN}=1 μF, C_{OUT}=0.1 μF, C_{SR}= 1 nF, R_L=10 Ω

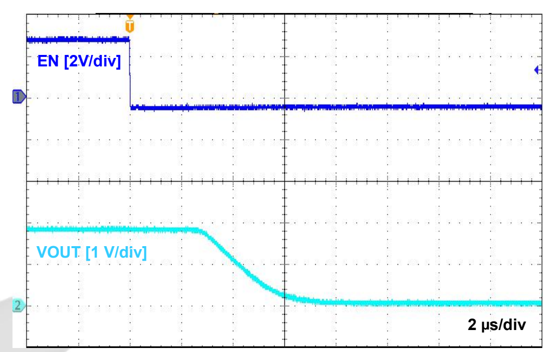


Figure 15. Turn-Off Response

V_{IN}=1.8 V, C_{IN}=1 μF, C_{OUT}=0.1 μF, C_{SR}=1 nF, R_L=10 Ω

APPLICATION INFORMATION

The GLF1531Q is a 2 A fully integrated load switch with the programmable slew rate control to limit the inrush current during turn on. The device is capable to operate over a wide input range from 0.8 V to 5.5 V along with very low on-resistance, in result to reduce conduction loss. The device consumes very low leakage current to avoid the extra standby current and then improve power consumption at the off state.

Programmable Output Voltage Rise Time

An external capacitor between the SR and GND pin sets the output voltage slew rate of each channel individually. Table 1 is for selecting rising time by different C_{SR} and V_{IN}.

C_{SR} (pF)	Rise Time of Output Voltage, t_R Typ (µs) C_{OUT} = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, T_A = 25 °C						
	5.0 V_{IN}	3.3 V_{IN}	2.5 V_{IN}	1.8 V_{IN}	1.5 V_{IN}	1.0 V_{IN}	0.8 V_{IN}
0	293	269	266	229	233	216	200
220	813	677	645	570	520	489	449
470	1313	1176	1010	885	831	747	680
1000	2830	2230	1904	1545	1509	1320	1120
2200	5230	4634	3994	3390	3134	2821	2559
4700	11660	9401	8714	7276	6833	6025	5446
10000	22600	19080	17330	14580	13620	12170	11200

Table 1. V_{OUT} Rise Time (µs) vs. C_{SR} & V_{IN}

Input and Output Capacitor

A minimum 0.1 µF input capacitor is recommended to place close to the VIN pin to reduce the voltage drop on the input power rail, which caused by transient inrush current at start-up. A higher input capacitance value is to attenuate the input voltage drop. Also, a minimum 0.1 µF output capacitor is recommended to minimize voltage undershoot happened at the output pin when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances exist, an output capacitor can improve the output voltage stability and system reliability. The C_{OUT} capacitor must be placed to the VOUT and GND pins as close as possible.

EN Pin

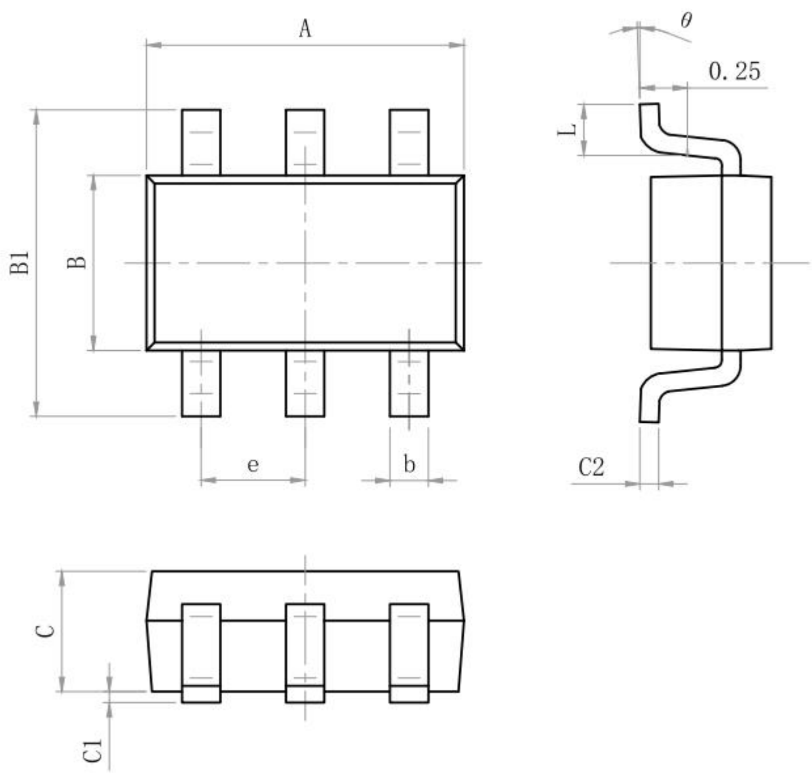
The EN pin controls the state of the device. The EN pin is compatible with the GPIO logic standard and has a low threshold which makes it capable to adapt the low-voltage signal. It can be used for any micro-controller with 1 V or higher GPIO voltage.

Board Layout

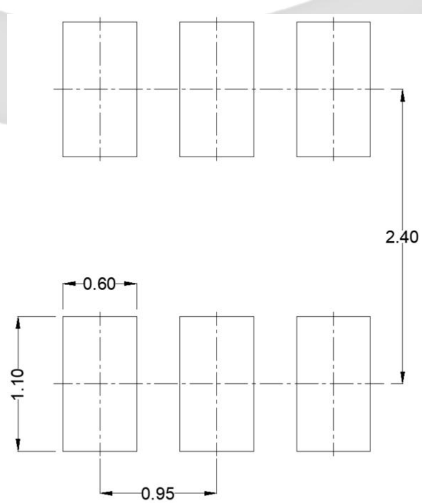
All traces should be as short as possible to minimize parasitic inductance. Wide traces of VIN, VOUT, and GND can reduce parasitic effects under dynamic operations to improve thermal performance at high current loading.

PACKAGE OUTLINE

Mark \ Size	Min (mm)	Max (mm)	Mark \ Size	Min (mm)	Max (mm)
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°

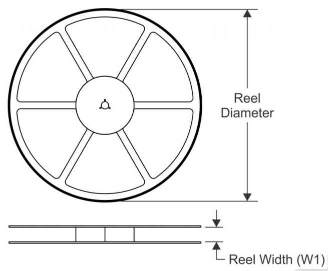


Recommended Footprint

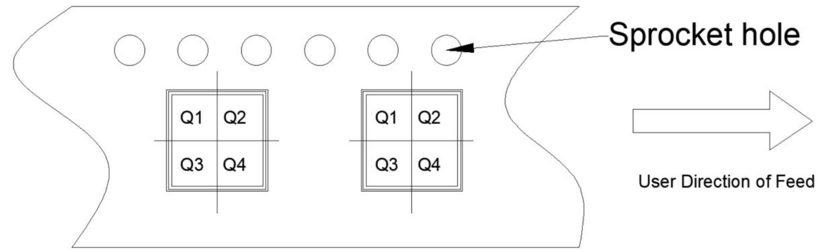


TAPE AND REEL INFORMATION

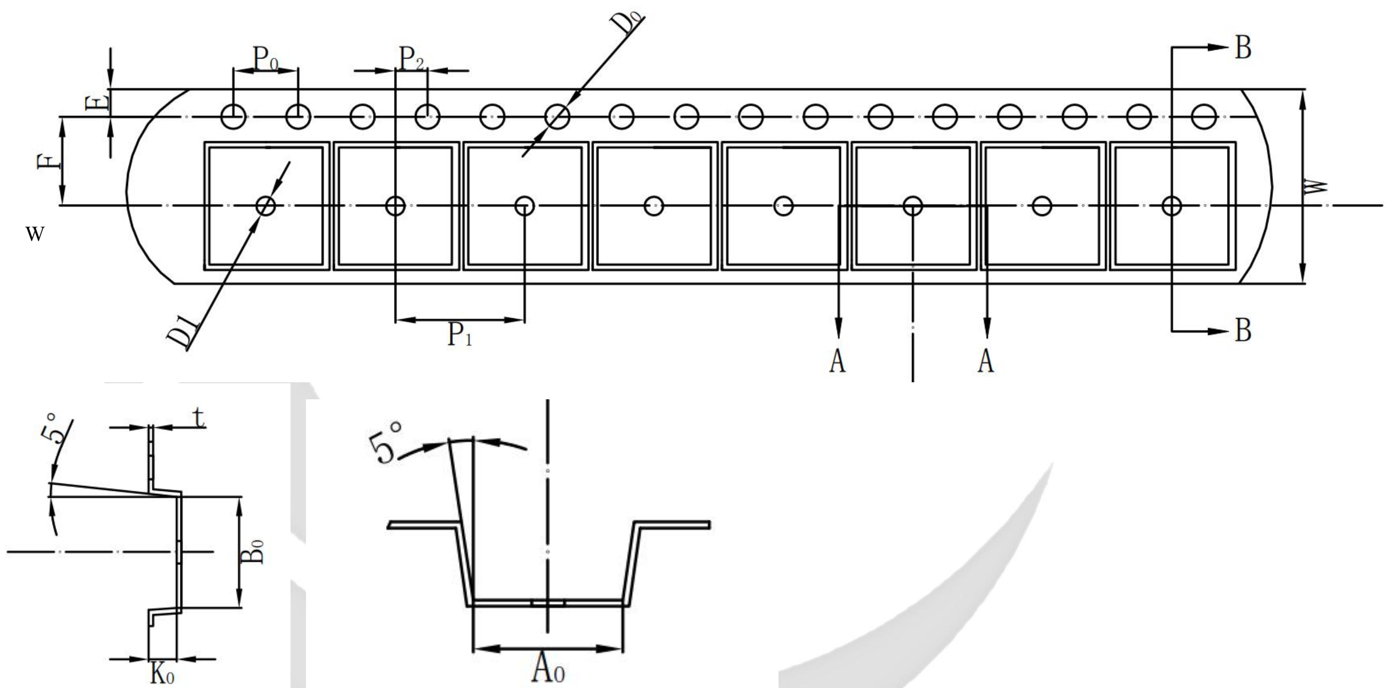
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel WidthW1	A0	B0	K0	P1	W	Pin1
GLF1531Q-T2G7	SOT23-6	6	3000	178	9	3.25	3.30	1.38	4	8	Q3

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P1: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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