GLF71307
Nano-Current Consumed, I$_Q$Smart™ LoadSwitch with Slew Rate Control

Product Specification

DESCRIPTION

The GLF71307 is an ultra-efficiency, 2.0 A rated, integrated load switch with integrated slew rate control. The best in class efficiency makes it an ideal choice for use in IoT, mobile, and wearable electronics.

The GLF71307 features an ultra-efficient I$_Q$Smart™ technology that supports the lowest quiescent current (I$_Q$) and shutdown current (I$_{SD}$) inx the industry. Low I$_Q$ and I$_{SD}$ solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF71307 integrated slew rate control greatly enhances system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF slew rate control specifically limits inrush currents during turn-on to minimize voltage droop.

The GLF71307 can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

The GLF71307 Load Switch device is small utilizing a wafer level chip scale package with 4 bumps in a 0.77 mm x 0.77 mm x 0.46 mm die size and a 0.4mm bump pitch.

FEATURES

- Ultra-Low I$_Q$: 1 nA Typ @ 5.5 V$_{IN}$
- Ultra-Low I$_{SD}$: 19 nA Typ @ 5.5 V$_{IN}$
- Low R$_{ON}$ = 34 mΩ Typ @ 5.5 V$_{IN}$
- I$_{OUT}$ Max = 2.0 A
- Wide Input Range: 1.1 V to 5.5 V
  6 V abs max
- Controlled Rise Time: 9 us at 3.3 V$_{IN}$
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- Temperature Range: - 40 to 85 °C
- HBM: 6 kV, CDM: 2 kV
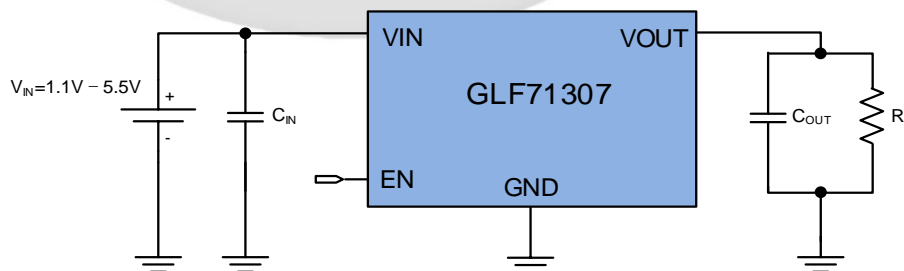- Ultra-Small: 0.77 mm x 0.77 mm

APPLICATIONS

- Wearables
- Data Storage, SSD
- Mobile Devices
- Low Power Subsystems

PACKAGE

| VOUT A1 | VIN A2 |
| GND B1 | EN B2 |

TOP VIEW

| VIN A2 | VOUT A1 |
| EN B2 | GND B1 |

BOTTOM VIEW
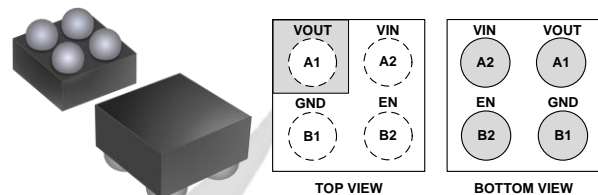
0.77 mm x 0.77 mm x 0.46 mm WLCSP

APPLICATION DIAGRAM

ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V	Output Discharge	EN Activity	Availability
GLF71307	S	34 mΩ	85 Ω	High	Released

FUNCTIONAL BLOCK DIAGRAM
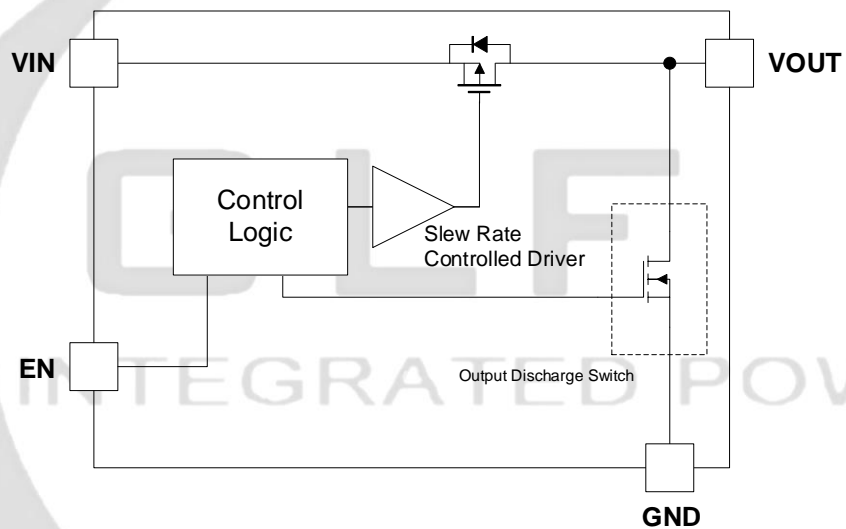
Figure 1. Functional Block Diagram

PIN CONFIGURATION

TOP VIEW

VOUT A1 | VIN A2
GND B1 | EN B2

BOTTOM VIEW

VIN A2 | VOUT A1
EN B2 | GND B1

Figure 2. 0.77 mm x 0.7 7mm x 0.46 mm WLCSP

PIN DEFINITION
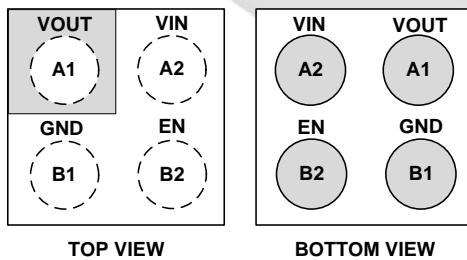
Pin #	Name	Description
A1	V_{OUT}	Switch Output
A2	V_{IN}	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V$_{IN}$, V$_{OUT}$, V$_{EN}$	Each Pin Voltage Range to GND		-0.3	6	V
I$_{OUT}$	Maximum Continuous Switch Current			2	A
P$_D$	Power Dissipation at T$_A$ = 25 °C			1	W
T$_{STG}$	Storage Temperature		-65	150	°C
T$_A$	Operating Temperature Range		-40	85	°C
θ$_{JA}$	Thermal Resistance, Junction to Ambient (board dependent)			110	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V$_{IN}$	Supply Voltage	1.1	5.5	V
T$_A$	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

Values are at V$_{IN}$ = 3.3 V and T$_A$ = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
V$_{IN}$	Supply Voltage			1.1		5.5	V
I$_Q$	Quiescent Current	EN = Enable, I$_{OUT}$=0 mA, V$_{IN}$ = V$_{EN}$ =5.5 V			1		nA
		EN=Enable, I$_{OUT}$=0 mA, V$_{IN}$=V$_{EN}$=5.5 V, Ta=85 °C [4]			7		
I$_{SD}$	Shutdown Current	EN = Disable, I$_{OUT}$=0 mA, V$_{IN}$=1.1 V			3		nA
		EN = Disable, I$_{OUT}$=0 mA, V$_{IN}$=1.8 V			4		
		EN = Disable, I$_{OUT}$=0 mA, V$_{IN}$=3.3 V			6		
		EN = Disable, I$_{OUT}$=0 mA, V$_{IN}$=4.5 V			9		
		EN = Disable, I$_{OUT}$=0 mA, V$_{IN}$=5.5 V			19	50	
		EN = Disable, I$_{OUT}$=0 mA, V$_{IN}$=5.5 V, Ta=55 °C [4]			110		
		EN = Disable, I$_{OUT}$=0 mA, V$_{IN}$=5.5 V, Ta=85 °C [4]			600		
R$_{ON}$	On-Resistance	V$_{IN}$=5.5 V, I$_{OUT}$= 500 mA	Ta=25 °C		34	47	mΩ
			Ta=85 °C [4]		40		
		V$_{IN}$=3.3 V, I$_{OUT}$= 500 mA	Ta=25 °C		42	56	
			Ta=85 °C [4]		50		
		V$_{IN}$=1.8 V, I$_{OUT}$= 300 mA	Ta=25 °C		68		
		V$_{IN}$=1.2 V, I$_{OUT}$= 100 mA	Ta=25 °C		125		
		V$_{IN}$=1.1 V, I$_{OUT}$= 100 mA	Ta=25 °C		155		
R$_{DSC}$	Output Discharge Resistance	E$_N$=Low , I$_{FORCE}$= 10 mA		70	85	100	Ω
V$_{IH}$	EN Input Logic High Voltage	V$_{IN}$=1.1 V - 1.8 V		0.9			V
		V$_{IN}$=1.8 V - 5.5 V		1.2			V
V$_{IL}$	EN Input Logic Low Voltage	V$_{IN}$=1.1 V - 1.8 V				0.3	V
		V$_{IN}$=1.8 V - 5.5 V				0.4	V
R$_{EN}$	EN Pulldown resistance	Internal Resistance		7	10.1	13	MΩ
I$_{EN}$	EN Current	E$_N$=5.5 V				0.8	µA
Switching Characteristics							
t$_{dON}$	Turn-On Delay[1]	R$_L$=150 Ω, C$_{OUT}$=0.1 µF			7.4		µs
t$_R$	V$_{OUT}$ Rise Time[1]				8.7		
t$_{dON}$	Turn-On Delay[1,4]	R$_L$=500 Ω, C$_{OUT}$=0.1 µF			7.3		
t$_R$	V$_{OUT}$ Rise Time[1,4]				8.2		
t$_{dOFF}$	Turn-Off Delay[2,3,4]	R$_L$=10 Ω, C$_{OUT}$=0.1 µF			0.5		
t$_F$	V$_{OUT}$ Fall Time[2,3,4]				1.0		
t$_{dOFF}$	Turn-Off Delay[2,3,4]	R$_L$=500 Ω, C$_{OUT}$=0.1 µF			1.1		
t$_F$	V$_{OUT}$ Fall Time[2,3,4]				20.6		

Notes:
1. t$_{ON}$ = t$_{dON}$ + t$_R$
2. t$_{OFF}$ = t$_{dOFF}$ + t$_F$
3. Output discharge path is enabled during off.
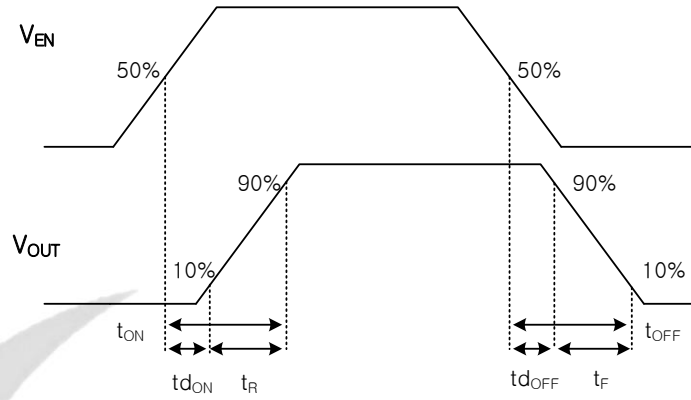4. By design; characterized; not production tested.

TIMING DIAGRAM

Figure 3. **Timing Diagram**

GLF INTEGRATED POWER

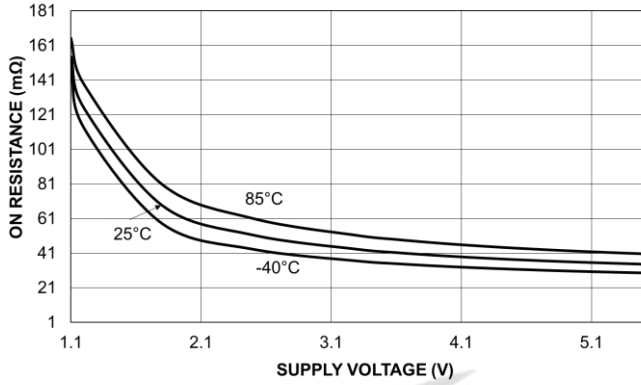## TYPICAL PERFORMANCE CHARACTERISTICS
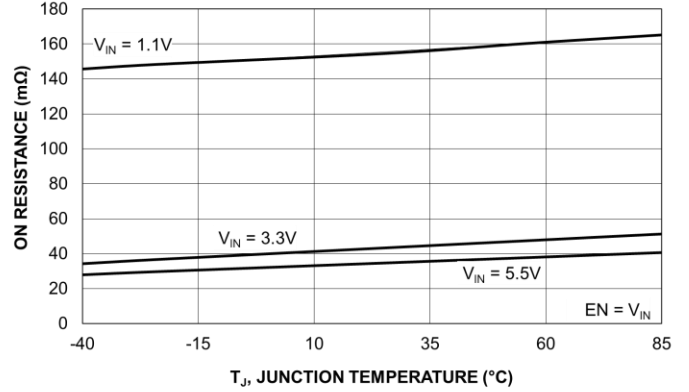
Figure 4. On-Resistance vs. Supply Voltage

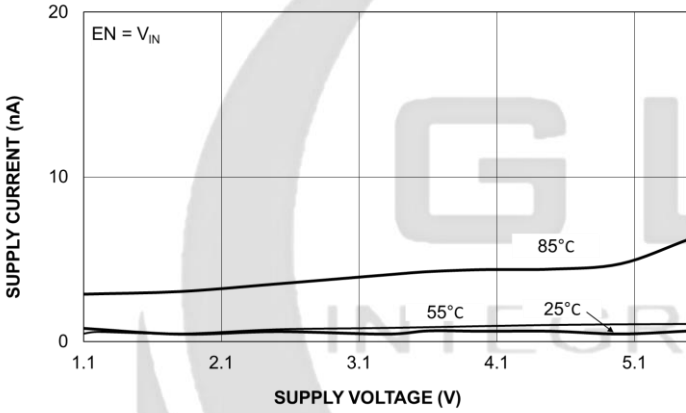**Figure 5. On-Resistance vs. Temperature**

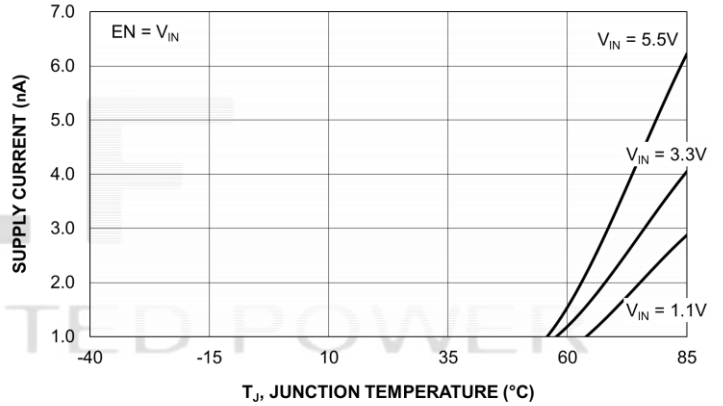**Figure 6. Quiescent Current vs. Supply Voltage**
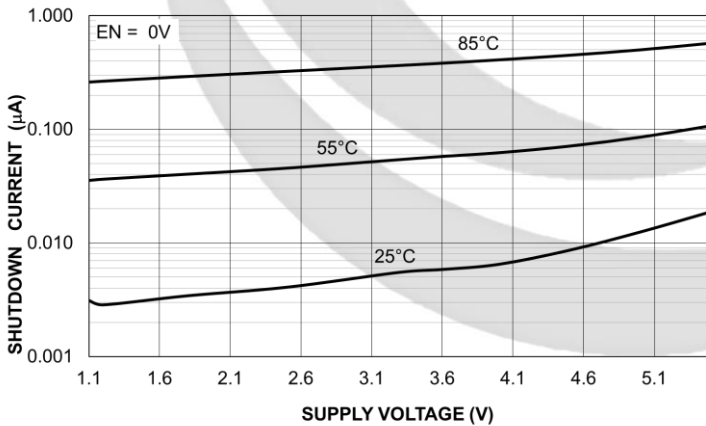
Figure 7. Quiescent Current vs. Temperature
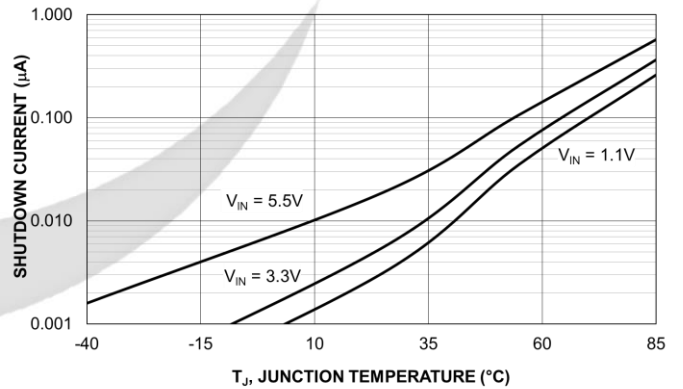
Figure 8. Shutdown Current vs. Supply Voltage
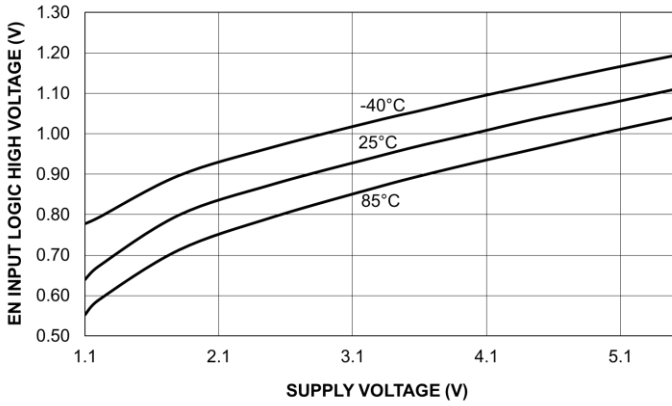
Figure 9. Shutdown Current vs. Temperature
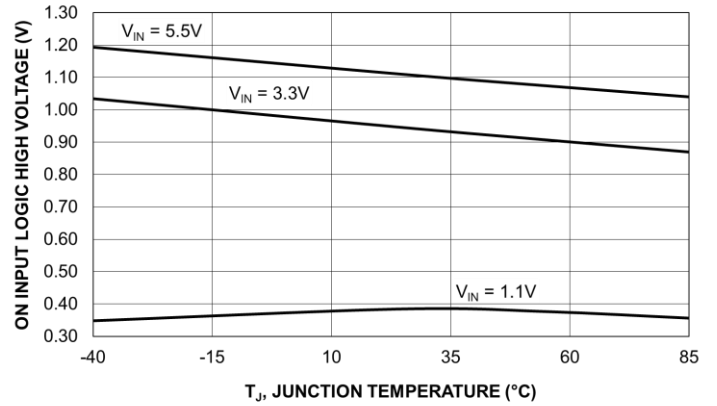
Figure 10. EN Input Logic High Threshold

Figure 11. EN Input Logic High Threshold Vs. Temperature
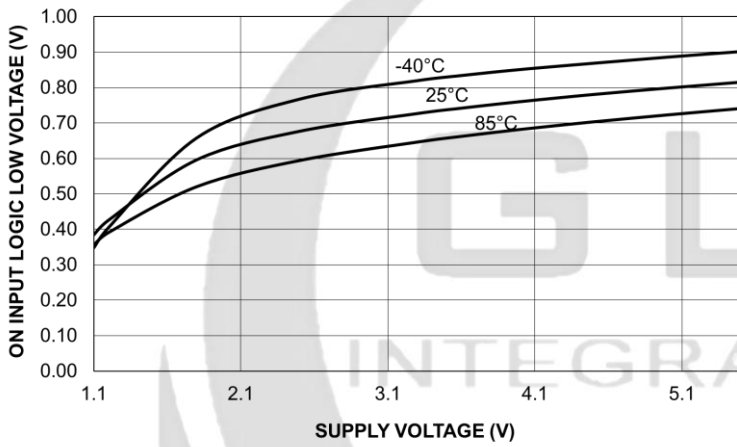
Figure 12. EN Input Logic Low Threshold
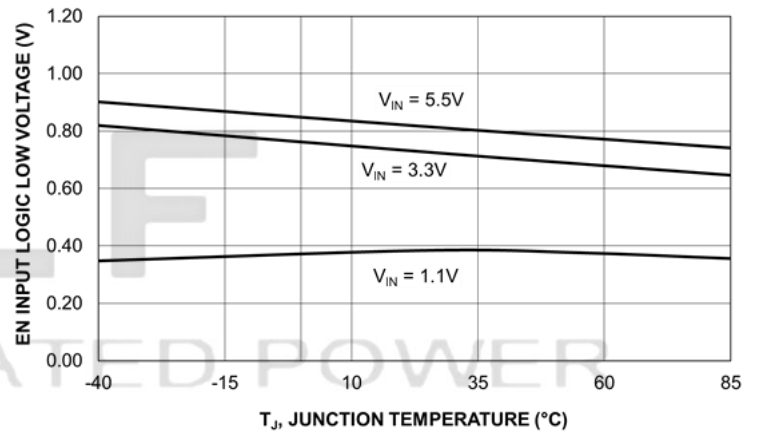

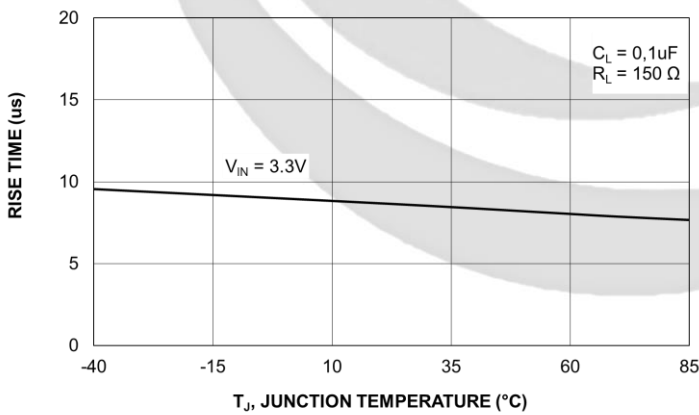**Figure 13. EN Input Logic Low Threshold Vs. Temperature**

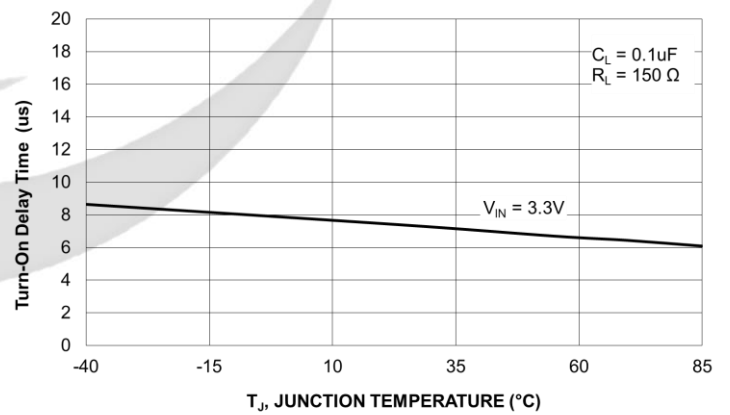**Figure 14. V_{OUT} Rise Time vs. Temperature**

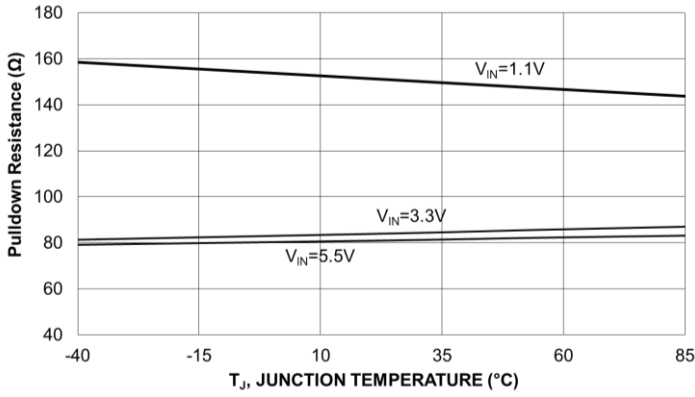**Figure 15. Turn-On Delay Time vs. Temperature**
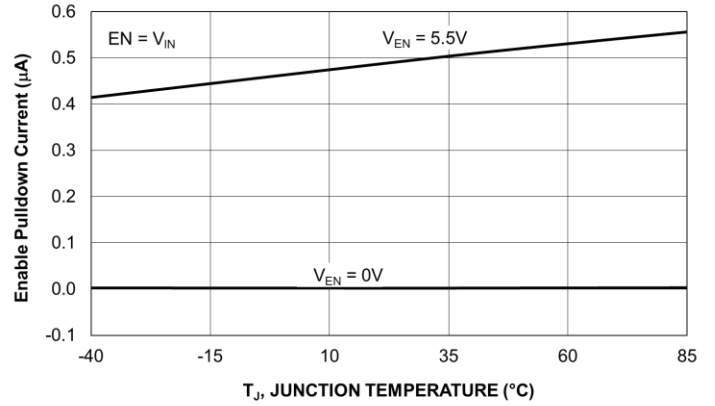
Figure 16. Pulldown Resistance vs. Temperature
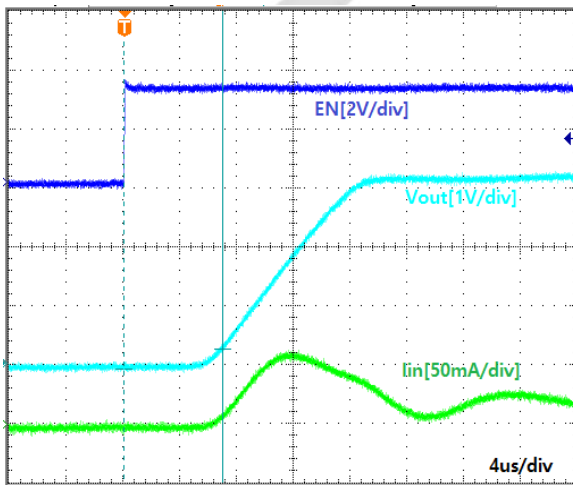

Figure 17. Enable Pulldown Current vs. Temperature

Figure 18. Turn-On Response
V$_{IN}$=3.3 V, C$_{IN}$=1.0 uF, C$_{OUT}$=0.1 uF, R$_L$=150 Ω
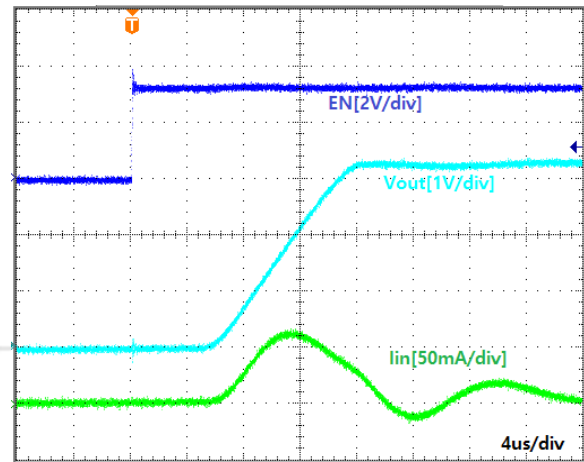
Figure 19. Turn-On Response
V$_{IN}$=3.3 V, C$_{IN}$=1.0 uF, C$_{OUT}$=0.1 uF, R$_L$=500 Ω
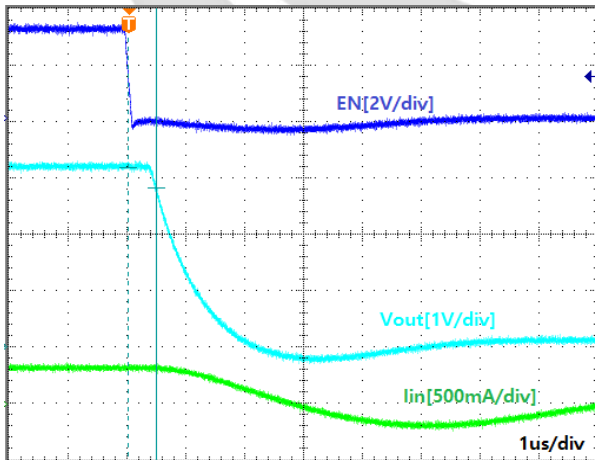
Figure 20. Turn-Off Response, Output Discharge
V$_{IN}$=3.3 V, C$_{IN}$=1.0 uF, C$_{OUT}$=0.1 uF, R$_L$=10 Ω
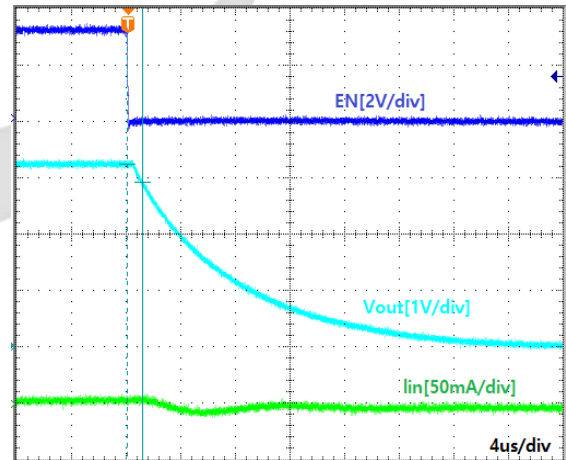
Figure 21. Turn-Off Response, Output Discharge
V$_{IN}$=3.3 V, C$_{IN}$=1.0 uF, C$_{OUT}$=0.1 uF, R$_L$=500 Ω

APPLICATION INFORMATION

The GLF71307 is an integrated 2.0 A, Ultra-Efficient I_QSmart™ LoadSwitch device with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.77 mm x 0.77 mm x 0.5 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.4 mm pitch for manufacturability.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin the moment when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

EN pin

The GLF71307 can be activated by EN pin high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known "off state" when no EN signal is applied from an external controller.

Output Discharge Function

The GLF71307 has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce voltage drops, and parasitic effects during dynamic operation as well as improve the thermal performance at high load currents.

PACKAGE OUTLINE
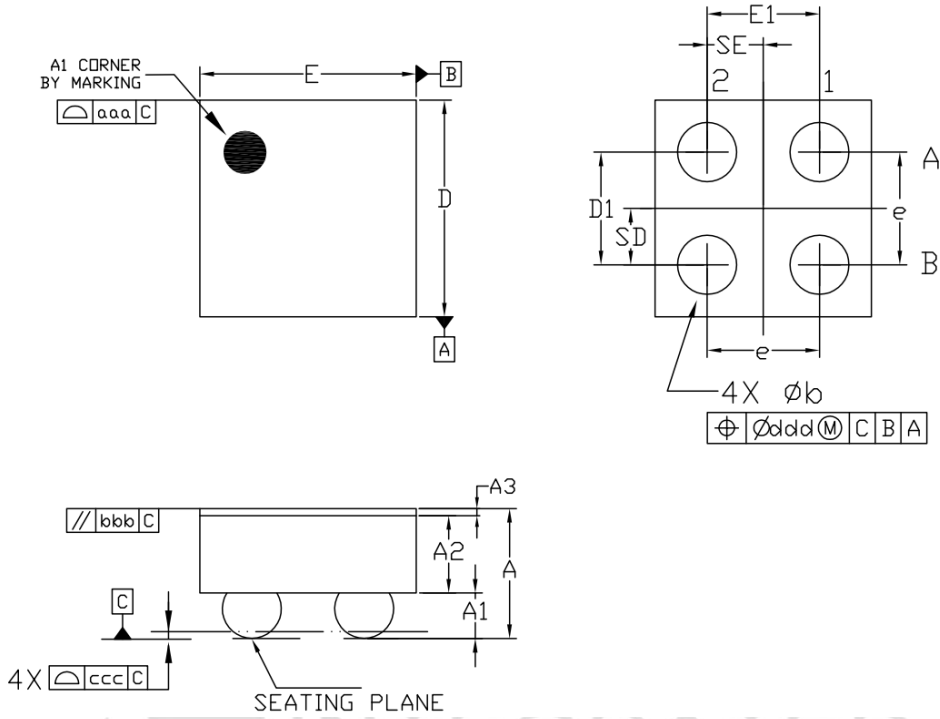
| Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.410	0.460	0.510
A1	0.135	0.160	0.185
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	0.755	0.770	0.785
E	0.755	0.770	0.785
D1	0.350	0.400	0.450
E1	0.350	0.400	0.450
b	0.170	0.210	0.250
e	0.400 BSC		
SD	0.200 BSC		
SE	0.200 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)

2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

3. A3: BACKSIDE LAMINATION
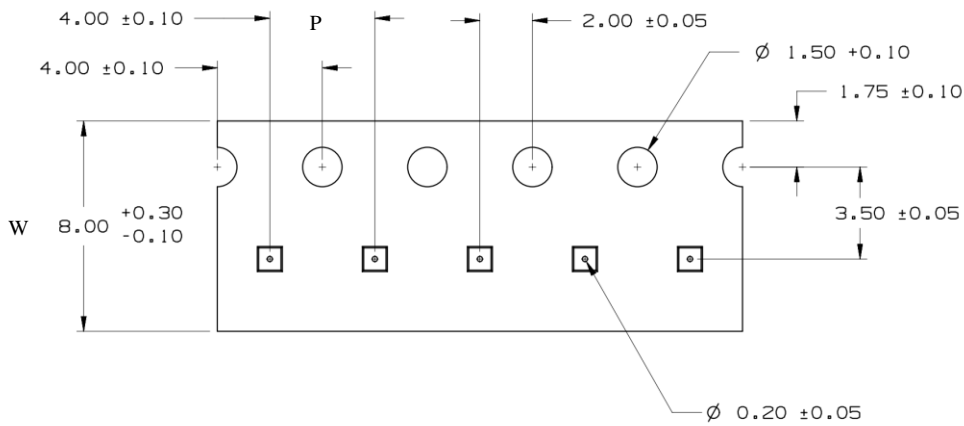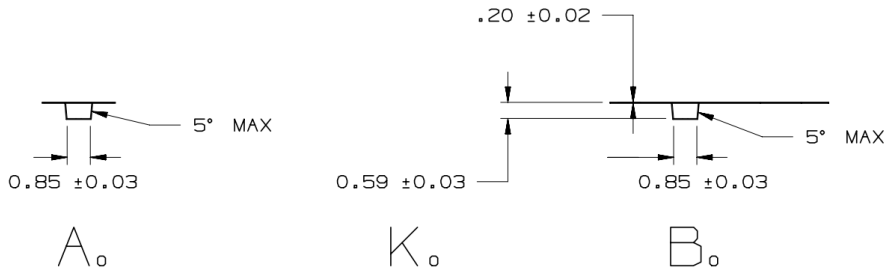
TAPE AND REEL INFORMATION

REEL DIMENSIONS
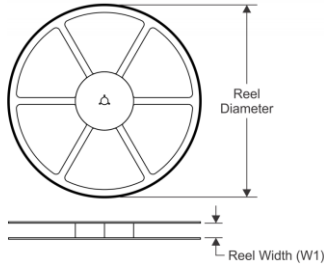
QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE
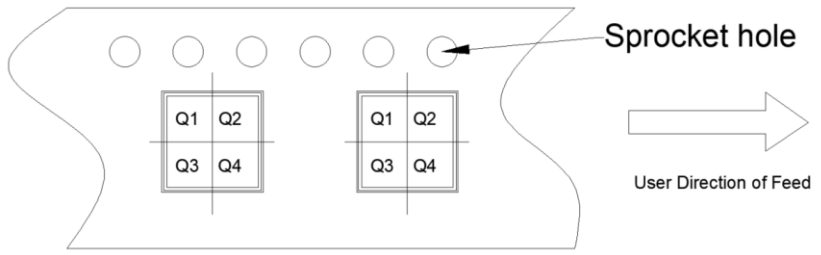
TAPE DIMENSIONS

Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF71307	WLCSP	4	4000	180	9	0.85	0.85	0.59	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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