GLF71325

Low R_{ON} I_QSmart™ Power Switch with Slew Rate Control

Product Specification

DESCRIPTION

The GLF71325 is an ultra-efficiency, 4 A rated, integrated load switch with integrated slew rate control. The best in class efficiency makes it an ideal choice for use in lower power subsystems and mobile electronics.

The GLF71325 features an ultra-efficient I_QSmart™ technology that supports the lowest R_{ON}, quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low R_{ON} reduces conduction losses, while low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF71325 integrated slew rate control greatly enhances system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF71325 slew rate control specifically limits inrush currents during turn-on to minimize voltage droop.

The GLF71325 can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

The GLF71325 offers best in class size and resistance performance utilizing a wafer level chip scale packaging with 6 bumps in a 0.97 mm x 1.47 mm x 0.55 mm die size and a 0.5 mm pitch.

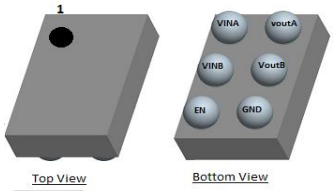
FEATURES

- Wide Input Range: 1.1 V to 5.5 V
  6 V_{abs} max
- Controlled Rise Time: 2.2 ms at $3.3V_{IN}$
- Low R_{ON}: 18 mΩ Typ at $3.3V_{IN}$
- Ultra-Low I_Q: 1 nA Typ at $3.3V_{IN}$
- Ultra-Low I_{SD}: 16 nA Typ at $3.3V_{IN}$
- I_{OUT} Max: 4 A at $5.5V_{IN}$
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- Wide Operating Temperature Range:
  -40 °C ~ 105 °C
- HBM: 6 kV, CDM: 2 kV
- Package: 0.97 mm x 1.47 mm WLCSP

APPLICATIONS

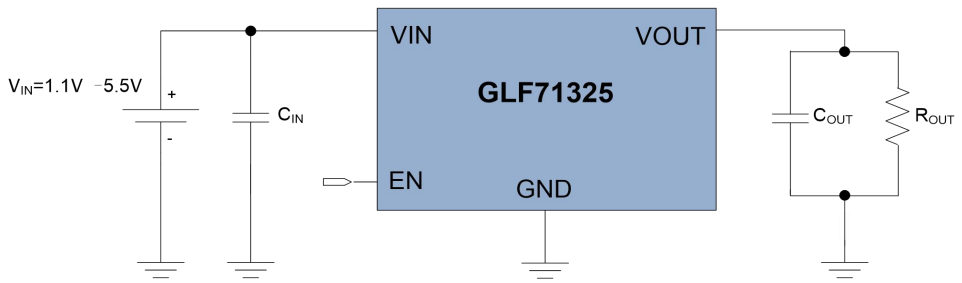
- Low Power Subsystems
- Data Storage, SSD
- Mobile Devices

PACKAGE



0.97 mm x 1.47 mm x 0.55 mm
0.5 mm pitch WLCSP

APPLICATION DIAGRAM



ORDERING INFORMATION

Part Number	Top Mark	R_{ON} (Typ) at 3.3 V	Output Discharge	EN Activity
GLF71325	HL	18 mΩ	80 Ω	High

FUNCTIONAL BLOCK DIAGRAM

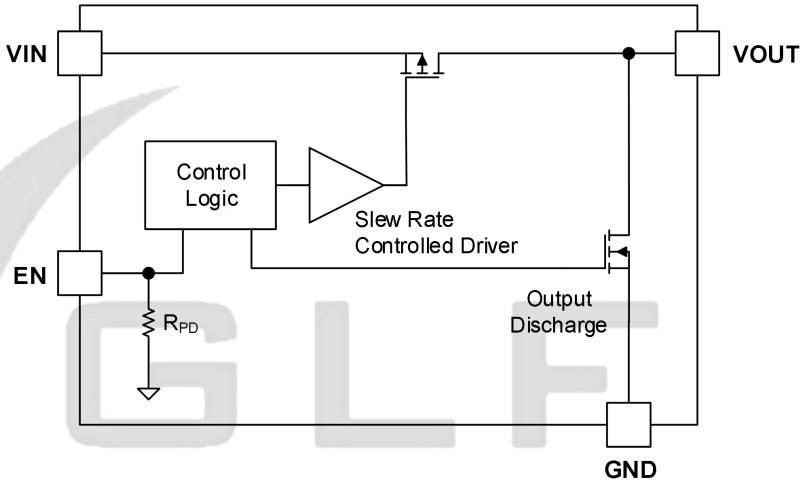


Figure 1. Functional Block Diagram

PIN CONFIGURATION

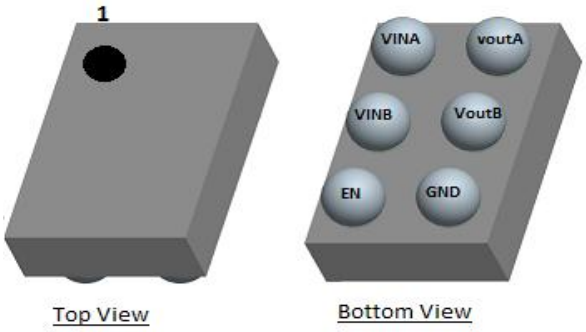


Figure 2. 0.97 mm x 1.47 mm x 0.55 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1, B1	V_{OUT}	Switch Output
A2, B2	V_{IN}	Switch Input. Supply Voltage for IC
C1	GND	Ground
C2	EN	Enable to control the switch

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			4	A
P_D	Power Dissipation at T_A = 25°C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	105	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.1	5.5	V
T_A	Ambient Operating Temperature	-40	105	°C

ELECTRICAL CHRACTERISTICS

V_{IN} = 1.1 V to 5.5 V, typical values are at V_{IN} = 3.3 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
V_{IN}	Supply Voltage			1.1		5.5	V
I_Q	Quiescent Current	EN = Enable, I_{OUT}=0 mA, V_{IN} = V_{EN} =3.3 V			1		nA
		EN=Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=3.3 V, Ta=85 °C (4)			7		
		EN=Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=3.3 V, Ta=105 °C (4)			30		
		EN = Enable, I_{OUT}=0 mA, V_{IN} = V_{EN} =5.5 V			3		
		EN=Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=5.5V, Ta=85 °C (4)			10		
		EN=Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=5.5V, Ta=105 °C (4)			40		
I_{SD}	Shutdown Current	EN = Disable, I_{OUT}=0 mA, V_{IN}=1.1 V			9		nA
		EN = Disable, I_{OUT}=0 mA, V_{IN}=1.8 V			11		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=3.3 V			16	25	
		EN = Disable, I_{OUT}=0 mA, V_{IN}=3.3 V, Ta=85 °C (4)			1.1		μA
		EN = Disable, I_{OUT}=0 mA, V_{IN}=3.3 V, Ta=105 °C (4)			4		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=4.5 V			30		nA
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V			50	100	
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=55 °C (4)			250		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=85 °C (4)			1.7		μA
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=105 °C (4)			5.5		
R_{ON}	On-Resistance	V_{IN}=5.5 V I_{OUT}= 500 mA	Ta = 25 °C		15	17	mΩ
			Ta = 85 °C		17		
			Ta = 105 °C		18		
		V_{IN}=3.3 V, I_{OUT}= 500 mA	Ta = 25°C		18	21	
			Ta = 85 °C		21		
			Ta = 105 °C		22		
		I_{OUT}= 300 mA	V_{IN}=1.8 V		28		
		I_{OUT}= 100 mA	V_{IN}=1.1 V		55		
R_{DSC}	Output Discharge Resistance	E_N=Low , I_{FORCE}= 10 mA			80	100	Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}=1.1-1.8 V		0.9			V
		V_{IN}=1.8-5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN}=1.1-1.8 V				0.3	V
		V_{IN}=1.8-5.5 V				0.4	V
R_{EN}	EN pull down resistance	E_N=5.5 V		7	10.1	13	MΩ
I_{EN}	EN Current					0.8	μA
Switching Characteristics							
t_{dON}	Turn-On Delay(1)	R_{OUT}=150 Ω, C_{OUT}=1.0 μF			1.5		ms
t_R	V_{OUT} Rise Time(1)				2.2		ms
t_{dOFF}	Turn-Off Delay(2, 3, 4)	R_{OUT}=150 Ω, C_{OUT}=1.0 μF			9		μs
t_F	V_{OUT} Fall Time(2, 3, 4)				117		μs

Notes: 1. $t_{ON} = t_{dON} + t_R$
2. $t_{OFF} = t_{dOFF} + t_F$
3. Output discharge path is enabled during off.
4. By design; characterized; not production tested.

TIMING DIAGRAM

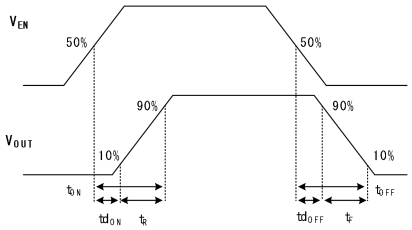


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

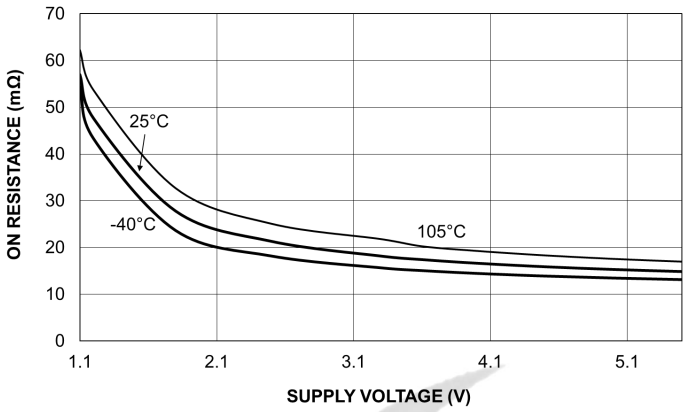


Figure 4. On-Resistance vs. Input Voltage

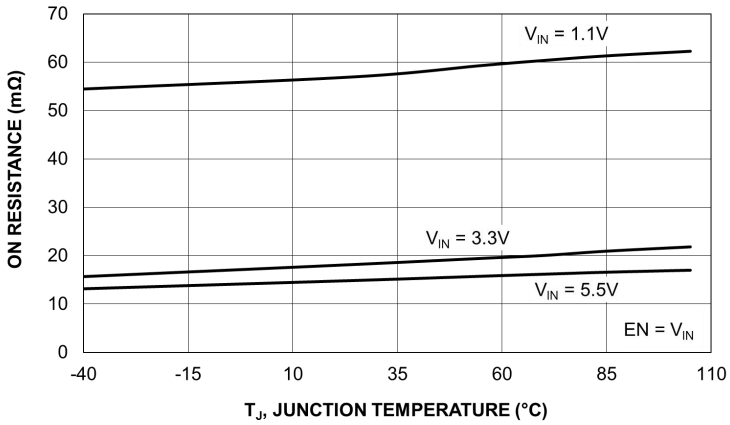


Figure 5. On-Resistance vs. Temperature

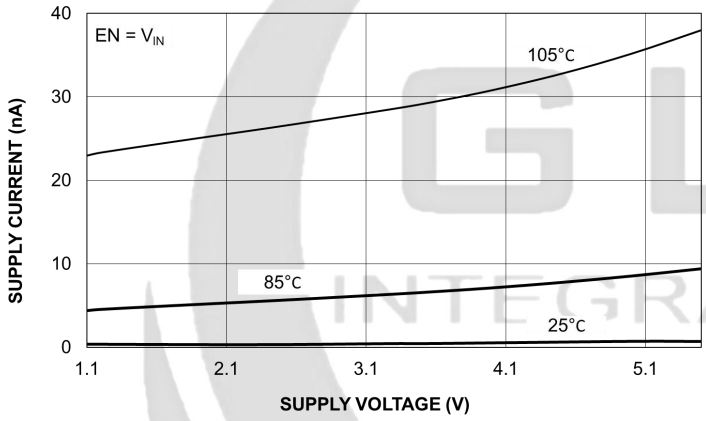


Figure 6. Quiescent Current vs. Input Voltage

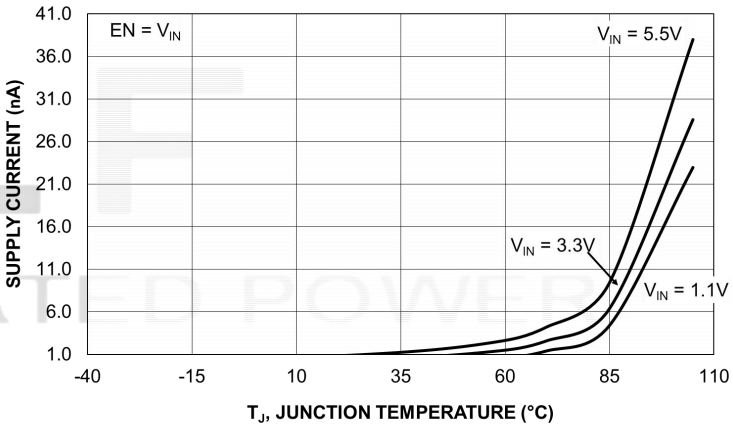


Figure 7. Quiescent Current vs. Temperature

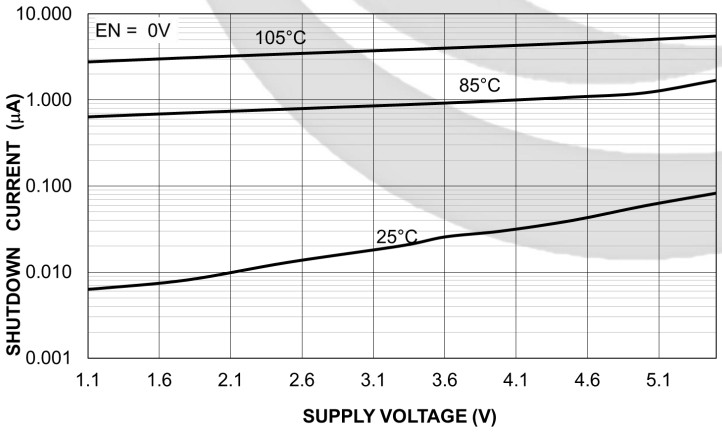


Figure 8. Shutdown Current vs. Input Voltage

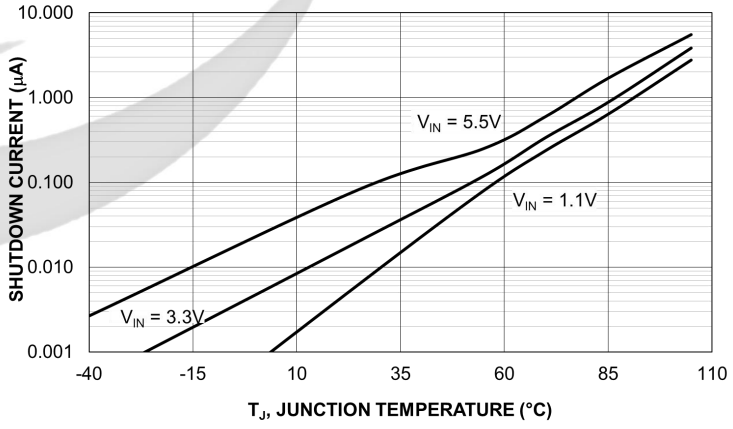


Figure 9. Shutdown Current vs. Temperature

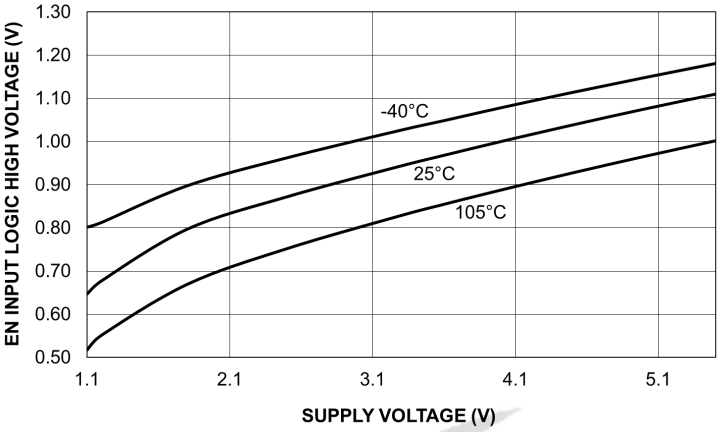


Figure 10. EN Input Logic High Threshold

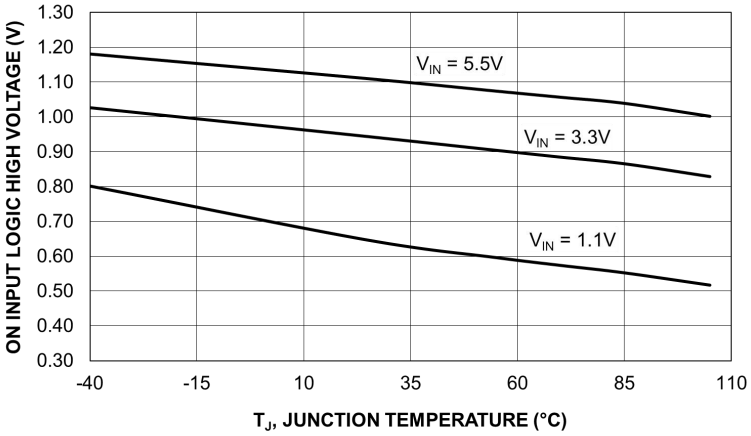


Figure 11. EN Input Logic High Threshold Vs. Temperature

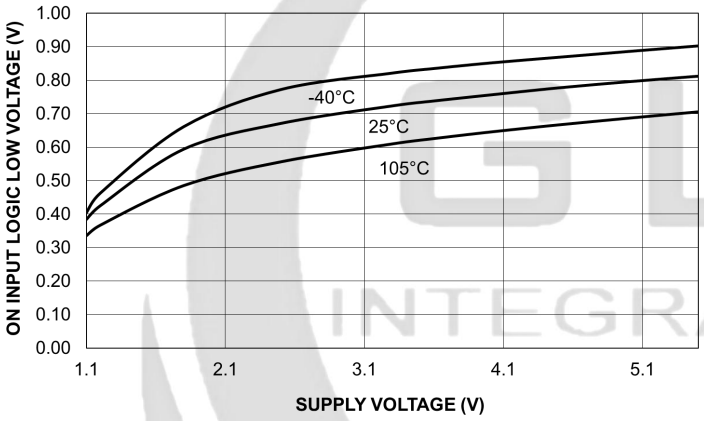


Figure 12. EN Input Logic Low Threshold

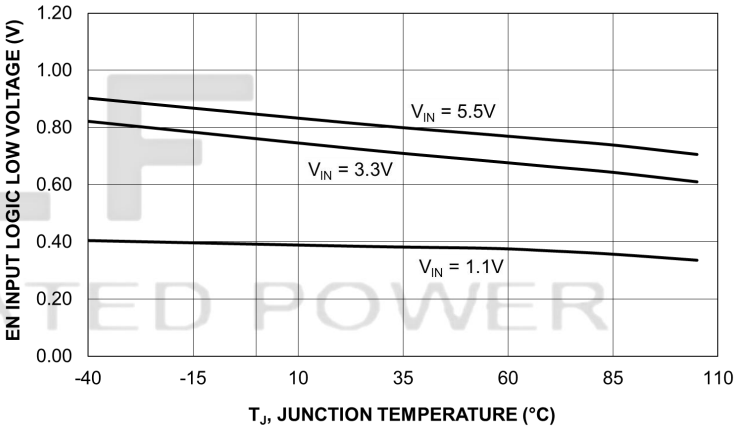


Figure 13. EN Input Logic Low Threshold Vs. Temperature

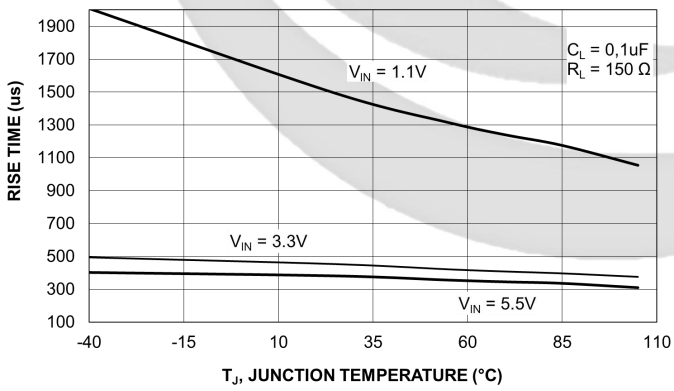


Figure 14. V_{OUT} Rise Time vs. Temperature

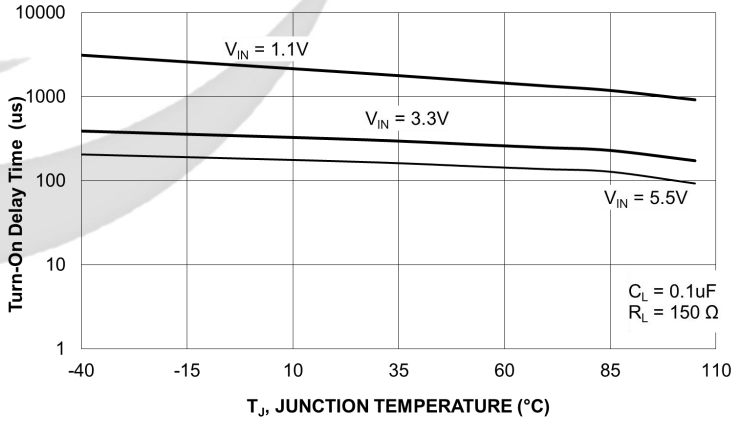


Figure 15. Turn-On Delay Time vs. Temperature

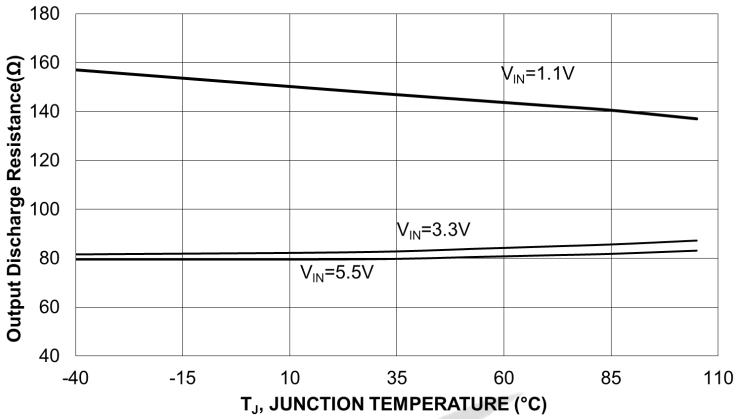


Figure 16. Output Discharge Resistance vs. Temperature

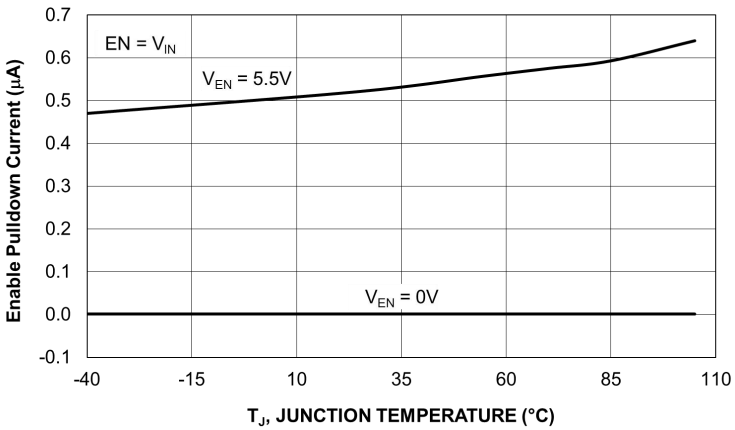


Figure 17. Enable Pulldown Current vs. Temperature

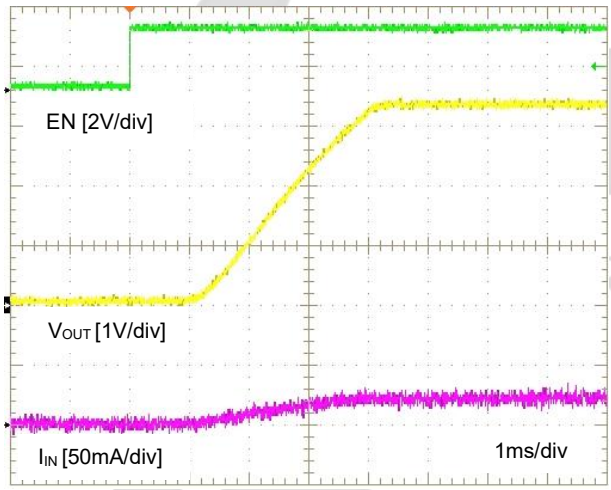


Figure 18. Turn-On Response
V_{IN}=3.3 V, C_{OUT}=1.0 µF, R_L=150 Ω

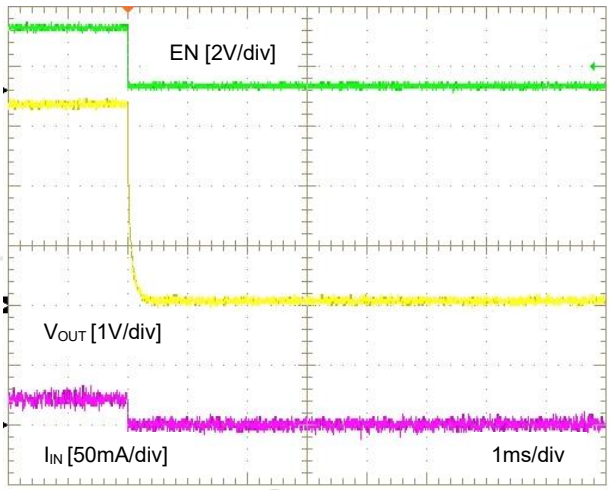


Figure 19. Turn-Off Response
V_{IN}=3.3 V, C_{OUT}=1.0 µF, R_L=150 Ω

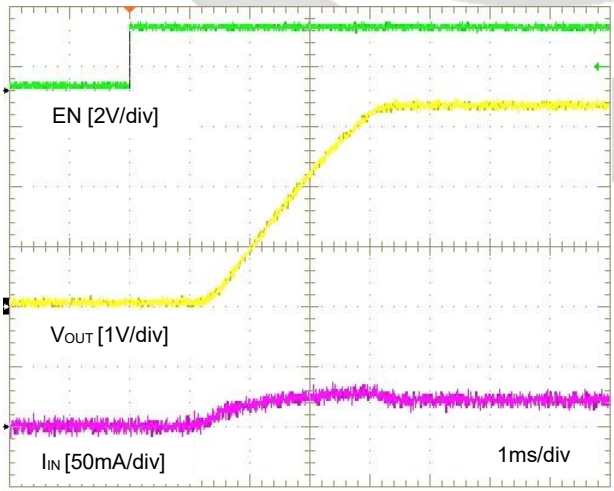


Figure 20. Turn-On Response
V_{IN}=3.3 V, C_{OUT}=10 µF, R_L=150 Ω

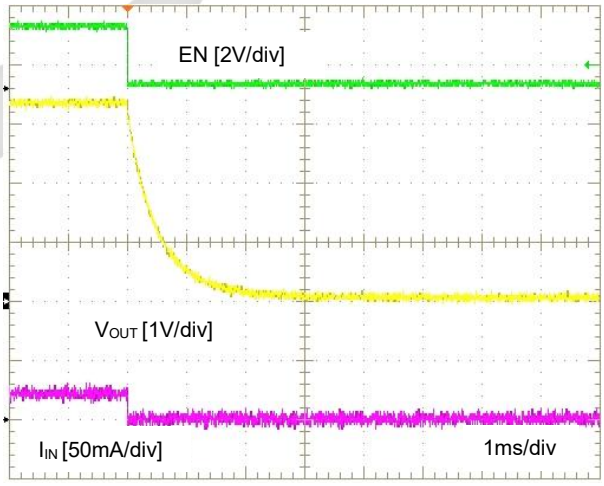


Figure 21. Turn-Off Response
V_{IN}=3.3 V, C_{OUT}=10 µF, R_L=150 Ω

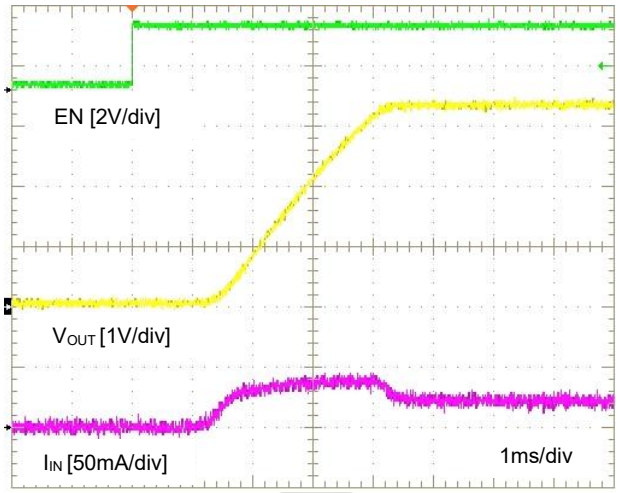


Figure 22. Turn-On Response
V_{IN}=3.3 V, C_{OUT}=22 µF, R_L=150 Ω

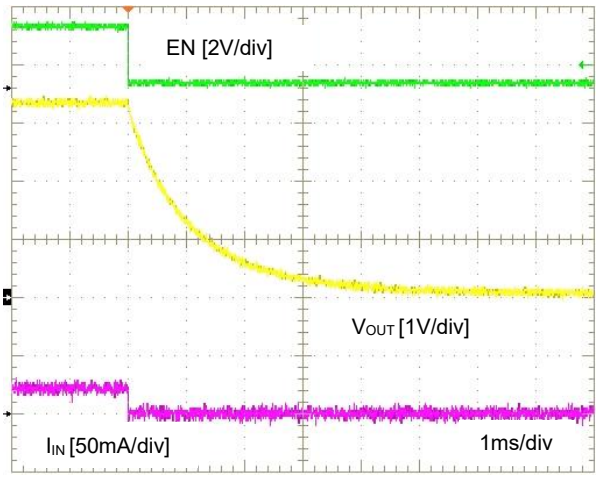


Figure 23. Turn-Off Response
V_{IN}=3.3 V, C_{OUT}=22 µF, R_L=150 Ω

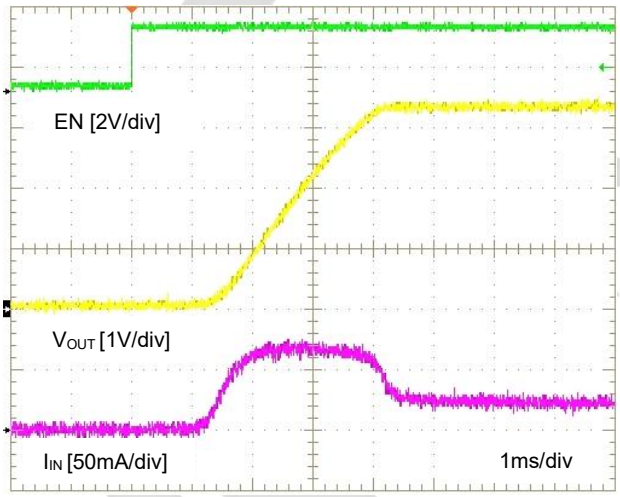


Figure 24. Turn-On Response
V_{IN}=3.3 V, C_{OUT}=47 µF, R_L=150 Ω

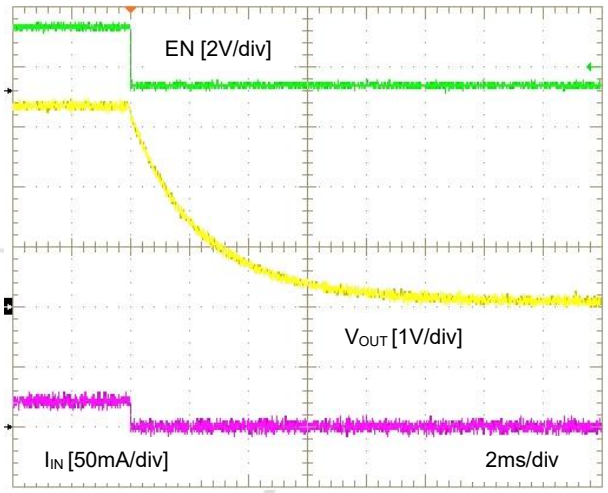


Figure 25. Turn-Off Response
V_{IN}=3.3 V, C_{OUT}=47 µF, R_L=150 Ω

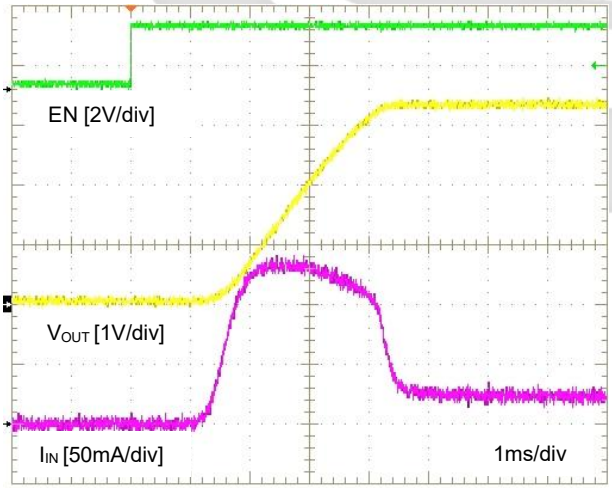


Figure 26. Turn-On Response
V_{IN}=3.3 V, C_{OUT}=100 µF, R_L=150 Ω

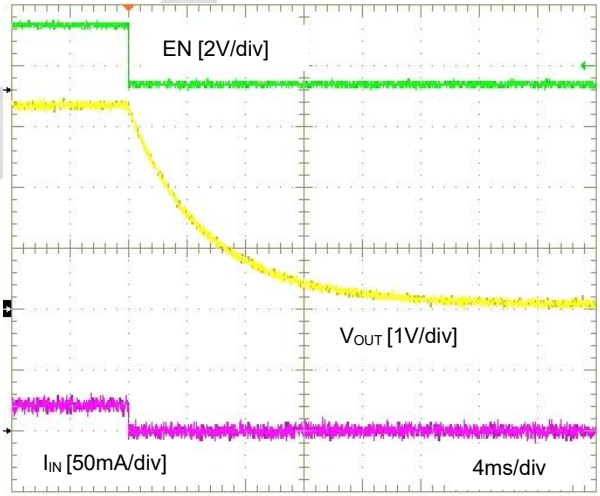


Figure 27. Turn-On Response
V_{IN}=3.3 V, C_{OUT}=100 µF, R_L=150 Ω

APPLICATION INFORMATION

The GLF71325 is an integrated 4 A, Ultra-efficient I_QSmart™ load switch device with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.97 mm x 1.47 mm x 0.55 mm wafer level chip scale package, saving space in compact applications. It is constructed using 6 bumps, with a 0.5 mm pitch for reliable manufacturability.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin the moment when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

EN pin

The GLF71325 can be activated by EN pin high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

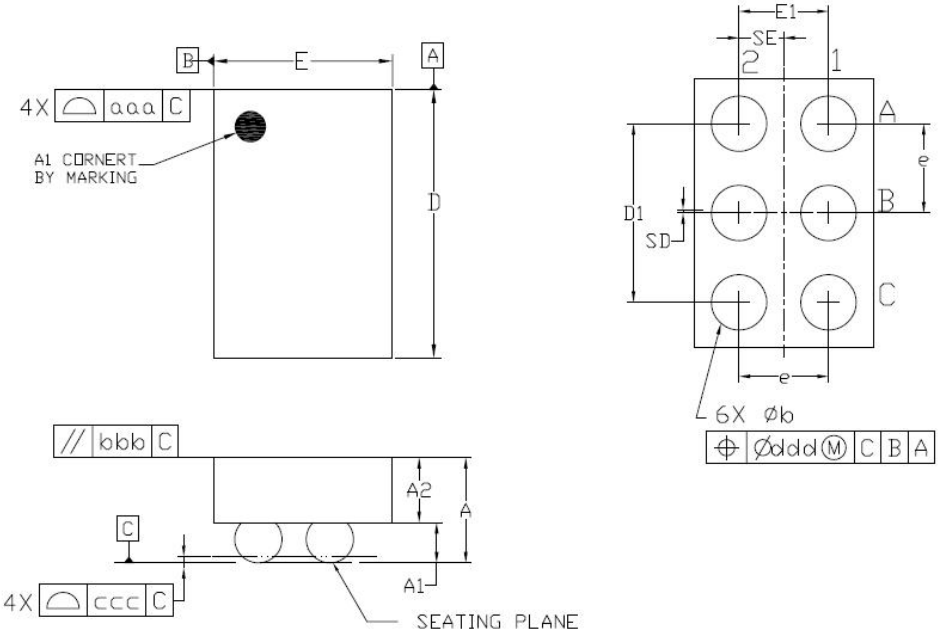
Output Discharge Function

The GLF71325 has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

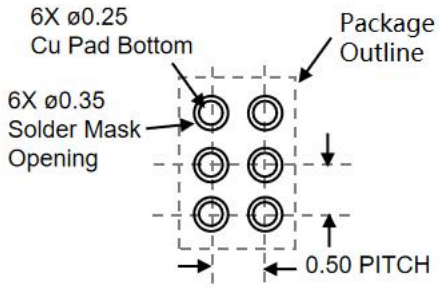
All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce voltage drops, and parasitic effects during dynamic operation as well as improve the thermal performance at high load currents.

PACKAGE OUTLINE



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.275	0.300	0.325
D	1.460	1.470	1.485
E	0.960	0.970	0.985
D1	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.000 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint

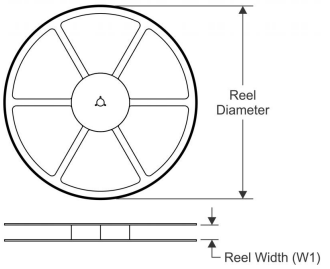


Notes

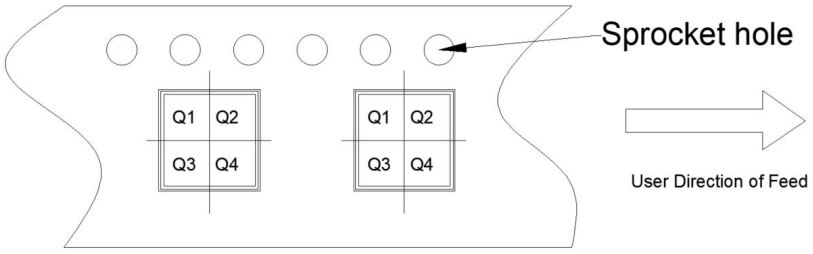
1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

TAPE AND REEL INFORMATION

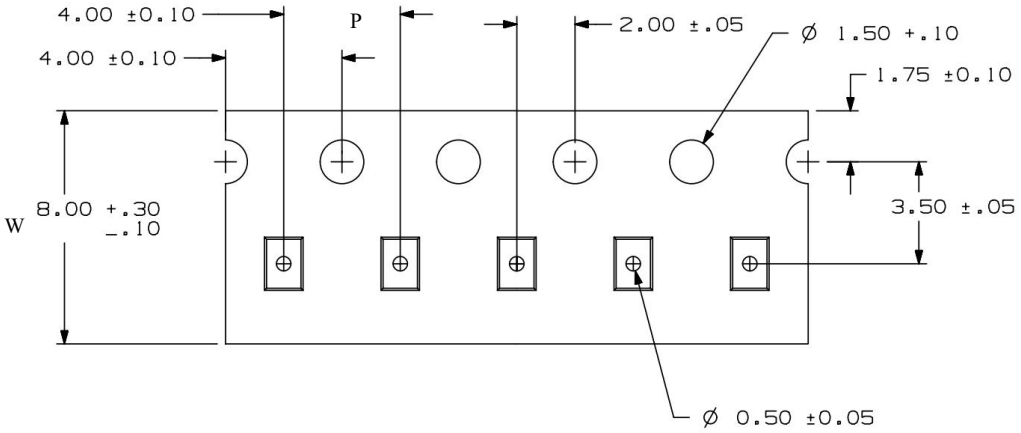
REEL DIMENSIONS

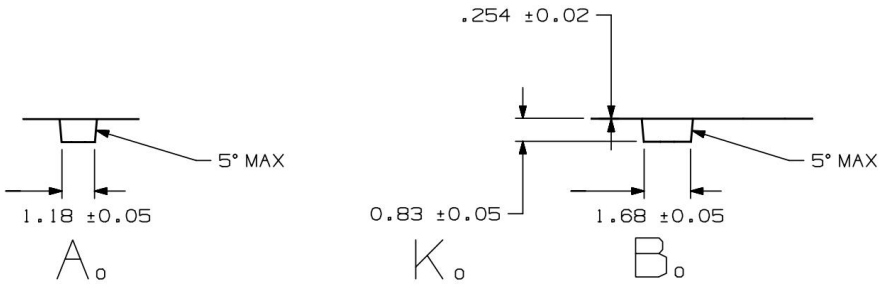


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF71325	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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