GLF78131, GLF78131T

3-Channel I_QSmart™ LoadSwitch

Product Specification

DESCRIPTION

The GLF78131 / GLF78131T is an ultra-efficienct, I_QSmart™ LoadSwitch with three independent and identical load switches integrated. Each load switch features an ultra-efficient I_QSmart™ technology that supports some of the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF78131 / GLF78131T integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush current that result in voltage droop and/or bus reset events, the slew rate control specifically limits inrush current during turn-on to minimize voltage droop.

The GLF78131 / GLF78131T Load Switch device supports an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

The GLF78131 / GLF78131T is utilizing a wafer level chip scale package with 12 bumps in a 1.27 mm x 1.67 mm die size and a 0.4 mm bump pitch. The GLF78131T is ultra-thin. Its thickness is 0.35 mm Typ, 0.4 mm Max.

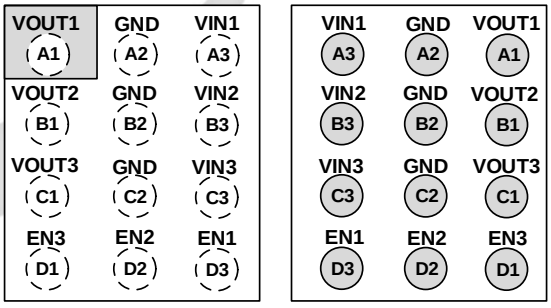
FEATURES

- Each Channel is identical
- Ultra-Low I_Q: 6 nA Typ @ 5.5 V_{IN}
- Ultra-Low I_{SD}: 23 nA Typ @ 5.5 V_{IN}
- Low R_{ON} = 60 mΩ Typ @ 5.5 V_{IN}
- I_{OUT} Max = 1.5 A
- Supply Voltage Range: 1.1 V to 5.5 V
  6 V abs max
- Controlled Rise Time: 500 µs at 3.3 V_{IN}
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- Temperature Range: -40 to 85 °C
- HBM: 6 kV, CDM: 2 kV

APPLICATIONS

- Low Power Subsystems
- Thin Mobile Devices & Wearables
- IoT Devices

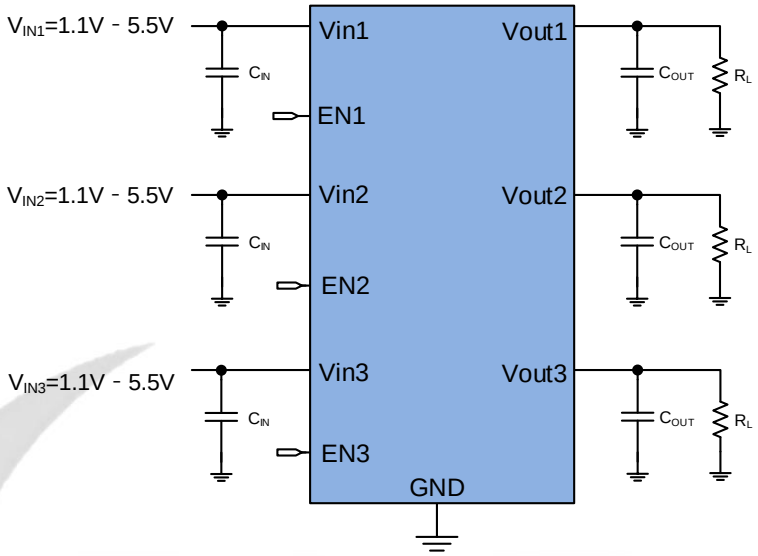
PACKAGE



TOP VIEW BOTTOM VIEW

GLF78131 : 1.27 mm x 1.67 mm x 0.55 mm
GLF78131T : 1.27 mm x 1.67 mm x 0.35 mm

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V	Output Discharge(Typ)	EN Activity	Package Thickness	Availability
GLF78131	TA	60 mΩ	225 Ω	High	T=0.55 mm	Release
GLF78131T	AP	60 mΩ	225 Ω	High	T=0.35 mm	On Request

FUNCTIONAL BLOCK DIAGRAM (Each Channel is identical)

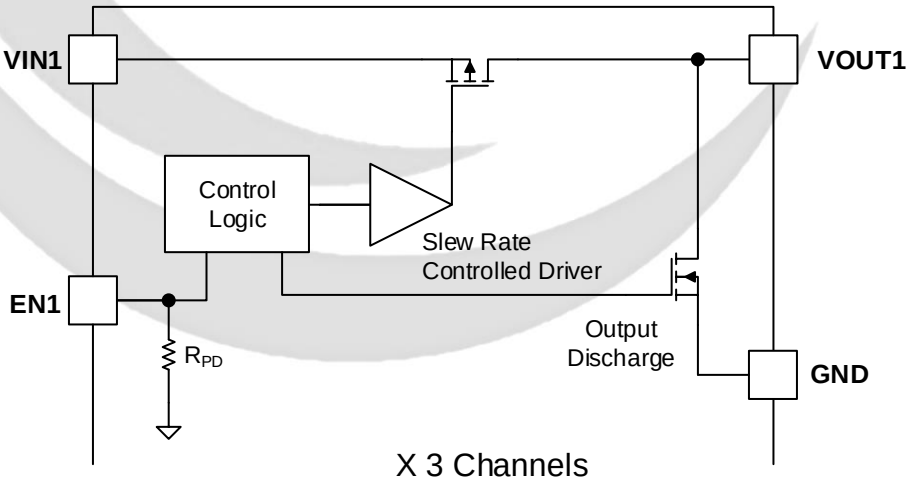
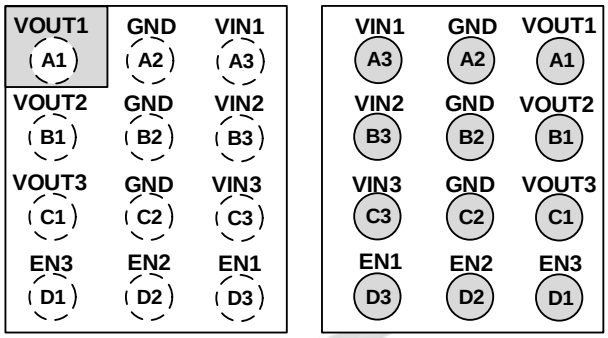


Figure 1. Functional Block Diagram of Single Channel

PIN CONFIGURATION



TOP VIEW BOTTOM VIEW

Figure 2. 1.27 mm x 1.67 mm x 0.5 mm WLCSP

1.27 mm x 1.67 mm x 0.35 mm Ultra-Thin WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	VOUT1	Switch Output
A2	GND	Ground
A3	VIN1	Switch Input
B1	VOUT2	Switch Output
B2	GND	Ground
B3	VIN2	Switch Input
C1	VOUT3	Switch Output
C2	GND	Ground
C3	VIN3	Switch Input
D1	EN3	Enable to control the switch. There is an internal pull-down resistor.
D2	EN2	Enable to control the switch. There is an internal pull-down resistor.
D3	EN1	Enable to control the switch. There is an internal pull-down resistor.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN} Pins, V_{OUT} Pins, EN	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			1.5	A
P_D	Power Dissipation at T_A = 25°C			TBD	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (1 in^2 pad of 2 oz. copper using 2S2P PCB)			84	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.1	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS OF SINGLE CHANNEL (Each Channel is identical)

Values are at V_{IN} = 3.3 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
V_{IN}	Supply Voltage			1.1		5.5	V
I_Q	Quiescent Current	EN = Enable, I_{OUT} = 0 mA, V_{IN} = V_{EN} = 5.5 V			6	20	nA
		EN = Enable, I_{OUT} = 0mA, V_{IN} = V_{EN} = 5.5 V, Ta = 85 °C (4)			12		
I_{SD}	Shut Down Current	EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.1 V			3		nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.8 V			4		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.3 V			6		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 4.5 V			11		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 5.5 V			23	50	
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 5.5 V, Ta = 55 °C (4)			100		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 5.5 V, Ta = 85 °C (4)			530		
R_{ON}	On-Resistance	V_{IN} = 5.5 V, I_{OUT} = 500 mA	Ta = 25 °C		60	70	mΩ
			Ta = 85 °C (4)		75		
		V_{IN} = 3.3 V, I_{OUT} = 500 mA	Ta = 25 °C		70	80	
			Ta = 85 °C (4)		85		
		V_{IN} = 1.8 V, I_{OUT} = 300 mA	Ta = 25 °C		95		
		V_{IN} = 1.2 V, I_{OUT} = 100 mA	Ta = 25 °C		150		
		V_{IN} = 1.1 V, I_{OUT} = 100 mA	Ta = 25 °C		165		
R_{DSC}	Output Discharge Resistance	E_N = Low , I_{FORCE} = 10 mA			235		Ω
V_{IH}	EN Input Logic High Voltage	V_{IN} = 1.1 V to 1.8 V		0.9			V
		V_{IN} = 1.8 V to 5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 1.1 V to 1.8 V				0.3	V
		V_{IN} = 1.8 V to 5.5 V				0.4	V
R_{EN}	EN pull down resistance	Internal Resistance		7	10.1	13	MΩ
I_{EN}	EN Current	E_N = 5.5 V				0.75	μA
Switching Characteristics							
t_{dON}	Turn-On Delay(1)	R_L = 10 Ω, C_{OUT} = 0.1 μF			320		μs
t_R	V_{OUT} Rise Time(1)				500		
t_{dOFF}	Turn-Off Delay(2,3,4)	R_L = 10 Ω, C_{OUT} = 0.1 μF			0.6		
t_F	V_{OUT} Fall Time(2,3,4)				2.1		

Notes:
1. $t_{ON} = t_{dON} + t_R$
2. $t_{OFF} = t_{dOFF} + t_F$
3. Output discharge path is enabled during off.
4. By design; characterized; not production tested.

TIMING DIAGRAM

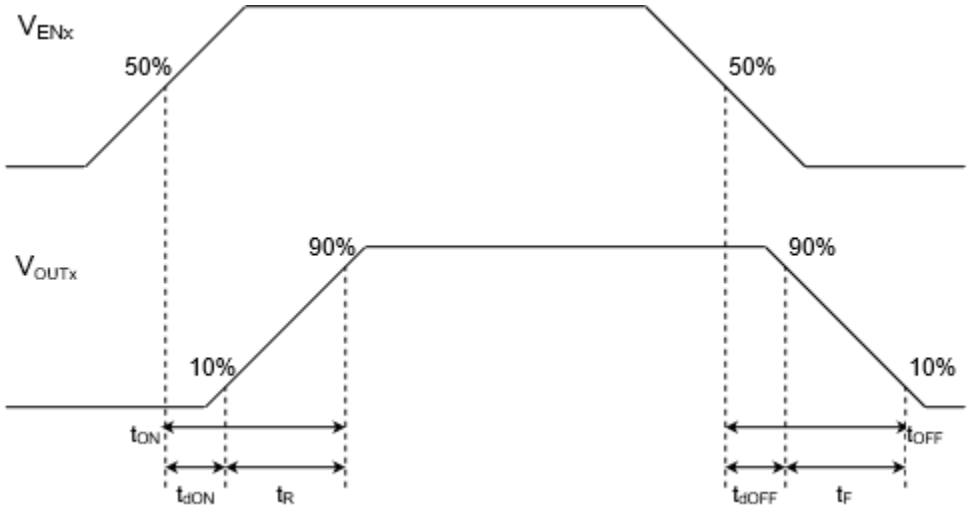


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

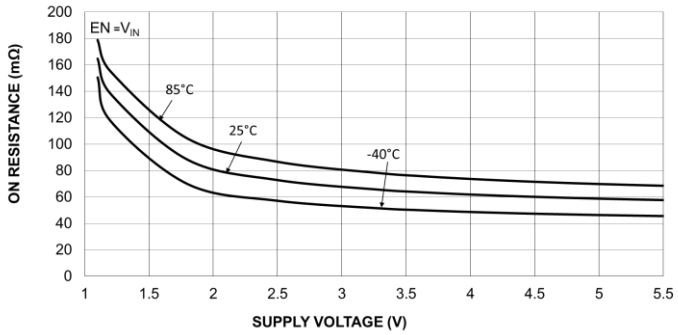


Figure 4. On-Resistance vs. Supply Voltage

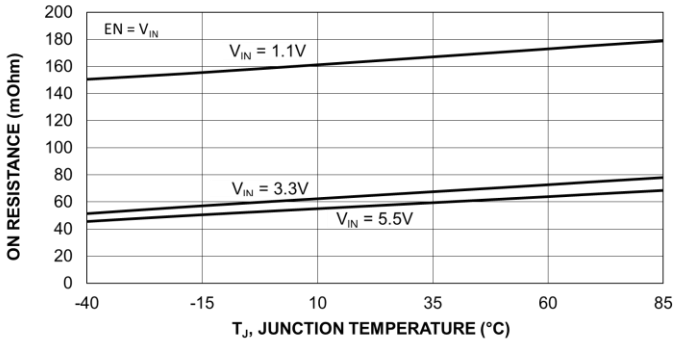


Figure 5. On-Resistance vs. Temperature

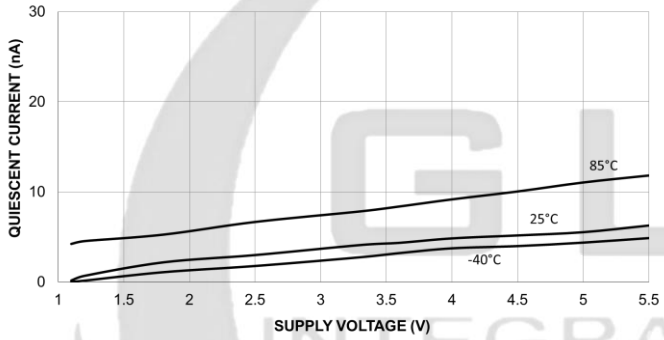


Figure 6. Quiescent Current vs. Supply Voltage

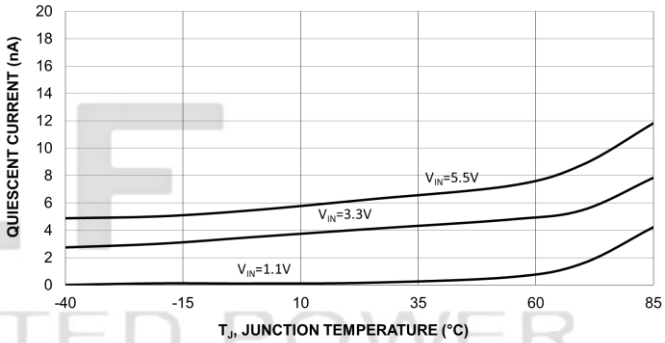


Figure 7. Quiescent Current vs. Temperature

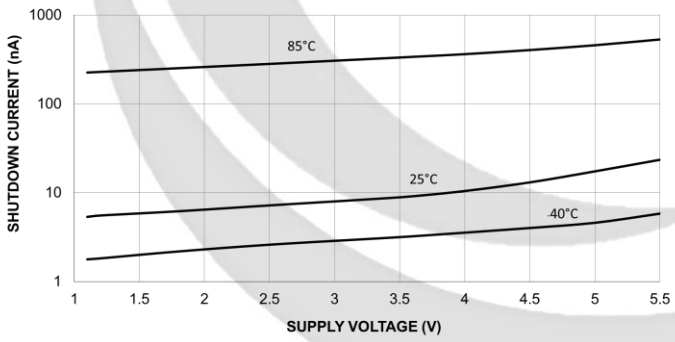


Figure 8. Shutdown Current vs. Supply Voltage

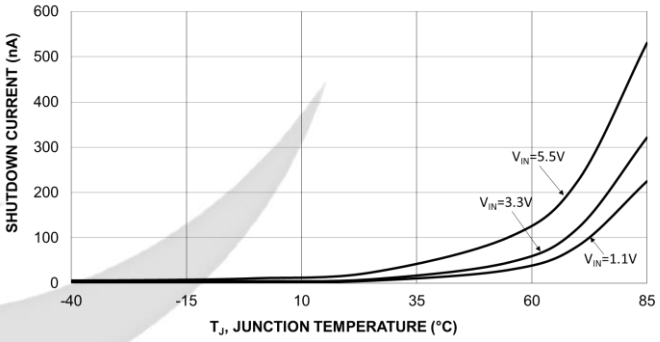


Figure 9. Shutdown Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

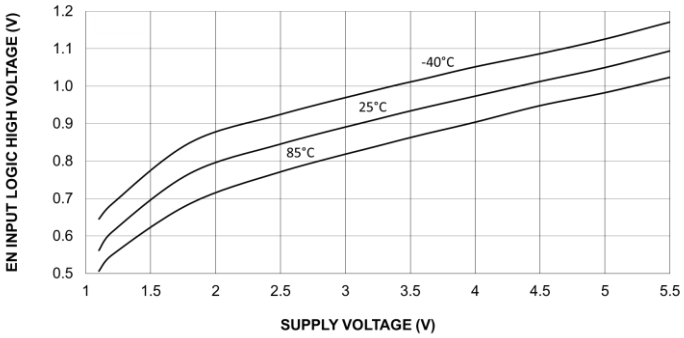


Figure 10. EN Input Logic High Threshold

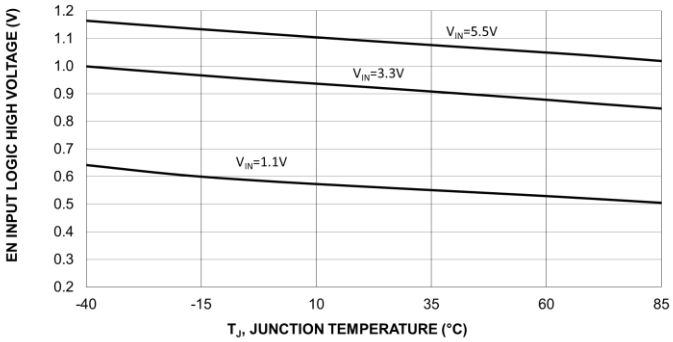


Figure 11. EN Input Logic High Threshold Vs. Temperature

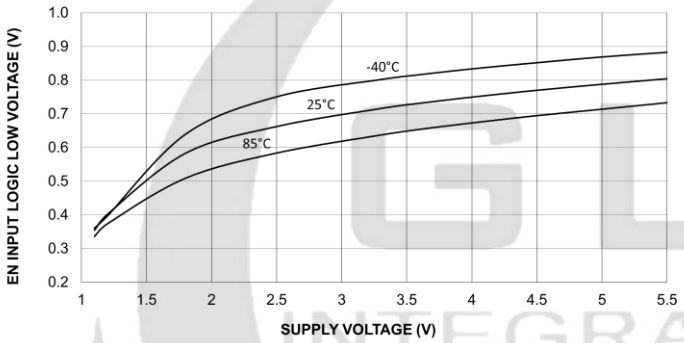


Figure 12. EN Input Logic Low Threshold

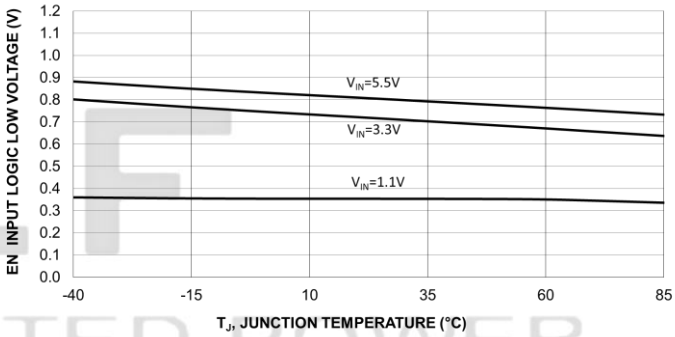


Figure 13. EN Input Logic Low Threshold Vs. Temperature

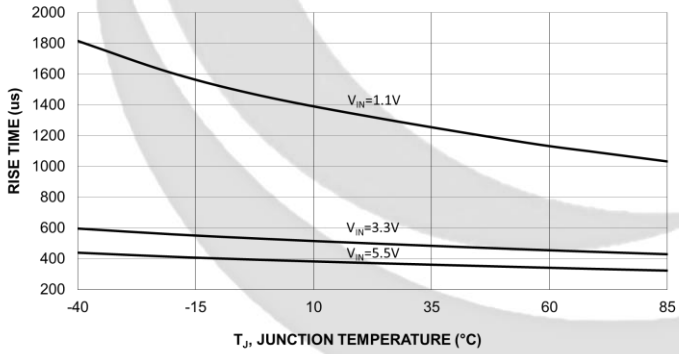


Figure 14. V_{OUT} Rise Time vs. Temperature

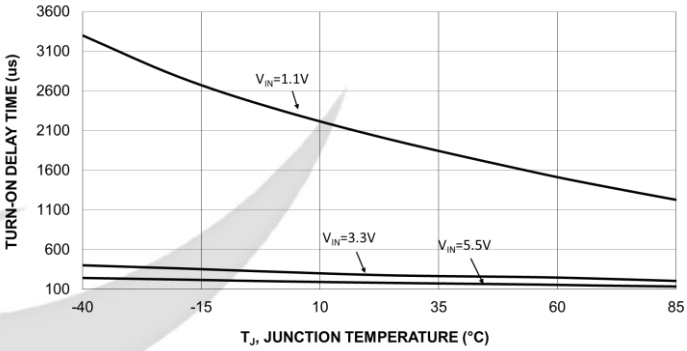


Figure 15. Turn-On Delay Time vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

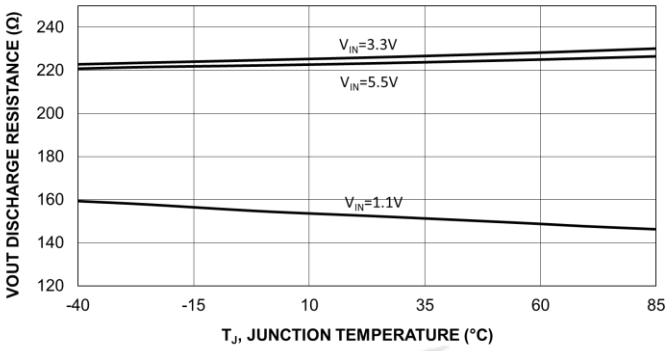


Figure 16. VOUT Discharge Resistance vs. Temperature

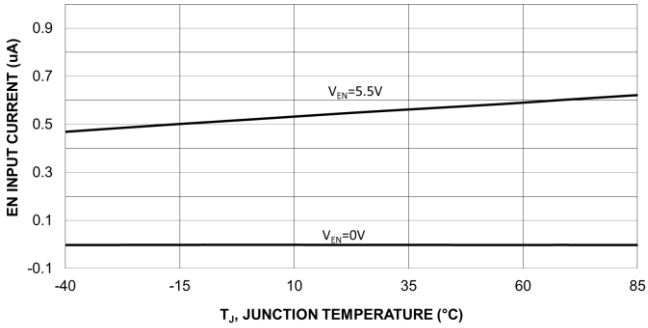


Figure 17. Enable Input Current vs. Temperature

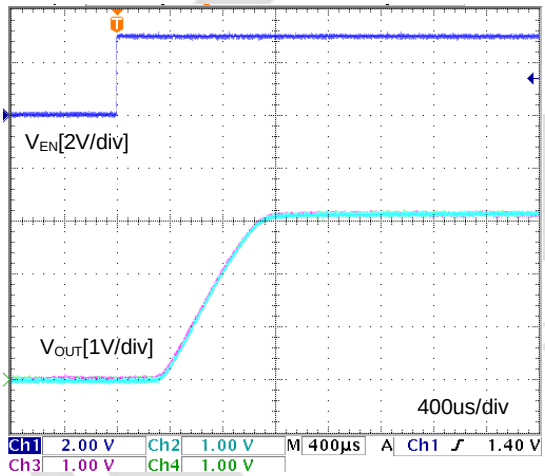


Figure 18. Turn-On Response
V_{IN} = 3.3 V, C_{IN} = C_{OUT} = 0.1 µF, R_L = 10 Ω

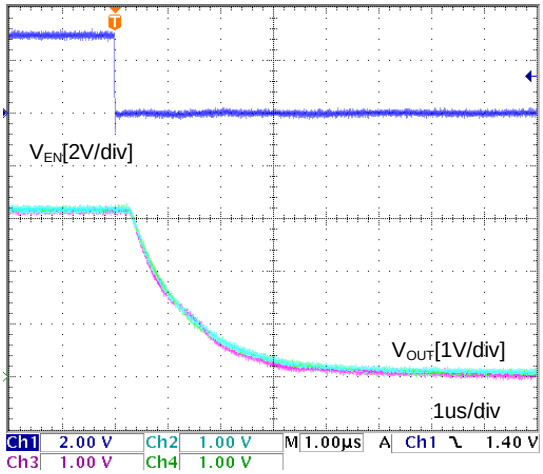


Figure 19. Turn-Off Response
V_{IN} = 3.3 V, C_{IN} = C_{OUT} = 0.1 µF, R_L = 10 Ω

APPLICATION INFORMATION

The GLF78131 / GLF78131T is an ultra-efficiency, IQSmart™ LoadSwitch with three independent and identical load switches integrated. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save input power.

Input Capacitor

A 0.1 μF capacitor is recommended to be placed close to each V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

A 0.1 μF output capacitor is recommended to mitigate voltage undershoot on the output pin the moment when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductance. If load inductance does exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

EN pin

The GLF78131 and GLF78131T can be activated by EN pin high level. Note that each EN pin has an internal pull-down resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

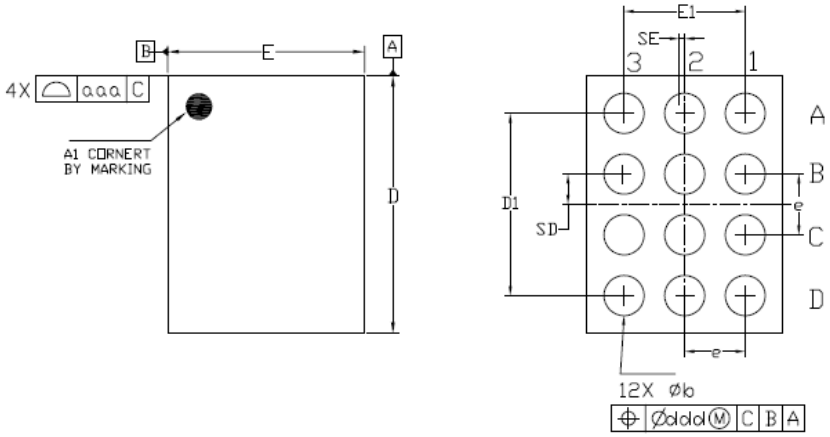
Output Discharge Function

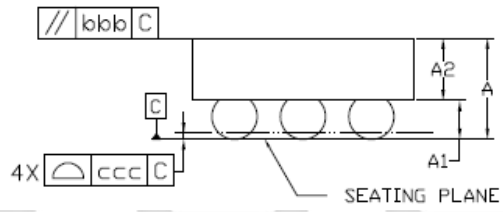
The GLF78131 and GLF78131T have an internal discharge N-channel FET switch on each VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce voltage drops and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

PACKAGE OUTLINE (GLF78131)



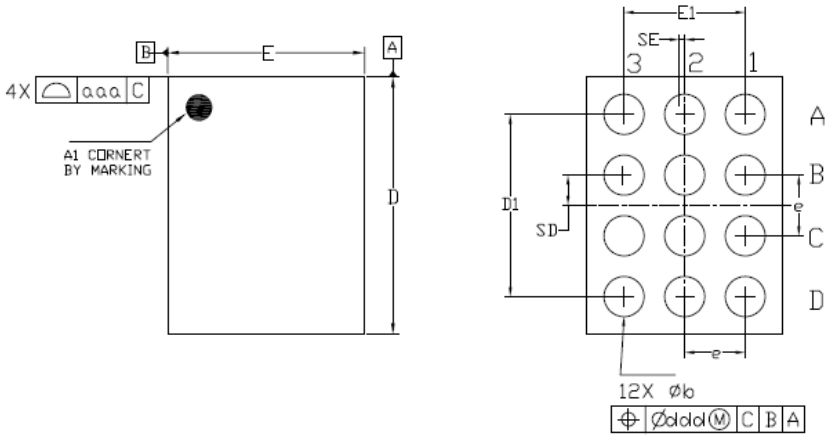


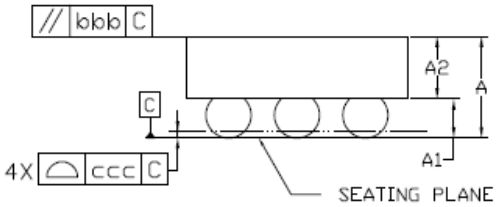
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.175	0.200	0.225
A2	0.325	0.350	0.375
D	1.655	1.670	1.685
E	1.255	1.270	1.285
D1	1.150	1.200	1.250
E1	0.750	0.800	0.850
b	0.215	0.265	0.315
e	0.400 BSC		
SD	0.200 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

PACKAGE OUTLINE (GLF78131T)





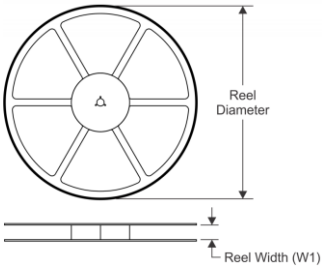
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.300	0.350	0.400
A1	0.075	0.100	0.125
A2	0.225	0.250	0.275
D	1.655	1.670	1.685
E	1.255	1.270	1.285
D1	1.150	1.200	1.250
E1	0.750	0.800	0.850
b	0.200	0.230	0.260
e	0.400 BSC		
SD	0.200 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

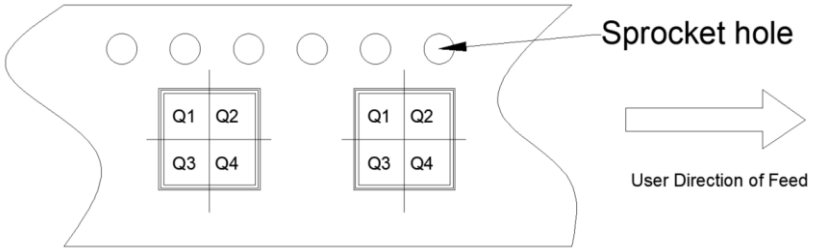
1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

TAPE AND REEL INFORMATION

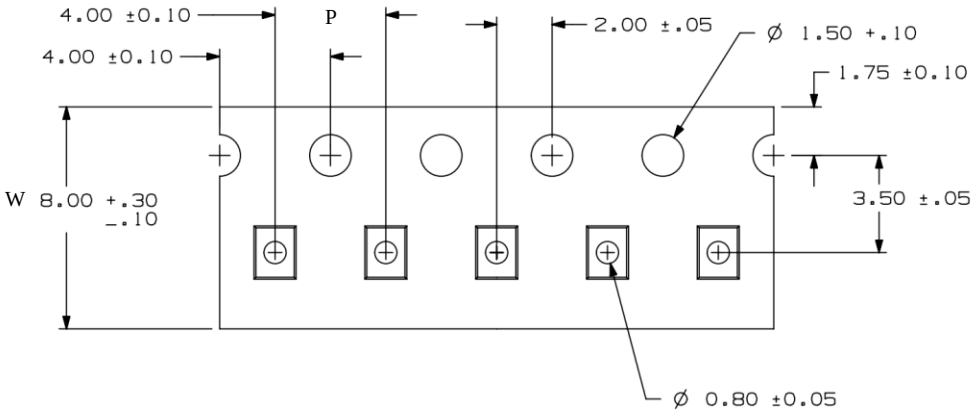
REEL DIMENSIONS

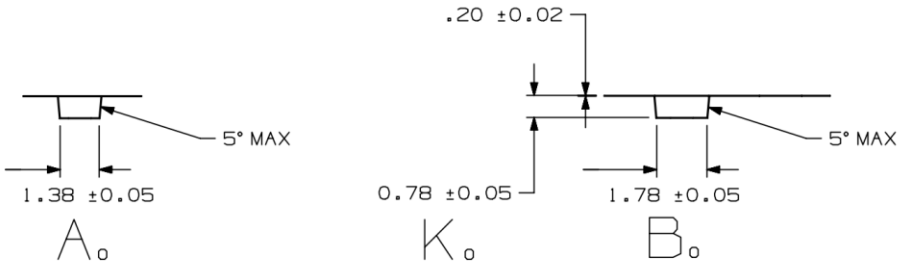


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF78131	WLCSP	12	3000	180	9	1.38	1.78	0.78	4	8	Q1
GLF78131T	WLCSP	12	3000	180	9	1.38	1.78	0.78	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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