GLF71315

Ultra-Efficient, I_QSmart™ Power Load Switch with Slew Rate Control

Product Specification

DESCRIPTION

The GLF71315 is an ultra-efficiency, 2 A rated, Load Switch with integrated slew rate control. The best in class efficiency makes it an ideal chose for use in IoT, mobile, and wearable electronics.

The GLF71315 features ultra-efficient I_QSmart™ technology that supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF71315 integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF71315 slew rate control specifically limits inrush currents during turn-on to minimize voltage droop.

GLF71315 Load Switch devices support an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduce operating cost.

GLF71315 Load Switch device is small utilizing a chip scale package with 4 bumps in a 0.97 mm x 0.97 mm x0.55 mm die size and a 0.5 mm bump pitch.

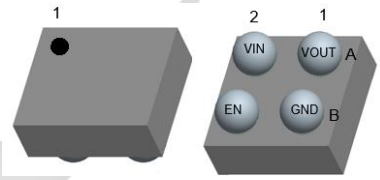
FEATURES

- Ultra-Low I_Q: 7 nA Typ at 5.5 V_{IN}
- Ultra-Low I_{SD}: 28 nA Typ at 5.5 V_{IN}
- Low R_{ON} : 31 mΩ Typ at 5.5 V_{IN}
- I_{OUT} Max: 2 A
- Wide Input Range: 1.1 V to 5.5 V
  6 V abs max
- Controlled Rise Time: 335 µs at 3.3 V_{IN}
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- Wide Operating Temperature Range:
  -40 °C ~ 105 °C
- HBM: 6 kV, CDM: 2 kV
- Ultra-Small: 0.97 mm x 0.97 mm WLCSP

APPLICATIONS

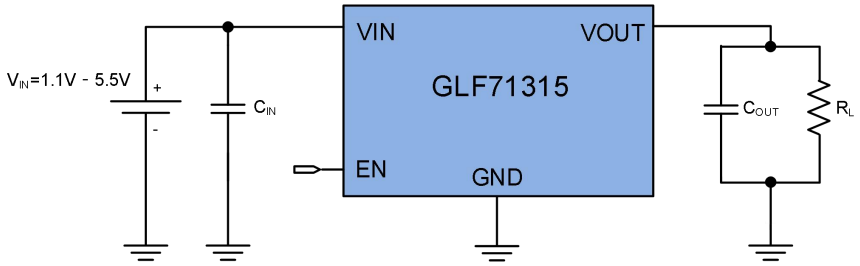
- Wearables
- Data Storage, SSD
- Mobile Devices
- Low Power Subsystems

PACKAGE



0.97mm x 0.97mm x 0.55mm WLCSP

APPLICATION DIAGRAM



ORDERING INFORMATION

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V	Output Discharge	EN Activity
GLF71315	HC	31 mΩ	85 Ω	High

FUNCTIONAL BLOCK DIAGRAM

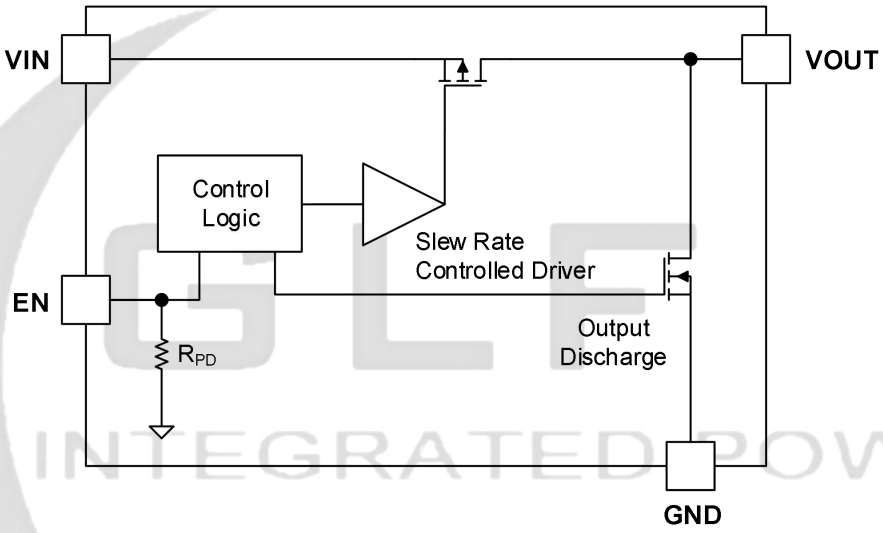


Figure 1. Functional Block Diagram

PIN CONFIGURATION

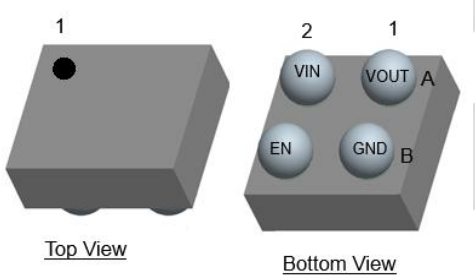


Figure 2. 0.97 mm x 0.97 mm x 0.55 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	VOUT	Switch Output
A2	VIN	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_{IN}, V_{OUT}, V_{EN} to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2	A
P_D	Power Dissipation at T_A = 25°C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	105	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.1	5.5	V
T_A	Ambient Operating Temperature	-40	+105	°C

ELECTRICAL CHARACTERISTICS

Values are at V_{IN} = 3.3V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
V_{IN}	Supply Voltage			1.1		5.5	V
I_Q	Quiescent Current (1)	EN = Enable, I_{OUT}=0 mA, V_{IN} = V_{EN} =5.5 V			7	70	nA
		EN = Enable, I_{OUT}=0 mA, V_{IN}= V_{EN}=5.5 V, Ta=85°C (5)			12		
		EN=Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=5.5 V, Ta=105°C (5)			17		
I_{SD}	Shut Down Current	EN = Disable, I_{OUT}=0 mA, V_{IN}=1.1 V			5		nA
		EN = Disable, I_{OUT}=0 mA, V_{IN}=1.8 V			6		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=3.3 V			9	35	
		EN = Disable, I_{OUT}=0 mA, V_{IN}=4.5 V			13		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V			28	100	
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=85°C (5)			1		µA
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=105°C (5)			2.7		
R_{ON}	On-Resistance	V_{IN}=5.5 V, I_{OUT}= 500 mA	Ta=25°C		31	34	mΩ
			Ta=85°C (5)		36		
			Ta=105°C (5)		39		
		V_{IN}=3.3 V, I_{OUT}= 500 mA	Ta=25°C		36	41	
			Ta=85°C (5)		43		
			Ta=105°C (5)		46		
		V_{IN}=1.8 V, I_{OUT}= 300 mA	Ta=25°C		52		
		V_{IN}=1.1 V, I_{OUT}= 100 mA	Ta=25°C		95		
R_{DSC}	Output Discharge Resistance	EN=Low , I_{FORCE}= 10 mA		70	85	100	Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}=1.1 V – 1.8 V		0.9			V
		V_{IN}=1.8 V - 5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN}=1.1 V – 1.8 V				0.3	V
		V_{IN}=1.8 V - 5.5 V				0.4	V
R_{EN}	EN pull down resistance	Internal Resistance			9.5		MΩ
I_{EN}	EN Current	EN=5.5 V				1.0	µA
Switching Characteristics							
t_{dON}	Turn-On Delay (2)	R_L=150 Ω, C_{OUT}=0.1 µF			210		µs
t_R	V_{OUT} Rise Time (2)				335		
t_{dON}	Turn-On Delay (2,5)	R_L=500 Ω, C_{OUT}=0.1 µF			220		
t_R	V_{OUT} Rise Time (2,5)				330		
t_{dOFF}	Turn-Off Delay (3,4,5)	R_L=10 Ω, C_{OUT}=0.1 µF			0.38		
t_F	V_{OUT} Fall Time (3,4,5)				1.3		
t_{dOFF}	Turn-Off Delay (3,4,5)	R_L=500 Ω, C_{OUT}=0.1 µF			0.9		
t_F	V_{OUT} Fall Time (3,4,5)				16		

Notes:
1. I_Q does NOT include Enable pull down current through the pull down resistor R_{PD}.
2. t_{ON} = t_{dON} + t_R
3. t_{OFF} = t_{dOFF} + t_F
4. Output discharge path is enabled during off.
5. By design; characterized, not production tested.

TIMING DIAGRAM

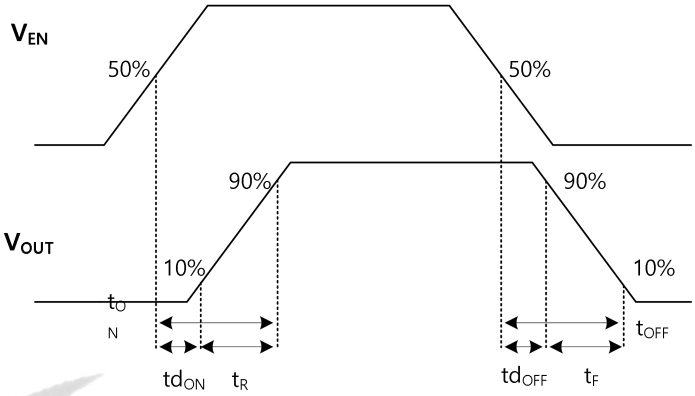


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

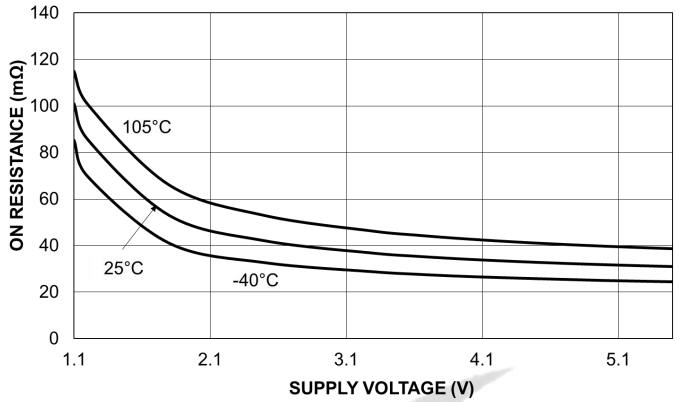


Figure 4. On-Resistance vs. Input Voltage

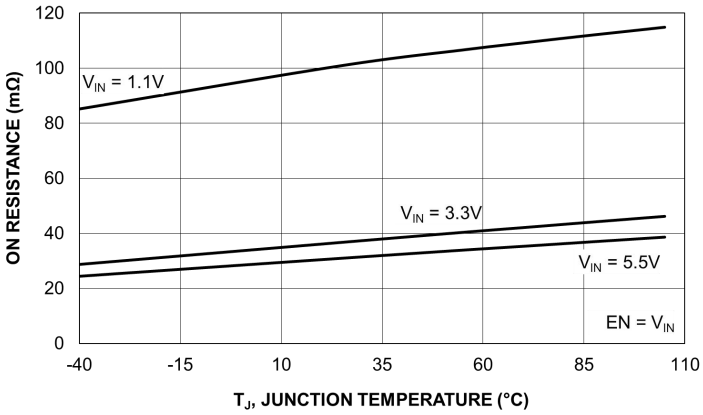


Figure 5. On-Resistance vs. Temperature

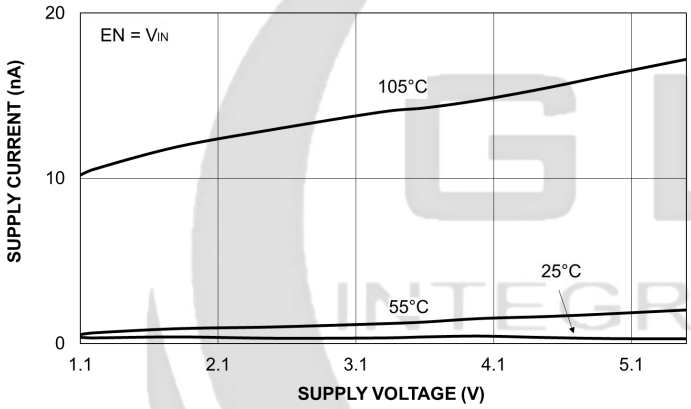


Figure 6. Quiescent Current vs. Input Voltage

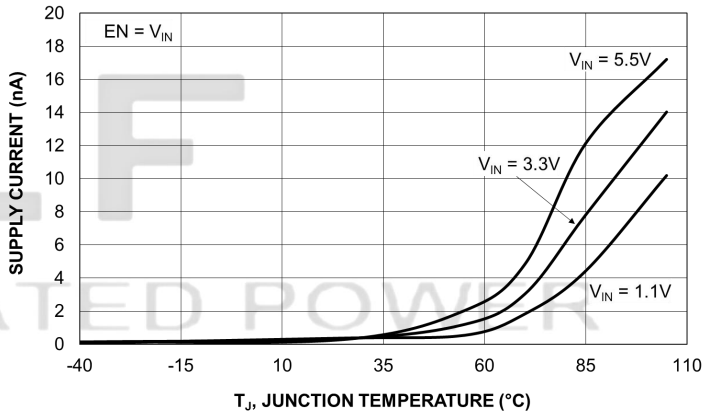


Figure 7. Quiescent Current vs. Temperature

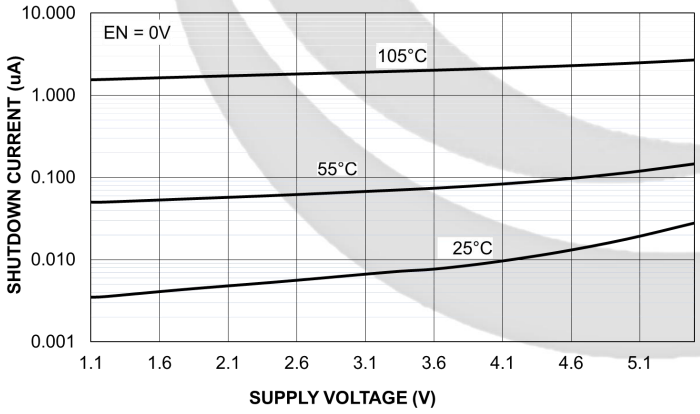


Figure 8. Shut Down Current vs. Input Voltage

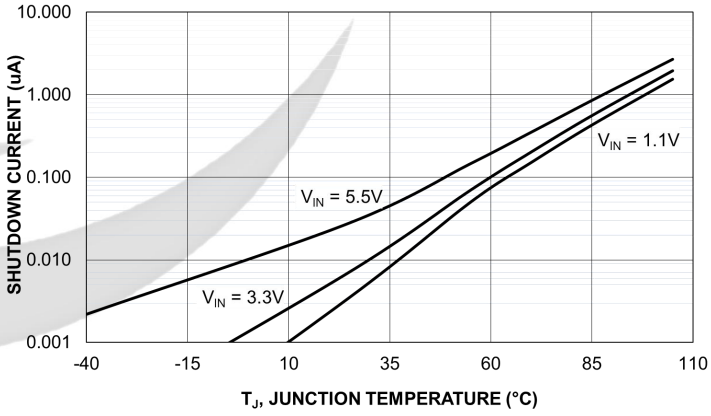


Figure 9. Shut Down Current vs. Temperature

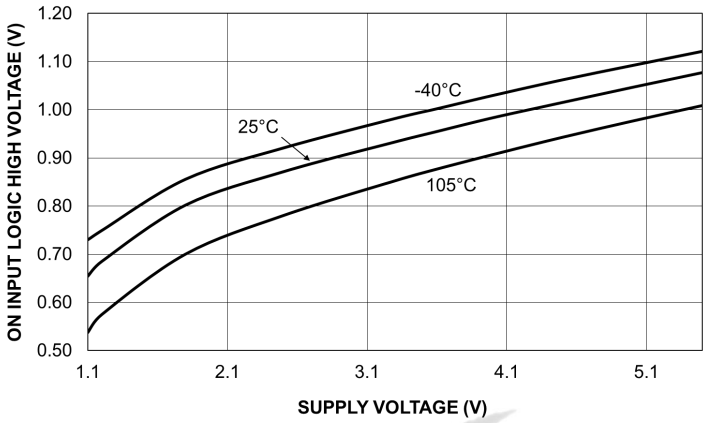


Figure 10. EN Input Logic High Threshold

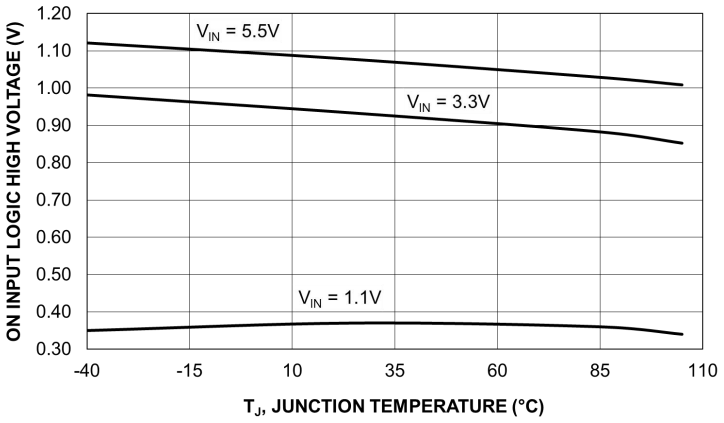


Figure 11. EN Input Logic High Threshold Vs. Temperature

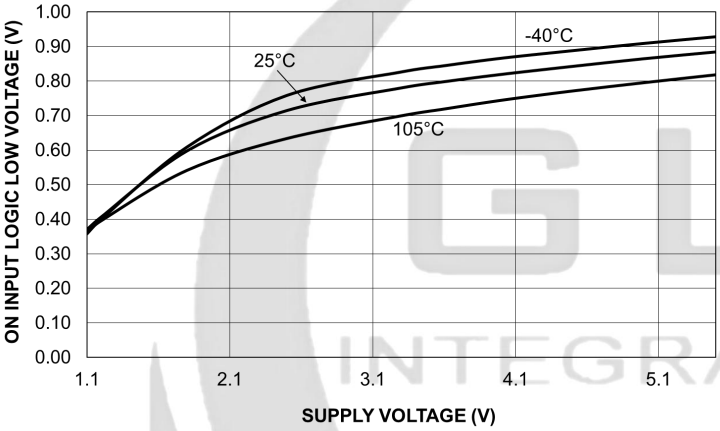


Figure 12. EN Input Logic Low Threshold

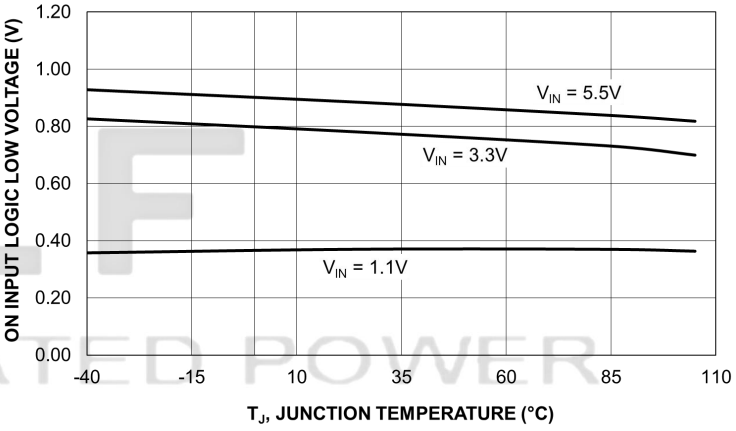


Figure 13. EN Input Logic Low Threshold Vs. Temperature

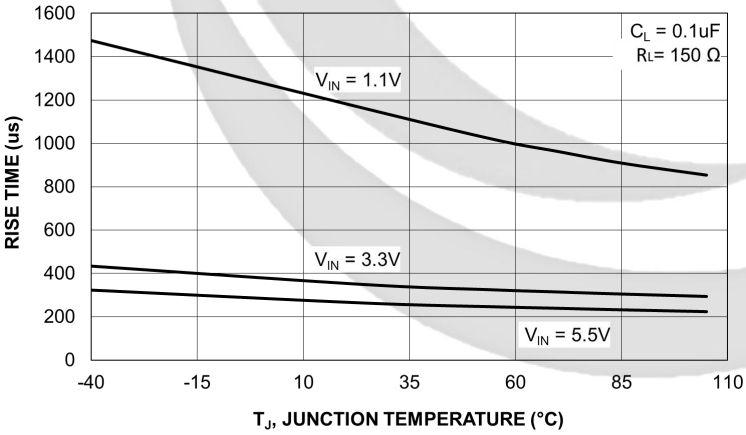


Figure 14. VOUT Rise Time vs. Temperature

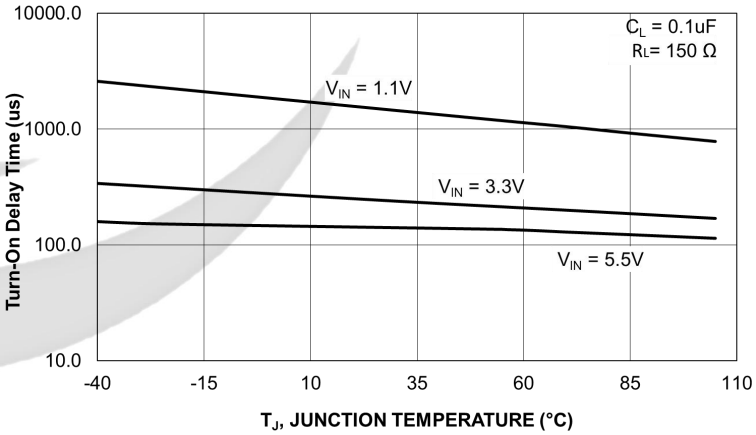


Figure 15. Turn-On Delay Time vs. Temperature

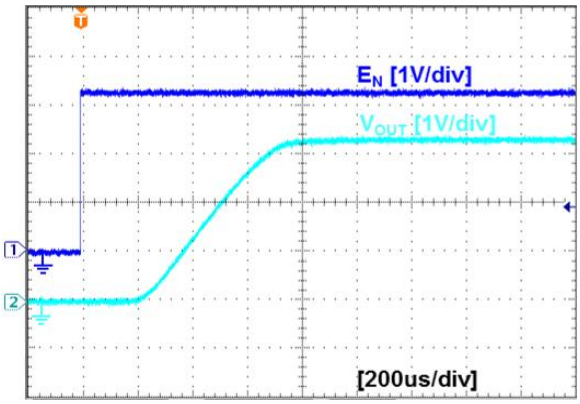


Figure 16. Turn-On Response
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT}=0.1 µF, R_L=10 Ω

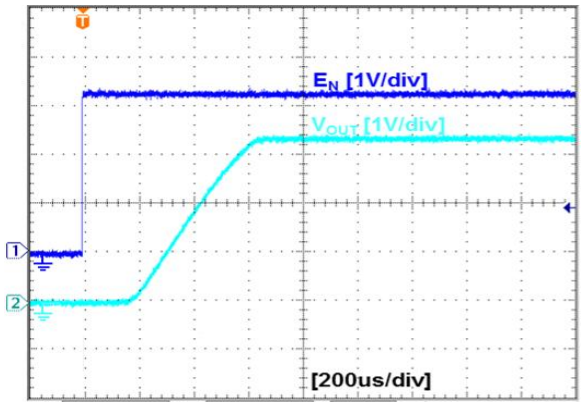


Figure 17. Turn-On Response
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT}=0.1 µF, R_L=500 Ω

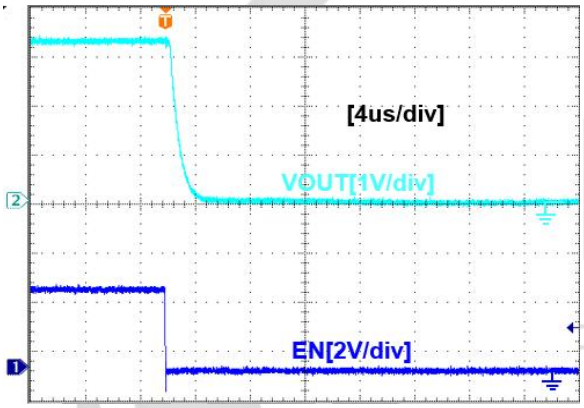


Figure 18. Turn-Off Response, Output Discharge
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT}=0.1 µF, R_L=10 Ω

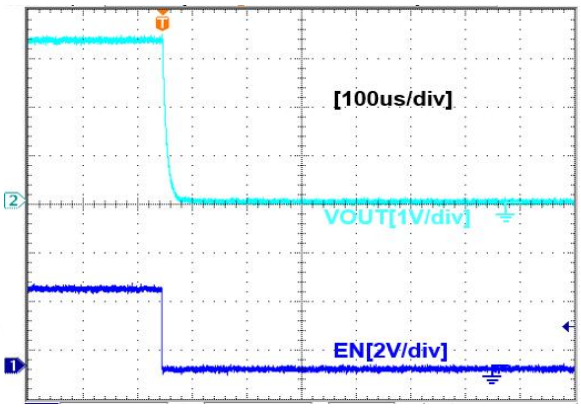


Figure 19. Turn-Off Response, Output Discharge
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT}=0.1 µF, R_L=500 Ω

APPLICATION INFORMATION

The GLF71315 is an integrated 2 A, Ultra-Efficient I_QSmart™ Load Switch device with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.97 mm x 0.97 mm x 0.55 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.5 mm pitch for manufacturability.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be spaced close to the VOUT and GND pins.

EN pin

The GLF71315 can be activated by forcing EN pin high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

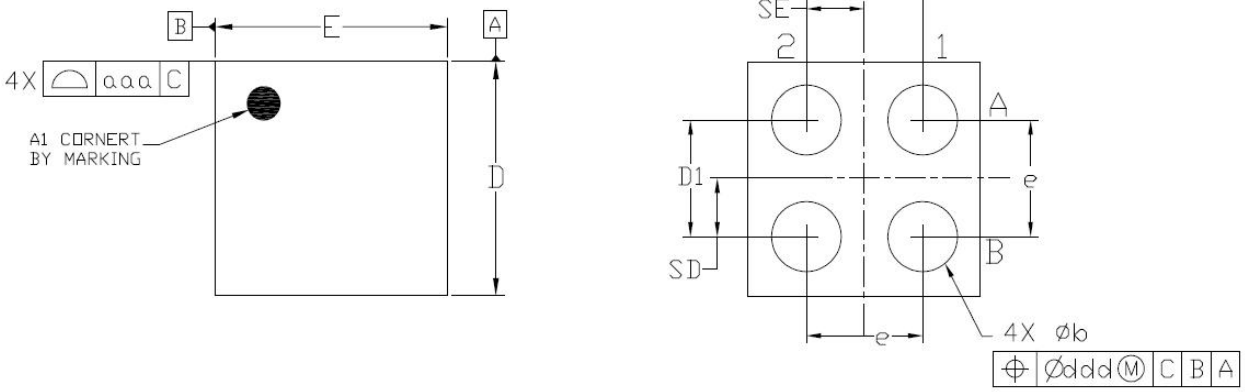
Output Discharge Function

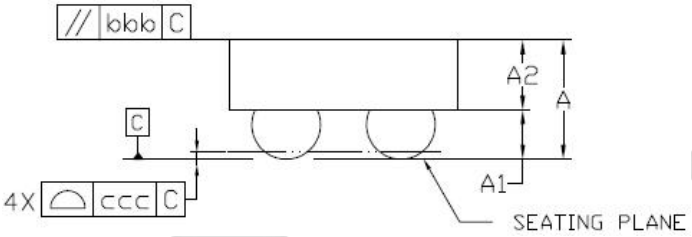
The GLF71315 has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

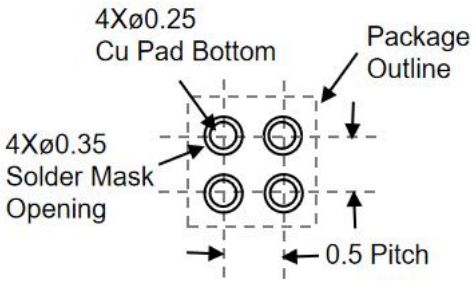
PACKAGE OUTLINE





Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.275	0.300	0.325
D	0.955	0.970	0.985
E	0.955	0.970	0.985
D1	0.450	0.500	0.550
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.250 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint

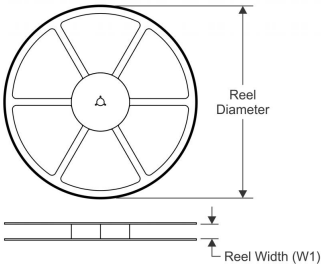


Notes

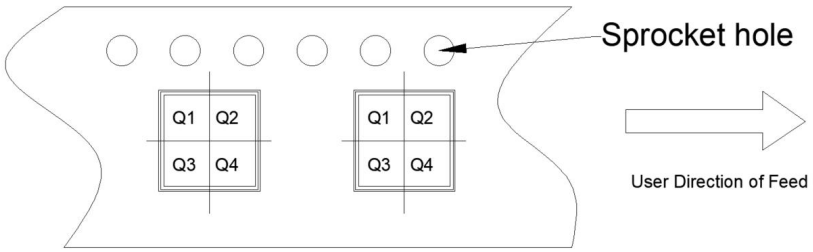
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

TAPE AND REEL INFORMATION

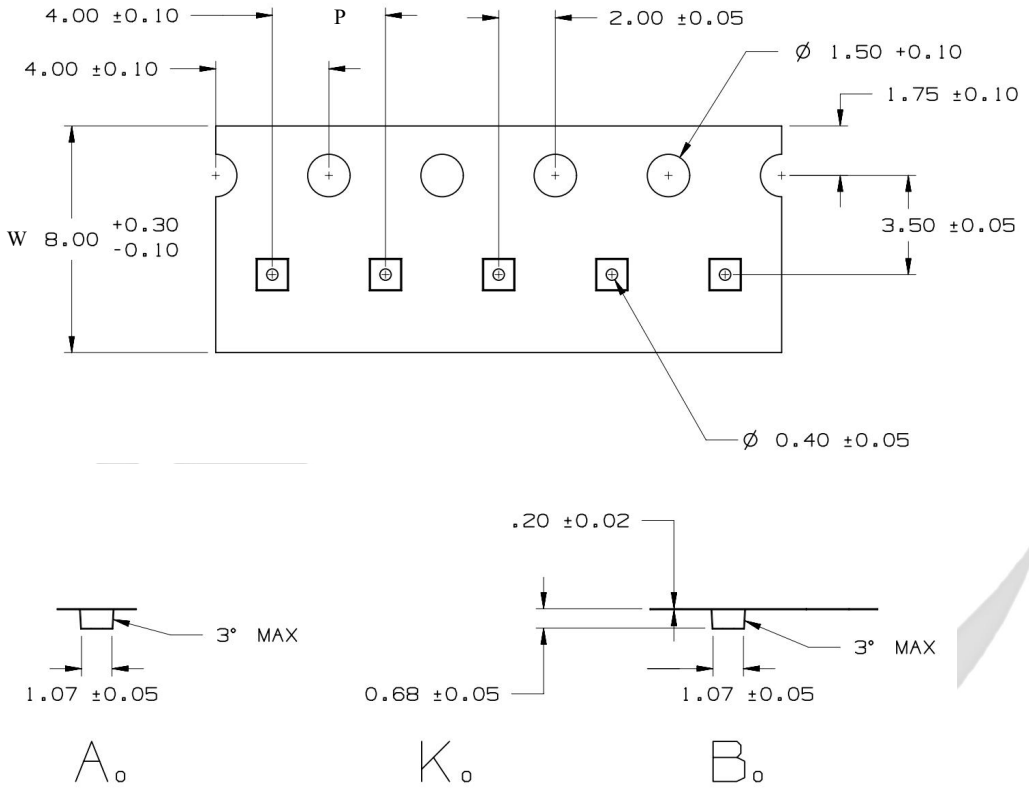
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF71315	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a preliminary version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

DISCLAIMERS

Information in this document is believed to be accurate and reliable, however GLF assumes no liability for errors or omissions. Device performance may be impacted by testing methods and application use cases. Users are responsible to independently evaluate the applicability, usability, and suitability of GLF devices in their application. In no case will GLF be liable for incidental, indirect, or consequential damages associated with the use, mis-use, or sale of its product. Customers are wholly responsible to assure GLF devices meet their system level and end product requirements. GLF retains the right to change the information provided in this data sheet without notice.