GLF76521 / GLF76521T

Integrated Load Switch with Deep Sleep Mode

Target Specification

DESCRIPTION

The GLF76521 / GLF76521T is an ultra-thin, ultra-efficient I_QSmart™ load switch with an integrated deep sleep timer for wearables and IoT devices.

The /SRO pin activates ultra-deep sleep mode, conserving power by isolating the system from the battery with ultra-low standby current of 7 nA typical. The load switch, placed between the battery and the system, can help significantly extend system battery life in mobile devices during shipping or periods of extended off time.

The part supports two methods for entering deep sleep mode: through user input or interrupt initiated events. Deep sleep can be enabled or exited by holding the /SRO pin low for a predefined delay time (ideal for user control) or by providing a rising edge signal to the OFF pin (ideal for logic or interrupt control).

To exit deep sleep, the user can hold down the /SRO pin to ground for 0.3 seconds, or simply connect a charger adapter to trigger the Wake pin.

The GLF76521 / GLF76521T helps to reduce power consumption with the best in class R_{ON} and a breakthrough on state I_Q of only 3 nA typical when the switch is on.

The GLF76521 / GLF76521T integrated 1 ms slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Uncontrolled switching can generate high inrush currents that result in voltage droop and / or bus reset events. The GLF slew rate control specifically limits inrush currents during turn-on to minimize voltage droop. The output discharge functions ensures the output voltage will drop off quickly when the switch is disabled.

The GLF76521 is available in 0.97mm x 1.47mm x 0.55mm wafer level chip scale package (WLCSP). **The GLF76521T is ultra-thin: 0.35 mm typ, 0.4 mm Max.**

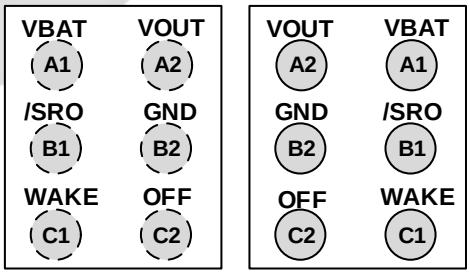
FEATURES

- Ultra-Low I_{SD}: 7 nA Typ @ 3.6VBAT
- Ultra-Low I_Q: 3 nA Typ @ 3.6VBAT
- Low R_{ON} : 31 mΩ Typ @ 3.6VBAT
- I_{OUT} Max : 2 A
- Wide Input Range: 1.8 V to 5.5 V
  6 V abs max
- Deep Sleep Mode by /SRO and OFF pins to disconnect the downstream system from the battery source
- Integrated Delay Time(Hold Time) to Deep Sleep, 1.8 s
- Turn-Off Delay Time, 1.8 s
- Controlled Output Rise Time: 1 ms at 3.6VBAT
- Integrated Output Discharge Switch When Disabled
- Operating Temperature Range: -40 to 85 °C
- HBM: 6 kV, CDM: 2 kV
- Ultra-Small: 0.97 mm x 1.47 mm WLCSP
- Ultra-Thin on GLF76521T: **0.35 mm typ**., 0.4 mm Max.

APPLICATIONS

- Wearables / Smart Cards
- IoT Devices
- Medical Devices

PACKAGE



TOP VIEW **BOTTOM VIEW**

0.97 mm x 1.47 mm x 0.55 mm WLCSP

0.97 mm x 1.47 mm x 0.35 mm Ultra-Thin WLCSP

DEVICE OPTIONS / PACKAGING INFORMATION

Part Number	Type	Top Mark	/SRO Hold Time	Output Discharge	Package	Tape and Reel Packaging
GLF76521	Deep Sleep after 1.8 sec	TT	1.8 sec	85 Ω	0.97 mm x 1.47 mm x 0.55 mm WLCSP	3000 Pieces on 7 inch reel
GLF76521T		TT		85 Ω	0.97 mm x 1.47 mm x 0.35 mm Ultra-Thin WLCSP	

APPLICATION DIAGRAM

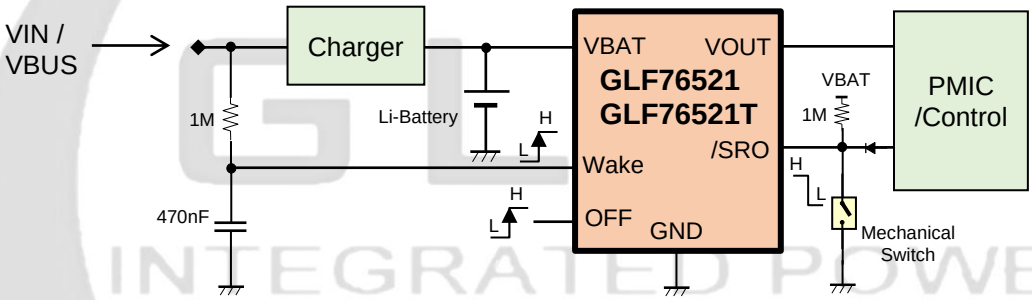


Figure 1. Typical Application with Standalone Charger IC

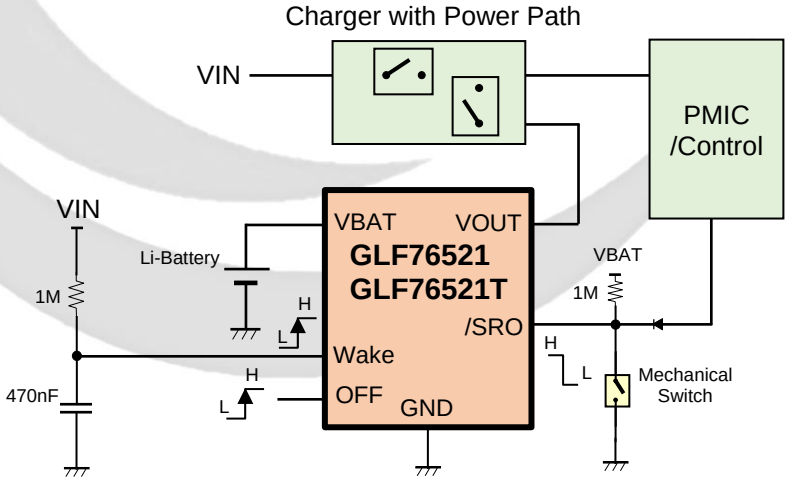


Figure 2. Typical Application with Charger IC with Power Path and PMIC

FUNCTIONAL BLOCK DIAGRAM

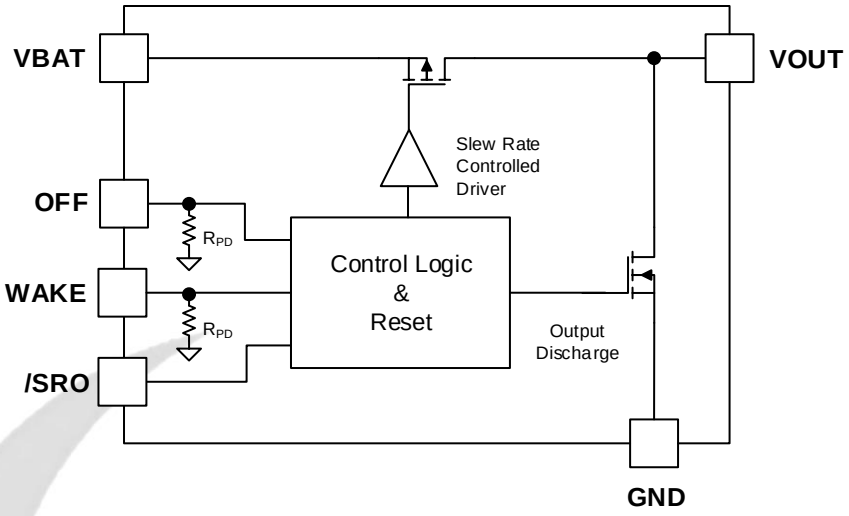
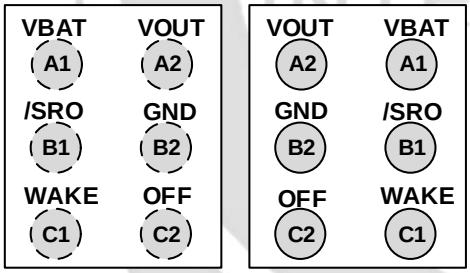


Figure 3. Functional Block Diagram

PIN CONFIGURATION



TOP VIEW **BOTTOM VIEW**

Figure 4. GLF76521 / GLF76521T Pinout

PIN DEFINITION

Pin #	Name	Description
A1	VBAT	Switch Input. VBAT pin connects to the positive input of an external battery.
A2	VOUT	Switch Output.
B1	/SRO	Reset Input or Power-On. Active Low. Requires an external pull-up resistor. Typically connects to the center between an external pull-up resistor tied to the battery and a mechanical key button on a device.
B2	GND	Ground.
C1	WAKE	System Wake Input. Triggered by rising edge signal to change the main switch from off to on-state. It has an internal pull-down resistance of 10 MΩ typ. to keep the WAKE pin grounded. No external pull-down resistor needed.
C2	OFF	Main Switch Off Input. Triggered by rising edge signal to change the main switch from on to off-state. It has an internal pull-down resistance of 10MΩ Typ. to keep the OFF pin grounded. No external pull-down resistor needed.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions. Extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VBAT, VOUT	Each Pin Voltage Range to GND		-0.3	6	V
/SRO, WAKE, OFF	Each Pin Voltage Range		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2	A
P_D	Power Dissipation at T_A = 25 °C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VBAT, VOUT	Supply Input and Output Voltage	1.8	5.5	V
/SRO, WAKE, OFF	Each Pin Voltage Range	0	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHRACTERISTICS

Values are at VBAT = 3.6 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
I_Q	Quiescent Current	VBAT = /SRO = 3.6 V, WAKE = OFF = GND I_{OUT} = 0 mA, Load Switch = On			3		nA
I_{SD}	Shut Down Current	VBAT = 3.6 V, VOUT = GND, Load Switch = Off			7	20	
		VBAT = 4.2 V, VOUT = GND, Load Switch = Off			9		
R_{ON}	On-Resistance	VBAT = 5.5 V, I_{OUT} = 500 mA	T_A = 25 °C		27		mΩ
			T_A = 85 °C (1)		32		
		VBAT = 4.2 V, I_{OUT} = 500 mA	T_A =25°C		29	31	
			T_A = 85 °C (1)		35		
		VBAT = 3.6 V, I_{OUT} = 500 mA	T_A = 25 °C		31	33	
			T_A = 85 °C (1)		37		
		VBAT = 3.0 V, I_{OUT} = 300 mA	T_A = 25 °C		34	36	
		VBAT = 1.5 V, I_{OUT} = 300 mA	T_A = 25 °C		70		
R_{DSC}	Output Discharge Resistance	VOUT = Off, I_{FORCE} = 10 mA		70	85	100	Ω
V_{IH}	Input Logic High Voltage (2)	VBAT = 1.5 to 5.5 V		1.2			V
V_{IL}	Input Logic Low Voltage (2)	VBAT = 1.5 to 5.5 V				0.5	
R_{PD}	Pull-down Resistance on OFF and Wake	VBAT = 5.5 V			10		MΩ
Power On (Load Switch Turn-On) and Deep Sleep Timing by /SRO (1)							
t_{VON}	Turn-On Delay Time(Hold Time)	VBAT = 3.6 V, R_L = 150 Ω, C_L = 10 µF			0.3		s
$t_{Slp-Dly}$	Delay Time(Hold Time) before Deep Sleep				1.8		
Power On (Load Switch Turn-On) Timing by WAKE (1)							
t_{dON}	Turn-On Delay	VBAT = 3.6 V, R_L = 150 Ω, C_L = 10 µF			0.8		ms
t_R	VOUT Rise Time				1		
t_{ON}	Turn-On Time (2)				1.8		
Power Off (Load Switch Turn-Off) by OFF (1)							
t_{SD}	Delay to Turn Off Load Switch	VBAT = 3.6 V, R_L = 150 Ω, C_L = 10 µF			1.8		s
t_F	VOUT Fall Time				1		ms
t_{OFF}	Turn Off Time (3)				1.9		s

Notes:

1. By design; characterized, not production tested.
2. Input pins are /SRO, OFF and WAKE.
3. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{SD} + t_F$

TIMING DIAGRAMS AND INPUT CONDITION

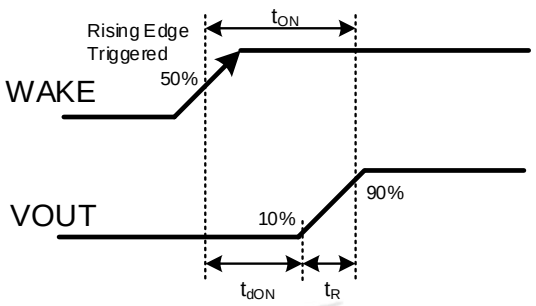


Figure 5. Power On by WAKE Pin

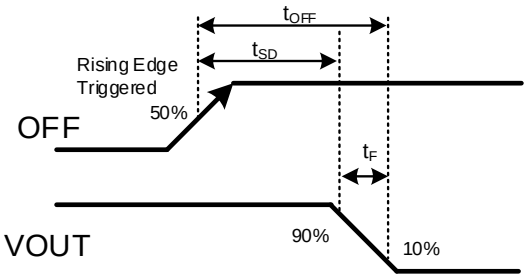


Figure 6. Power Off by OFF Pin

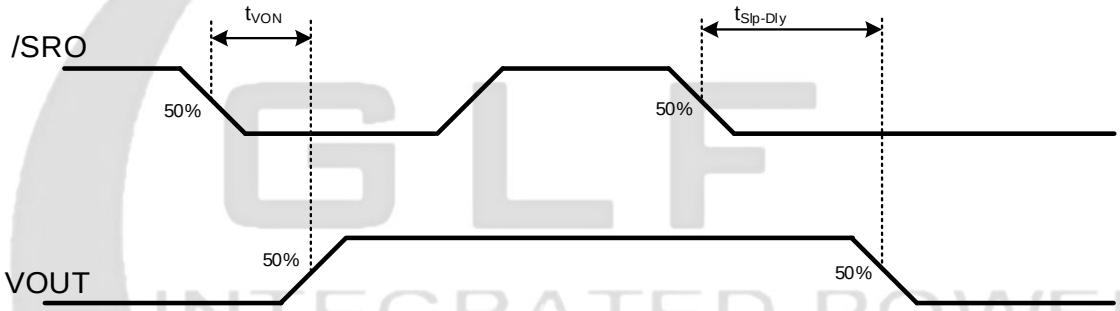


Figure 7. Power On and Deep Sleep by /SRO Pin

Pin Name	/SRO	WAKE	OFF	VOUT
Default State	1	0	0	GND

Notes: 1 = Logic High, 0 = Logic Low. VOUT = GND means internal load switch is off.

Table 1. Pin Default State with Input Power Source

Function	/SRO	WAKE	OFF	Delay Time(Hold time)	VOUT Action
Power-On	High to Low & Hold for t_{VON} = 0.3 s	X	X	t_{VON} = 0.3 s	VOUT = VBAT
	High	Low to High Rising Edge Triggered	X	t_{dON} = 0.8 ms (2)	VOUT = VBAT
Power-Off into Deep Sleep	High to Low & Hold for $t_{Slp-Dly}$ = 1.8 s	X	X	$t_{Slp-Dly}$ = 1.8 s	VOUT to GND
	High	Low	Low to High Rising Edge Triggered	t_{SD} = 1.8 s	VOUT to GND

Notes:
1. X = don't care
2. t_{dON} can be extended with external an capacitor on WAKE pin via RC time constant and trigger level of rising edge.

Table 2. Input Conditions and VOUT

TYPICAL PERFORMANCE CHARACTERISTICS

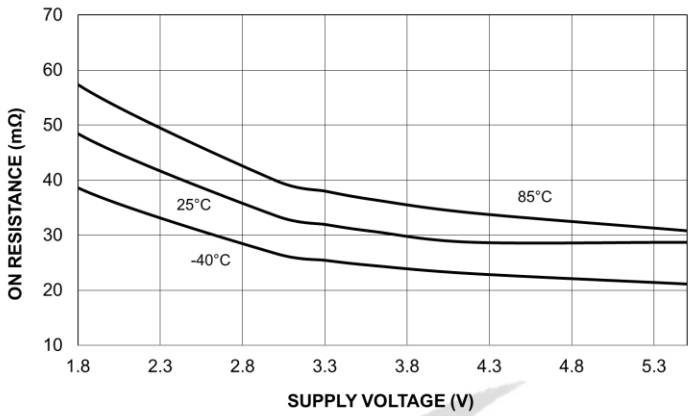


Figure 8. On-Resistance vs. Input Voltage

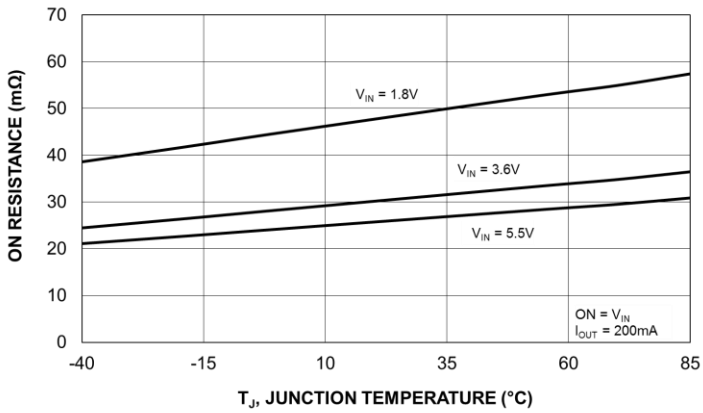


Figure 9. On-Resistance vs. Temperature

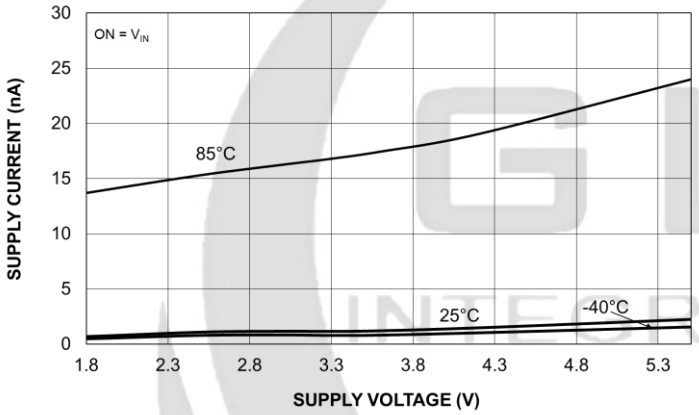


Figure 10. Quiescent Current vs. Input Voltage

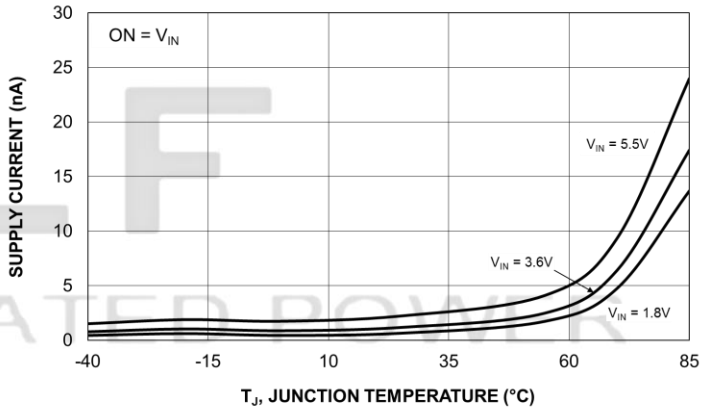


Figure 11. Quiescent Current vs. Temperature

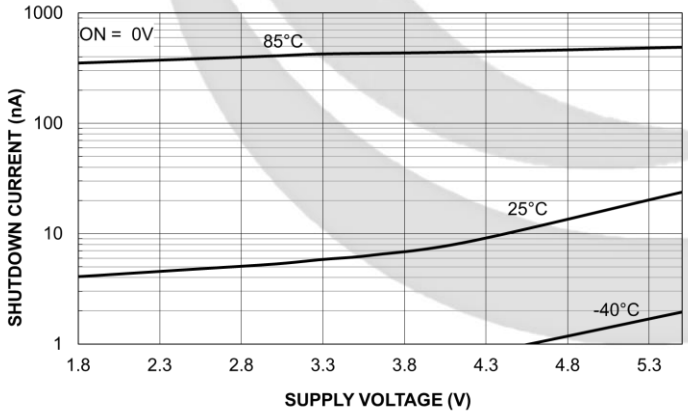


Figure 12. Shut Down Current vs. Input Voltage

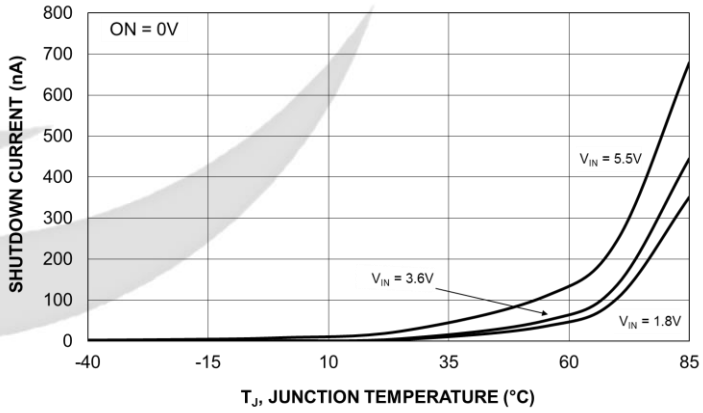


Figure 13. Shut Down current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

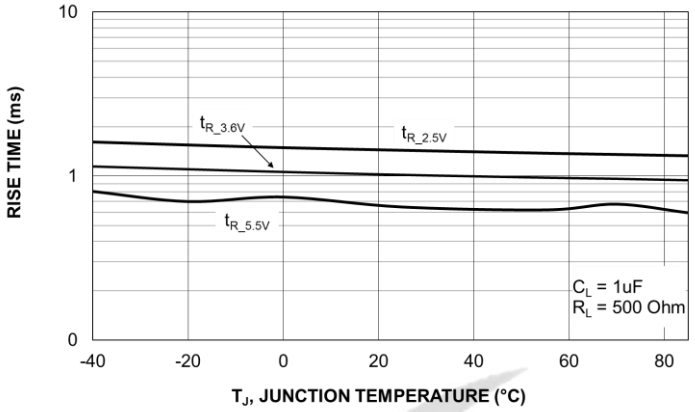


Figure 14. V_{OUT} Rise Time vs. Temperature

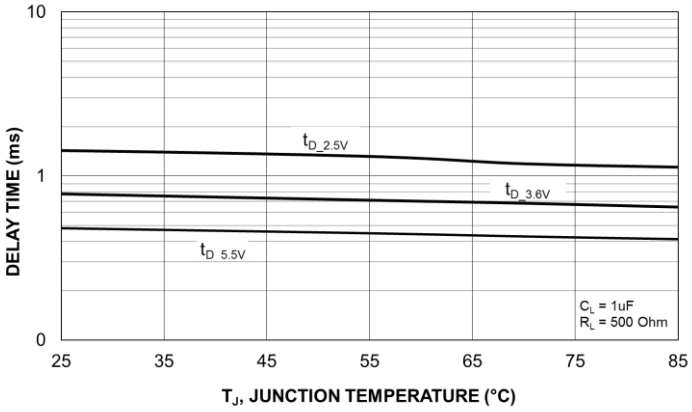


Figure 15. Turn-On Delay Time vs. Temperature

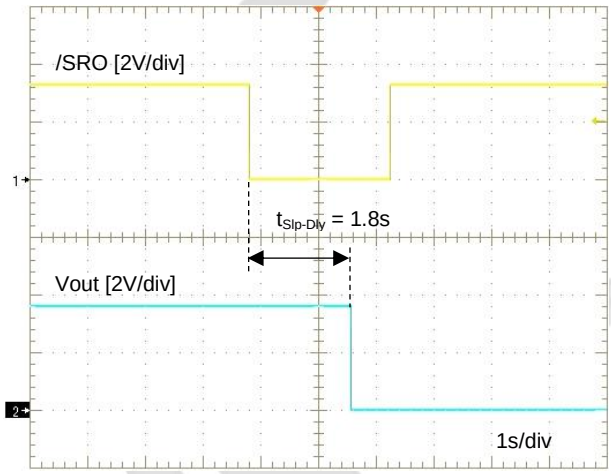


Figure 16. Delay time before Deep Sleep, $t_{Slp-Dly}$

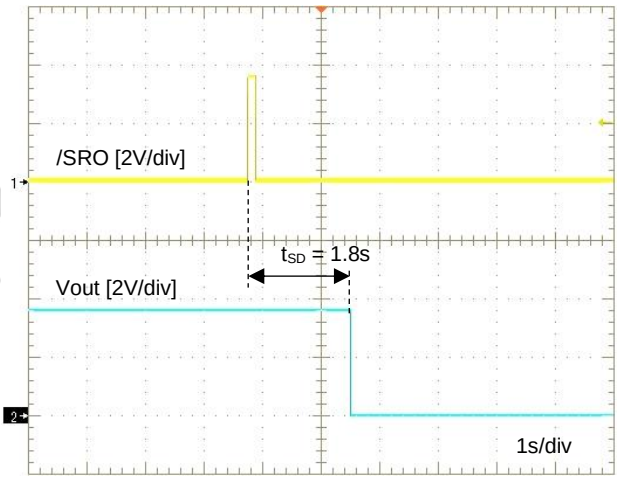


Figure 17. Turn-Off Response, t_{SD}

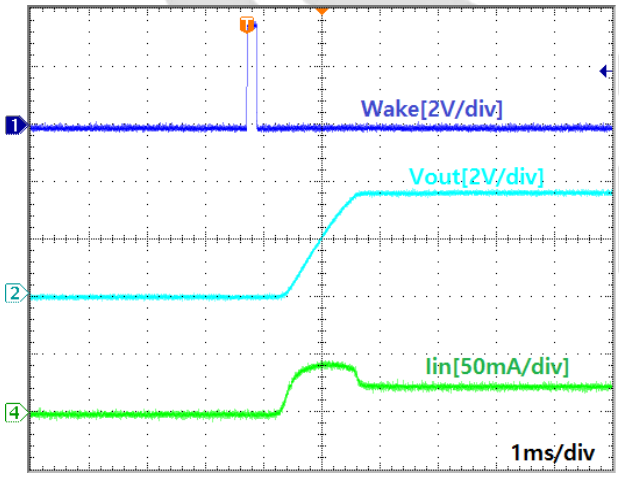


Figure 18. Turn-On Response
V_{IN}=3.6V, C_{IN}=10uF, C_L=10uF, R_L=150Ω

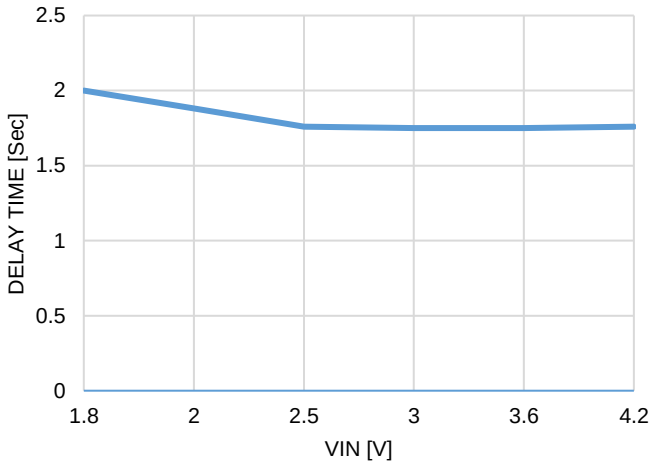


Figure 19. Delay Time of t_{SD} and $t_{Slp-Dly}$ vs. Input Voltage
C_{IN}=10uF, C_L=10uF, R_L=150Ω

APPLICATION INFORMATION

The GLF76521 / GLF76521T is an integrated load switch with deep sleep mode and is optimized to significantly extend battery life in mobile devices during long periods of shipping or off time. Typical applications are shown in Fig.1 and Fig. 2.

Power-On

There are two methods to enable the main switch of GLF76521 / GLF76521T and exit deep sleep mode. Fig. 20 shows the power-on sequence by /SRO and WAKE pins. The output discharge switch is active during deep sleep mode.

1) /SRO pin
While the main switch is turned off, holding the /SRO pin low for the preset delay time of 0.3 seconds turns the main switch on to wake up the downstream system.

2) WAKE pin
A rising edge on the WAKE pin turns on the main switch to connect the battery to the downstream system. The on delay time, t_{dON}, can be extended with an external capacitor on WAKE pin via RC time constant and trigger level of rising edge. The WAKE pin has an internal pull-down resistor of typically 10 MΩ to maintain a low state when no signal is asserted.

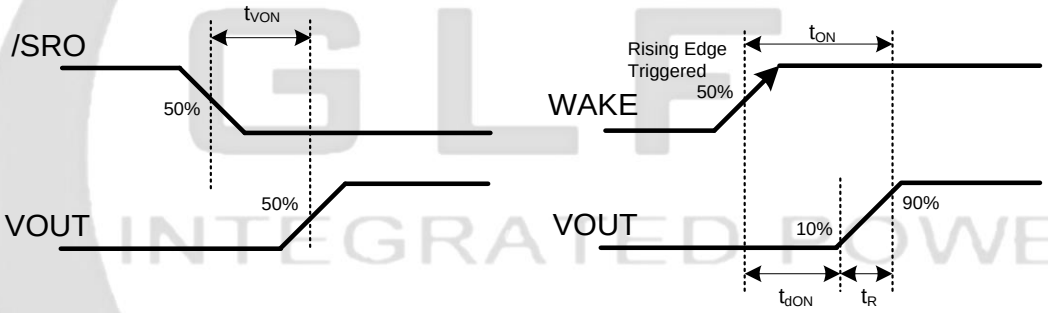


Figure 20. Power-On Mode by /SRO and WAKE

Deep Sleep Function

The GLF76521 / GLF76521T allows a mobile or wearable device to enter the deep sleep mode by disconnecting the downstream system from the battery and consuming only 7 nA typical standby current. There are two ways to enable deep sleep mode. Fig. 21 shows how to enter the deep sleep mode by /SRO or OFF pin. The output discharge switch is active when the main switch is off to quickly discharge VOUT to GND.

1) /SRO pin
While the main switch is turned on, holding the /SRO pin low for the preset delay time ($t_{Slp\text{-}Dly}$), of 1.8 seconds turns the main switch off and turns on the internal output discharge switch to quickly discharge VOUT. The GLF76521 / GLF76521T consumes ultra-low standby leakage current to maintain battery charge during deep sleep mode. If the /SRO pin enters a high state before the preset delay time of 1.8 seconds, VOUT remains connected to VBAT. The /SRO pin requires a pull-up resistor tied to the battery to maintain a high state during normal operation. An external key button on a device allows users to enter deep sleep mode as well as reset the system.

2) OFF pin
While the main switch is turned on, a rising edge on the OFF pin will put the GLF76521 / GLF76521T into deep sleep mode after the preset delay time (t_{SD}) of 1.8 seconds. The internal output discharge switch is turned on to quickly discharge VOUT. Note the /SRO pin has priority; if /SRO transitions from logic low to high within the preset delay time, the turn-off process is terminated and VOUT remains connected to VBAT. Another rising edge on the OFF pin will restart the turn-off process. The OFF pin has an internal pull-down resistor of typically 10 MΩ to maintain a low state when no signal is asserted.

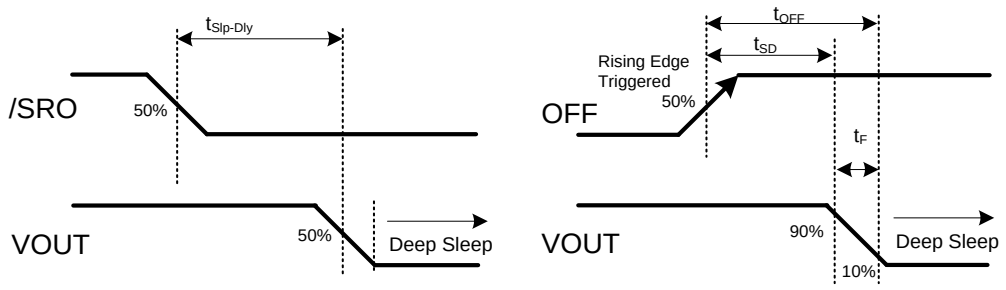


Figure 21. Deep Sleep Mode by /SRO and OFF

Input Priority

The GLF76521 / GLF76521T can enter or exit deep sleep mode via /SRO, OFF, and WAKE pins. When two input pins are asserted at the same time or in any sequence, the highest priority pin function takes place and any lower priority pin is ignored to avoid conflicts.

Input	Priority (1 : Highest)
/SRO	1
WAKE	2
OFF	3

Table 3. Pin Priority

Output Discharge Function

The GLF76521 / GLF76521T has an internal discharge switch on VOUT active during deep sleep mode. It will discharge any voltage on the downstream system quickly when the main switch is turned off. When the main switch is enabled, the output discharge switch is turned off.

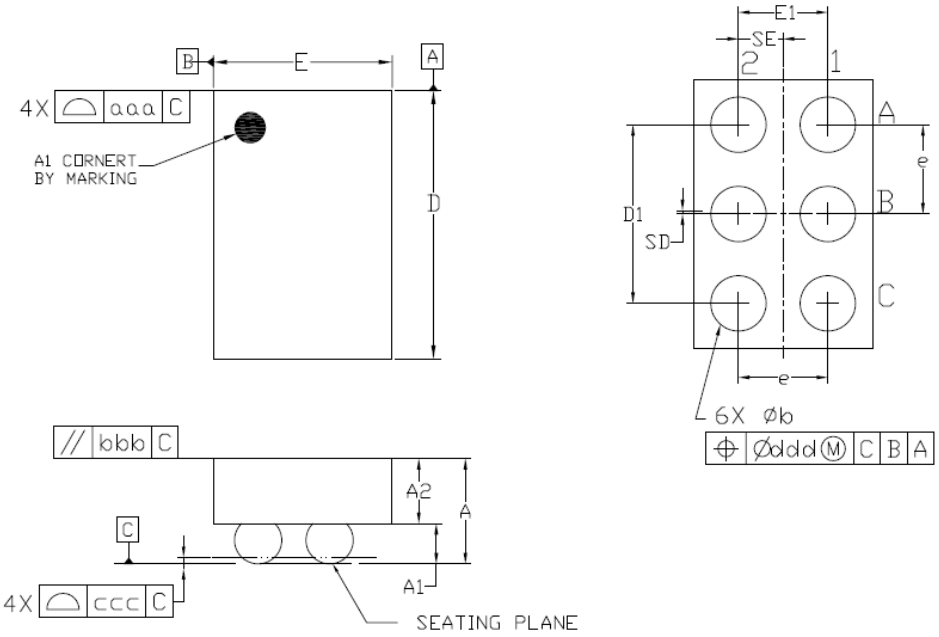
Input Capacitor

A 0.1 µF capacitor placed close to the VBAT pin is recommended to reduce voltage drop on the input power rail caused by transient inrush current at start-up. A higher capacitance value can be used to further attenuate the input voltage drop.

Output Capacitor

A 0.1 µF capacitor placed close to the VOUT pin is recommended to mitigate voltage undershoot on the output pin when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances exist, use of an output capacitor can improve output voltage stability and system reliability.

PACKAGE OUTLINE (GLF76521)

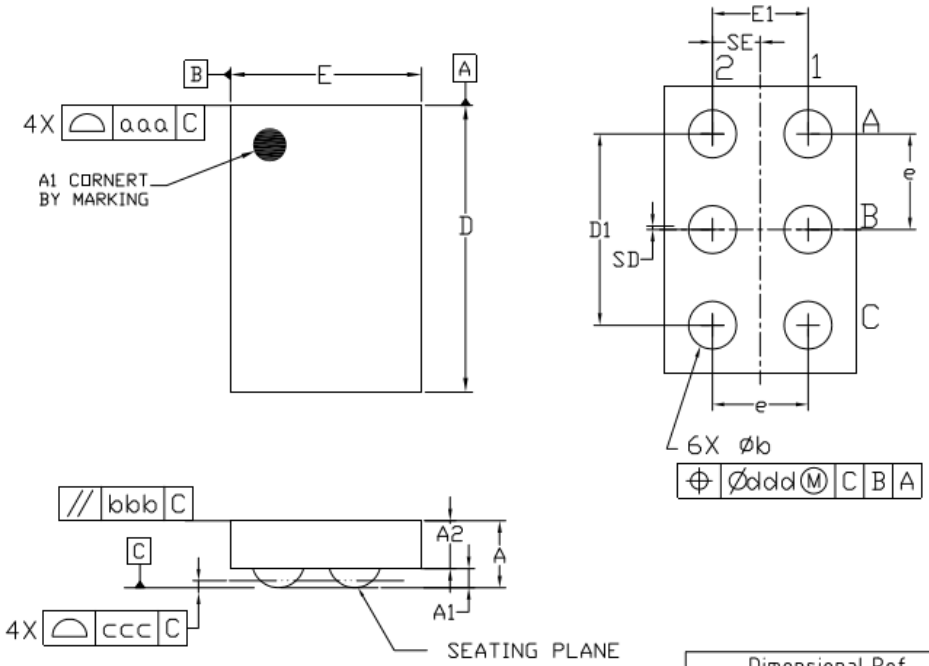


Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.275	0.300	0.325
D	1.460	1.470	1.485
E	0.960	0.970	0.985
D1	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.000 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

ULTRA-THIN PACKAGE OUTLINE (GLF76521T)



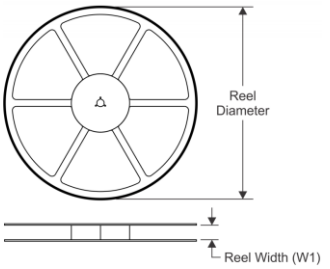
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.300	0.350	0.400
A1	0.075	0.100	0.125
A2	0.225	0.250	0.275
D	1.460	1.470	1.485
E	0.960	0.970	0.985
D1	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.210	0.250	0.290
e	0.500 BSC		
SD	0.000 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

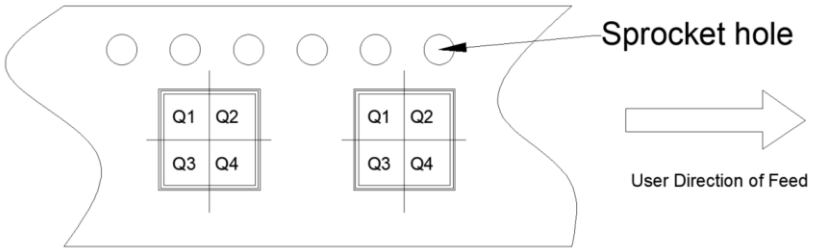
1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

TAPE AND REEL INFORMATION

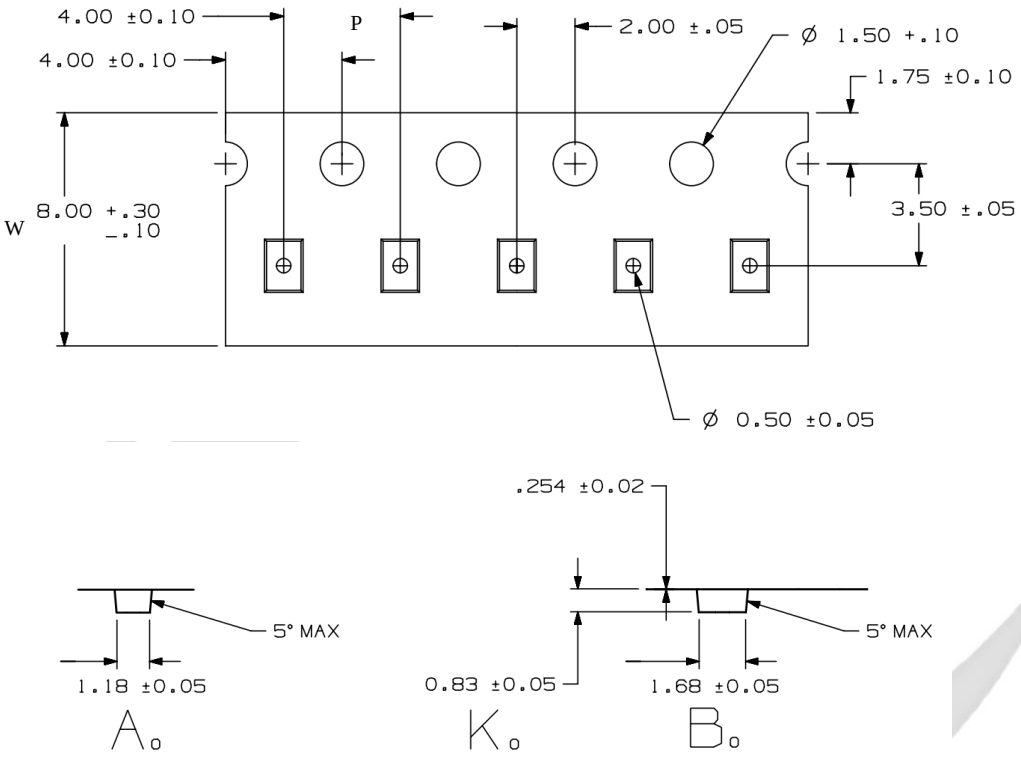
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF76521	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

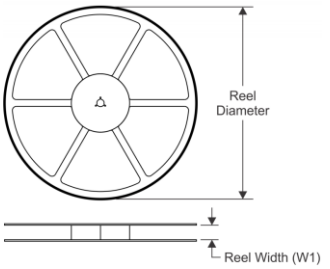
C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

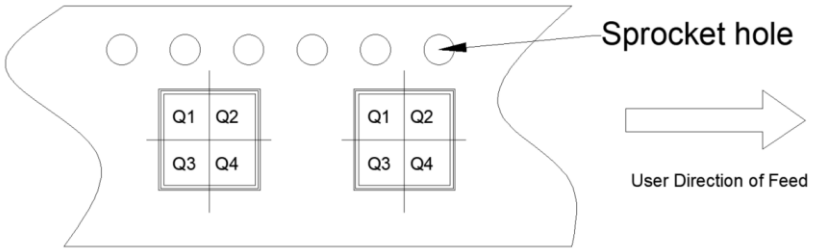
P: Pitch between successive cavity centers

TAPE AND REEL INFORMATION

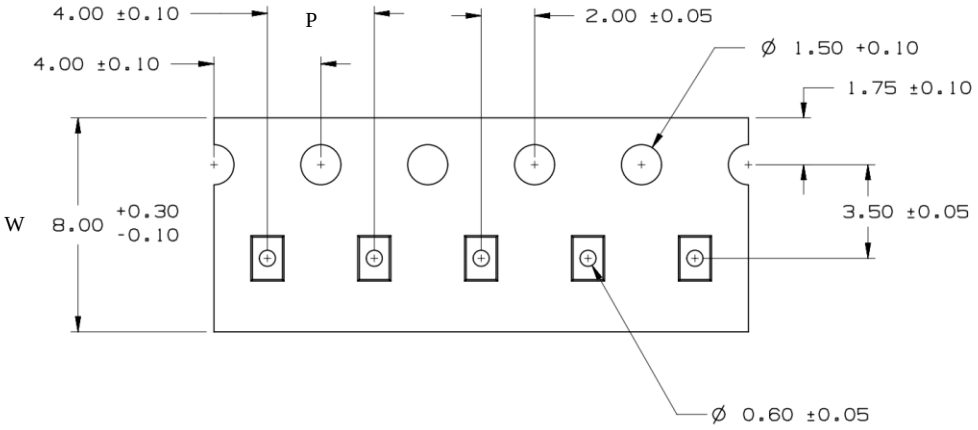
REEL DIMENSIONS

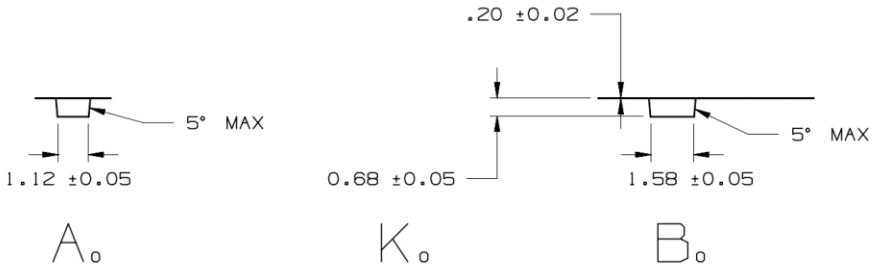


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF76521T	WLCSP	6	3000	180	9	1.12	1.58	0.68	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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