GLF72510, GLF72511

3 A Ultra Low Current Consumption N-channel Load Switch with Lower Input Voltage Range and Reverse Current Blocking

Product Specification

DESCRIPTION

The GLF72510 / GLF72511 Load Switch is a fully integrated 2A NMOS load switch with I_QSmart™ advanced technology. The device is targeted for the mobile computing and data storage markets as a high performance, low cost solution for load switch applications.

The GLF72510 / GLF72511 has a constant low on-resistance of 27 mΩ at room temperature. The fixed rise time helps prevent undesirable inrush current when turned on and the internal EN pin pulldown resistor ensures the device remains in the shutdown mode when disabled. In shutdown mode the GLF72510 / GLF72511 draws only 6 nA typical at 3.6 V input supply voltage.

The GLF72510 / GLF72511 is available in a wafer level chip scale package (WLCSP) measuring 0.97 mm x 0.97 mm x 0.55mm with a 0.5 mm pitch. This allows the user to save board space and increase cost savings.

The GLF72510 / GLF72511 features a reverse current blocking protection. When the GLF72510 / GLF72511 is disabled, it prevents reverse current flowing from the output to the input source.

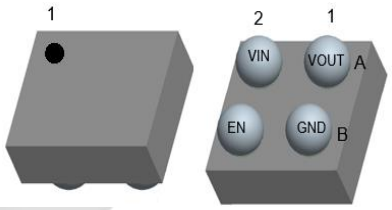
FEATURES

- Supply Voltage Range : 0.8 V to 3.6 V
- Low R_{ON} : 27 mΩ Typ at Supply Voltage Range
- I_{OUT} Max : 3 A
- Ultra-Low I_Q :
  - 50 nA Typ at 0.8 V_{IN}
  - 60 nA Typ at 1.0 V_{IN}
  - 80 nA Typ at 1.2 V_{IN}
- Integrated Slew Rate Control Driver
- Reverse Current Blocking Protection When Disabled
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch: GLF72511
- HBM : 6 kV, CDM : 2 kV
- Ultra-Small : 0.97mm x 0.97mm x 0.55mm Wafer Level Chip Scale Package

APPLICATIONS

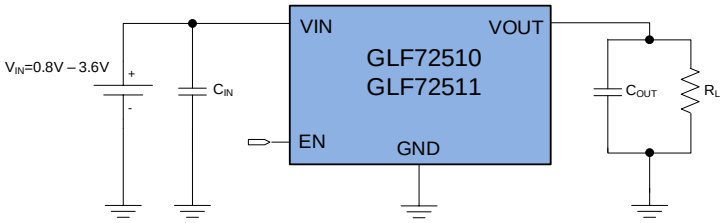
- Wearables
- Data Storage, SSD
- Low Power Subsystems

PACKAGE



0.97 mm x 0.97 mm x 0.55 mm WLCSP

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at 3.6 V	Output Discharge	EN Activity
GLF72510	CP	27 mΩ	No	High
GLF72511	CQ	27 mΩ	Yes	High

FUNCTIONAL BLOCK DIAGRAM

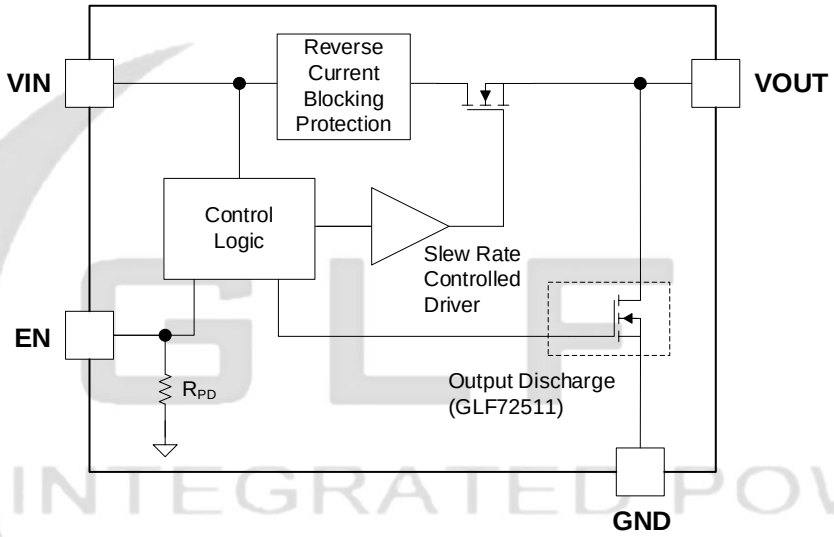


Figure 1. Functional Block Diagram

PIN CONFIGURATION

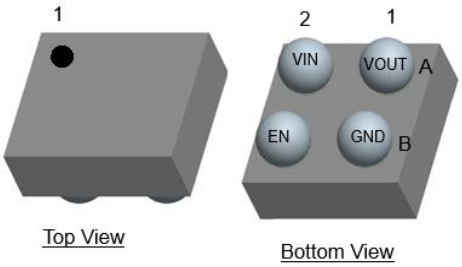


Figure 2. 0.97mm x 0.97mm x 0.55mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	V_{OUT}	Switch Output
A2	V_{IN}	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_{IN}, V_{OUT}, V_{EN} to GND		-0.3	4	V
I_{OUT}	Maximum Continuous Switch Current			3	A
P_D	Power Dissipation at T_A = 25°C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	0.8	3.6	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.8 V to 3.6 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Basic Operation						
I_Q	Quiescent Current	EN = Enable, I_{OUT} = 0 mA, V_{IN} = 0.8 V		50		nA
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 1.0 V		60		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 1.2 V		80		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 2.5 V		3		uA
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.0 V		8		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.3 V		10		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.6 V		15		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.6 V, Ta = 85 °C		29		
I_{SD}	Shutdown Current	EN = Disable, I_{OUT} = 0 mA, V_{IN} = 0.8 V		2		nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.0 V		2		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.2 V		3		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 2.5 V		4		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.0 V		5		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.3 V		5		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.6 V		6	15	
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.6 V, Ta = 85 °C		470	550	
R_{ON}	On-Resistance	V_{IN} = 0.8 V to 3.6 V, I_{OUT} = 300 mA, Ta = 25 °C		27	33	mΩ
		V_{IN} = 0.8 V to 3.6 V, I_{OUT} = 300 mA, Ta = 85 °C		35	40	
V_{IH}	EN Input Logic High Voltage	V_{IN} = 0.8 V – 1.5 V	0.8			V
		V_{IN} = 1.5 V – 3.6 V	1.1			V
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 0.8 V – 1.5 V			0.2	V
		V_{IN} = 1.5 V – 3.6 V			0.5	V
R_{EN}	EN pull down resistance	Internal Resistance		10		MΩ
R_{DSC}	Output Discharge Resistance (1)	GLF72511, EN = GND		85		Ω

Notes: 1. Output discharge path is disabled when main switch is off.

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.8 V to 3.6 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Characteristics (2)						
t_{dON}	Turn-On Delay R_{OUT} = 150 Ω, C_{OUT} = 0.1 µF	V_{IN} = 0.8 V		470		µs
		V_{IN} = 1.2 V		270		
		V_{IN} = 3.3 V		150		
		V_{IN} = 3.6 V		140		
t_R	V_{OUT} Rise Time R_{OUT} = 150 Ω, C_{OUT} = 0.1 µF	V_{IN} = 0.8 V		490		
		V_{IN} = 1.2 V		480		
		V_{IN} = 3.3 V		420		
		V_{IN} = 3.6 V		430		
t_{dOFF}	Turn-Off Delay R_{OUT} = 150 Ω, C_{OUT} = 0.1 µF	V_{IN} = 0.8 V		80		
		V_{IN} = 1.2 V		5		
		V_{IN} = 3.3 V		2		
		V_{IN} = 3.6 V		1		
t_F	V_{OUT} Fall Time, GLF72510 R_{OUT} = 150 Ω, C_{OUT} = 0.1 µF	V_{IN} = 0.8 V		30		
		V_{IN} = 1.2 V		30		
		V_{IN} = 3.3 V		30		
		V_{IN} = 3.6 V		30		
	V_{OUT} Fall Time, GLF72511 R_{OUT} = 150 Ω, C_{OUT} = 0.1 µF	V_{IN} = 0.8 V		24		
		V_{IN} = 1.2 V		14		
		V_{IN} = 3.3 V		11		
		V_{IN} = 3.6 V		12		

Notes: 2. By design; characterized, not production tested. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$

TIMING DIAGRAM

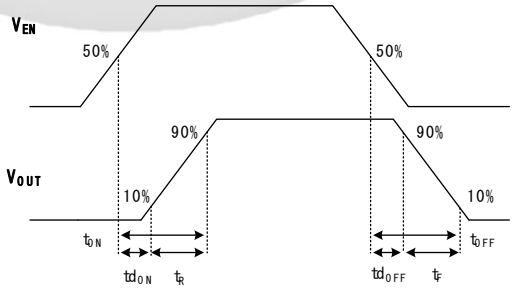


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

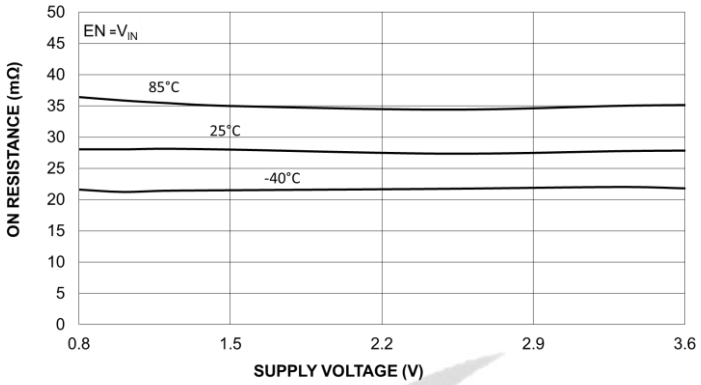


Figure 1. On-Resistance vs. Supply Voltage

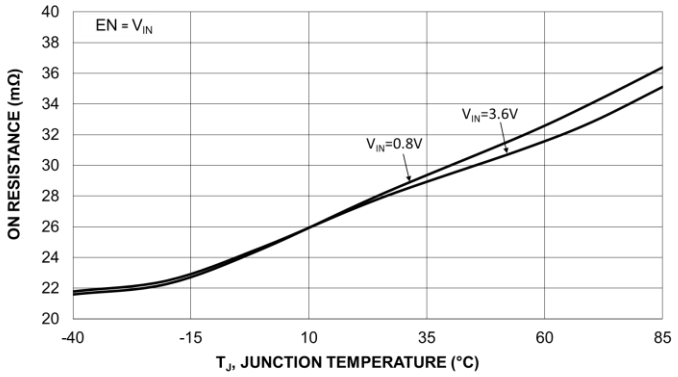


Figure 2. On-Resistance vs. Temperature

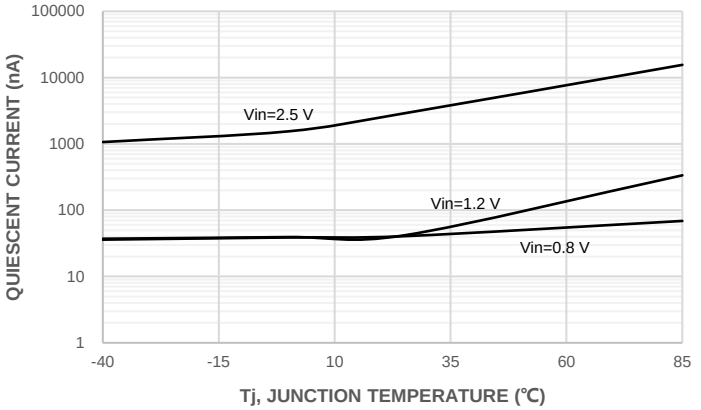


Figure 3. Quiescent Current vs. Temperature

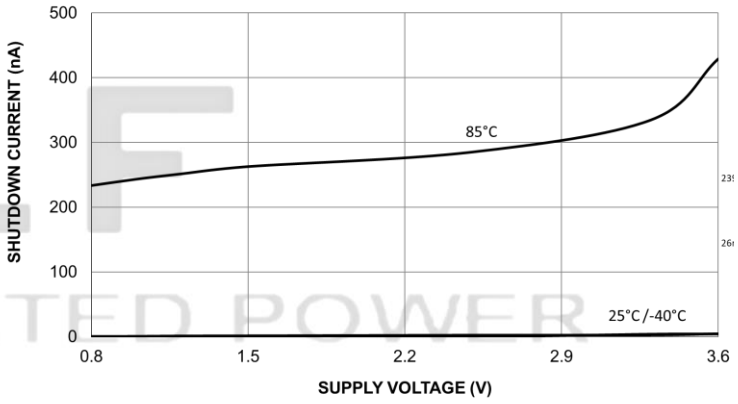


Figure 7. Shutdown Current vs. Supply Voltage

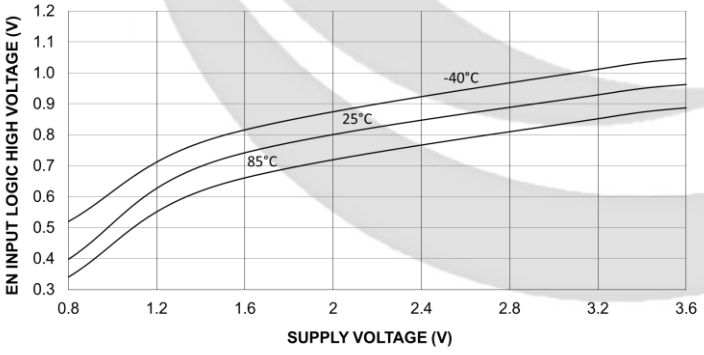


Figure 8. EN Input Logic High Threshold

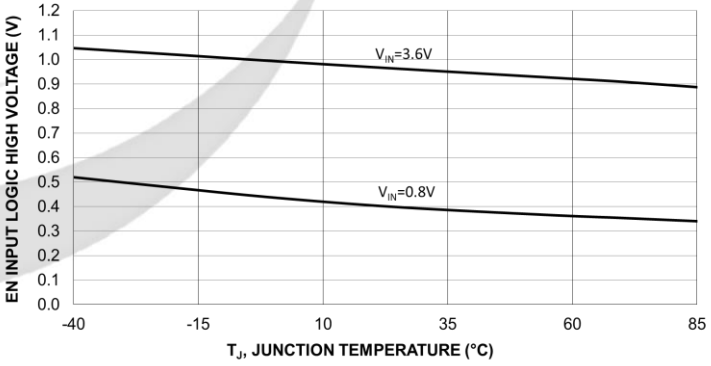


Figure 9. EN Input Logic High Threshold Vs. Temperature

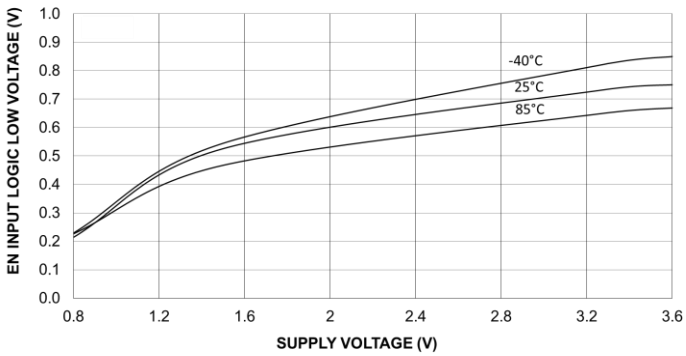


Figure 40. EN Input Logic Low Threshold

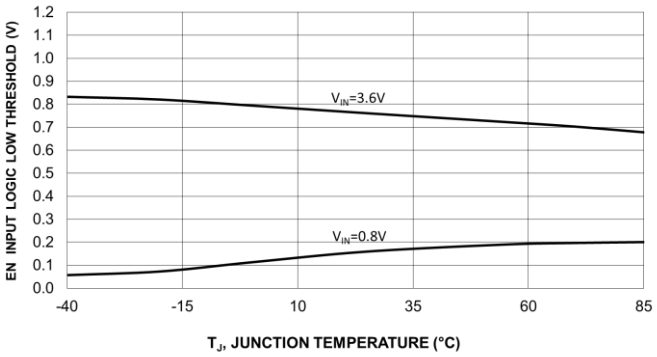


Figure 51. EN Input Logic Low Threshold Vs. Temperature

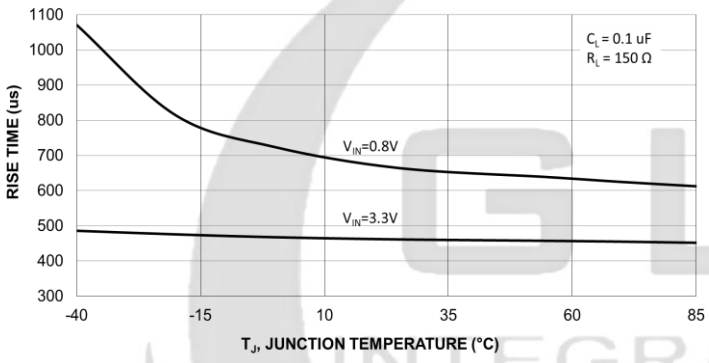


Figure 12. V_{OUT} Rise Time vs. Temperature

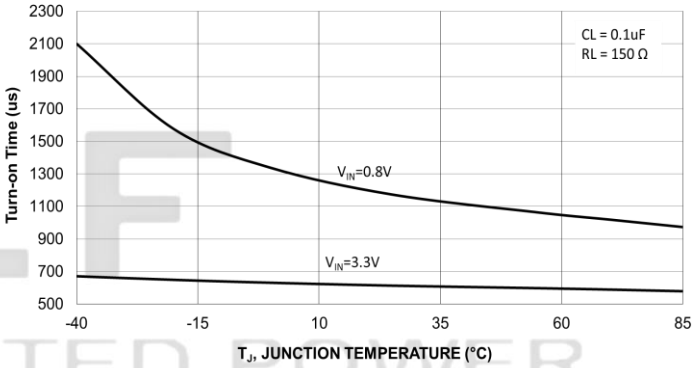


Figure 63. Turn-On Time vs. Temperature

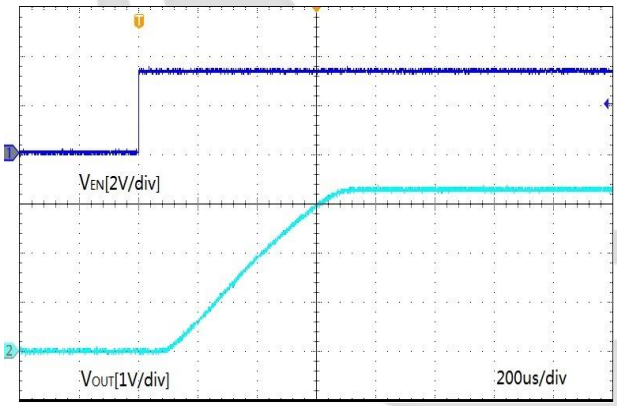


Figure 14. Turn-On Response
V_{IN} = 3.3 V, C_{OUT} = 0.1 uF, R_L = 150 Ω

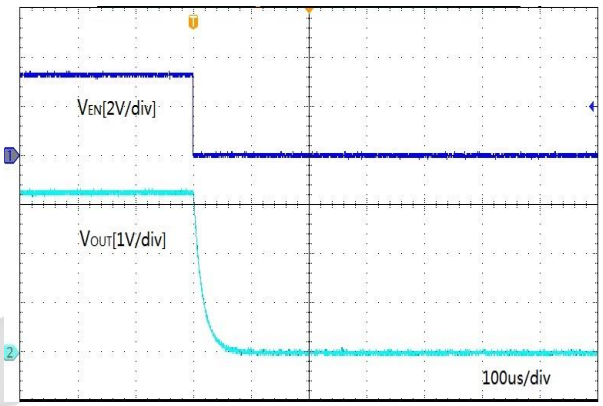


Figure 75. Turn-Off Response, GLF72511
V_{IN} = 3.3 V, C_{OUT} = 0.1 uF, R_L = 150 Ω

APPLICATION INFORMATION

The GLF72510 / GLF72511 is a fully integrated 3 A NMOS load switch with fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 0.8 V to 3.6 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current, avoiding unwanted standby current from the input power supply. The GLF72510 is available in the 0.97 mm x 0.97 mm x 0.55mm wafer level chip scale package with four bumps at 0.5 mm pitch to save space in compact applications.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

Reverse Current Blocking

The GLF72510 / GLF72511 has a built-in reverse current blocking protection. When the device is disabled, the reverse current blocking protection is activated to prevent the reverse current from the Vout to the Vin source.

EN pin

The GLF72510 / GLF72511 can be activated by EN pin high. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller.

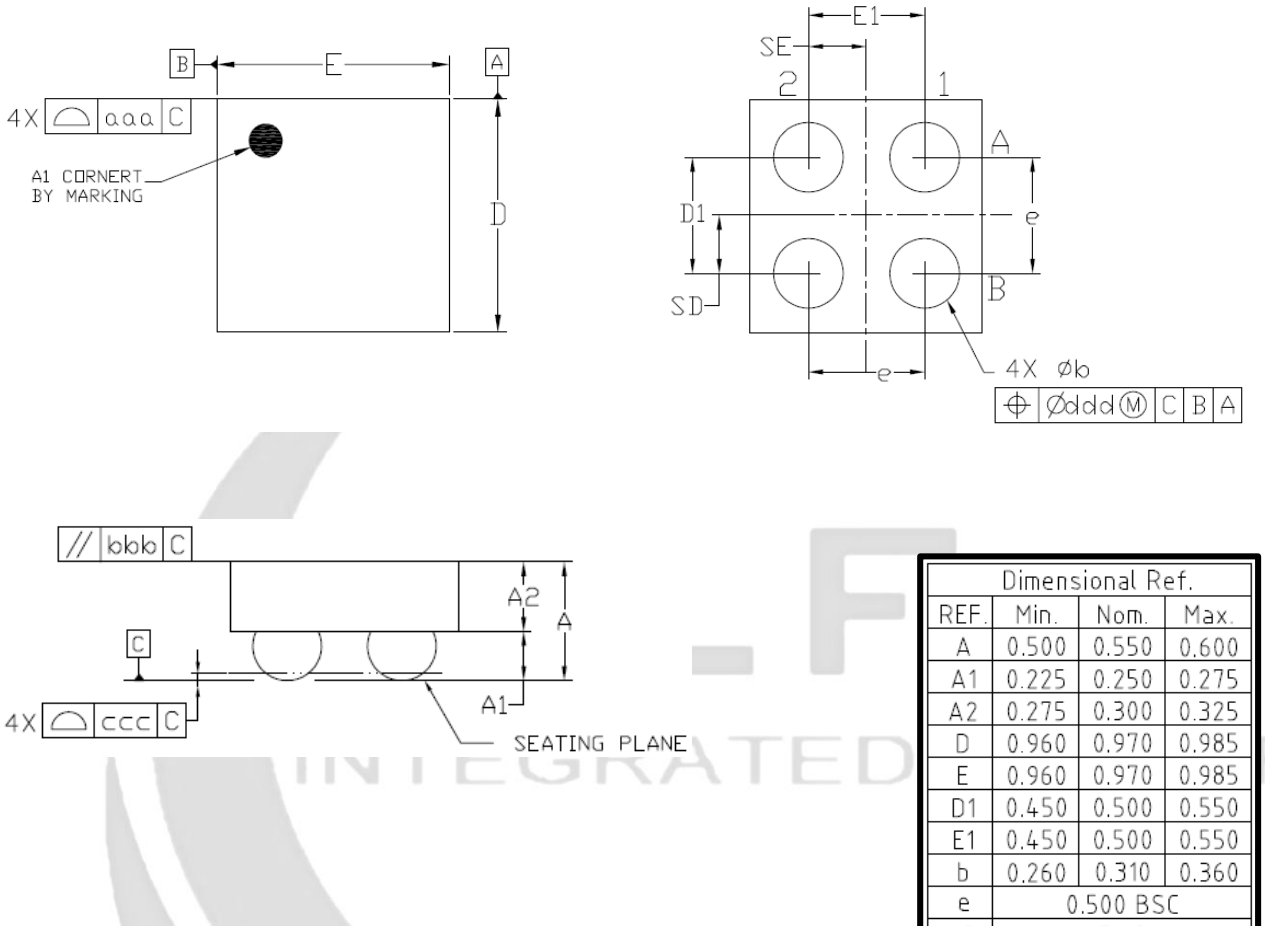
Output Discharge Function

The GLF72511 has an internal discharge N-channel FET switch on the VOUT node. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.

PACKAGE OUTLINE



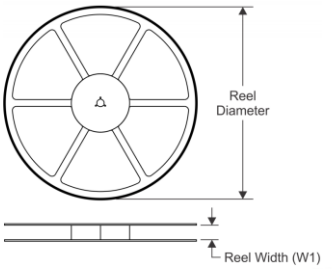
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.275	0.300	0.325
D	0.960	0.970	0.985
E	0.960	0.970	0.985
D1	0.450	0.500	0.550
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.250 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

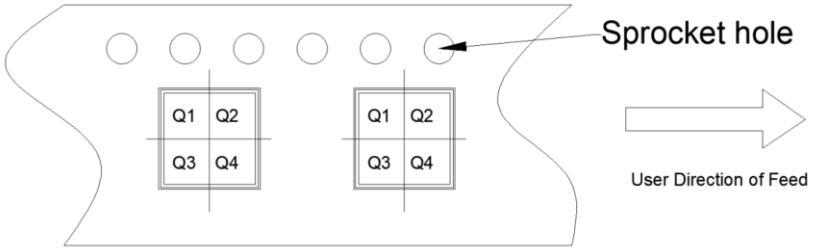
1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

TAPE AND REEL INFORMATION

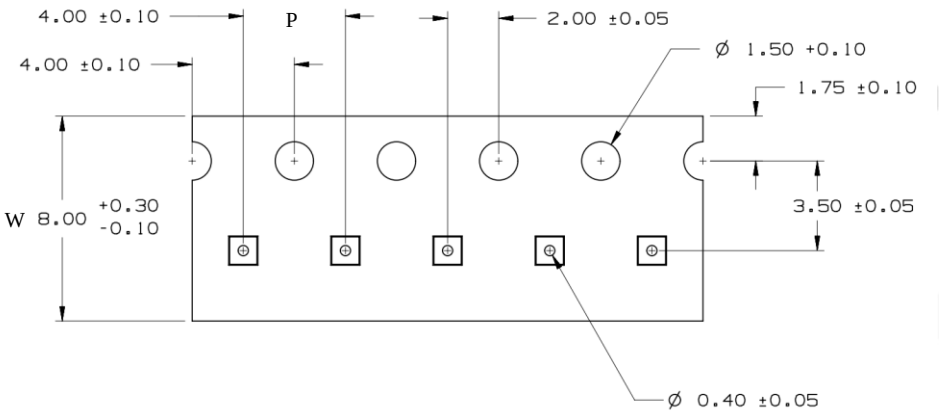
REEL DIMENSIONS

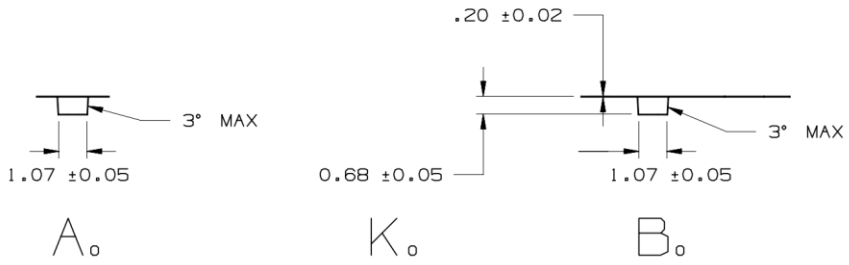


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF72510	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1
GLF72511	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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