

DESCRIPTION

The GLF72520 / GLF72524 Load Switch is a fully integrated 4 A NMOS load switch with I_QSmart™ advanced technology. The device is targeted for the mobile computing and data storage markets as a high performance, low cost solution for load switch applications.

The GLF72520 / GLF72524 has a constant low on-resistance of 10 mΩ at room temperature and a supply current consumption of less than 100 nA at lower input voltages. The fixed rise time helps prevent undesirable inrush current when turned on and the internal EN pin pulldown resistor ensures the device remains in the shutdown mode when disabled. In shutdown mode the GLF72520 / GLF72524 draws only 7 nA typical at 3.6 V input supply voltage.

The GLF72520 / GLF72524 features a reverse current blocking protection. When the GLF72520 / GLF72524 is disabled, it prevents reverse current flowing from the output to the input source.

The GLF72520 / GLF72524 is available in a wafer level chip scale package (WLCSP) measuring 0.97 mm x 1.47 mm x 0.55 mm with a 0.5 mm pitch. This allows the user to save board space and increase cost savings.

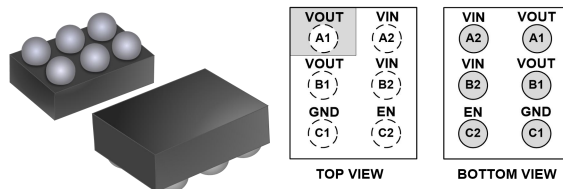
FEATURES

- Supply Voltage Range: 0.8 V to 3.6 V
- Low R_{ON}: 10 mΩ Typ
- I_{OUT} Max: 4 A
- Ultra-Low I_Q:
 - 60 nA Typ at 0.8 V_{IN}
 - 65 nA Typ at 1.0 V_{IN}
 - 70 nA Typ at 1.2 V_{IN}
- GLF72520 V_{OUT} Rise Time
 - 1150 μs at 0.8 V_{IN}
 - 800 μs at 3.3 V_{IN}
 - 780 μs at 3.6 V_{IN}
- GLF72524 V_{OUT} Rise Time
 - 460 μs at 0.8 V_{IN}
 - 280 μs at 3.3 V_{IN}
 - 280 μs at 3.6 V_{IN}
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch: GLF72524
- Reverse Current Blocking Protection When Disabled
- Operating Temperature Range: - 40 to 85 °C
- HBM: 6 kV, CDM: 2 kV
- 0.97 mm x 1.47 mm x 0.55 mm, 6 Bumps Wafer Level Chip Scale Package

APPLICATIONS

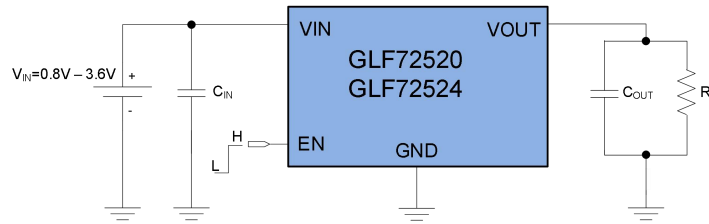
- Data Storage, SSD
- Wearables
- Low Power Subsystems

PACKAGE



0.97 mm x 1.47 mm x 0.55 mm, 0.5 mm Pitch

APPLICATION DIAGRAM



DEVICE ORDERING INFORMATION

Part Number	Top Mark	R _{ON} Typ. at Vin Range	Output Discharge	EN Activity
GLF72520	AS	10 mΩ	No	High
GLF72524	DJ		85 Ω	

FUNCTIONAL BLOCK DIAGRAM

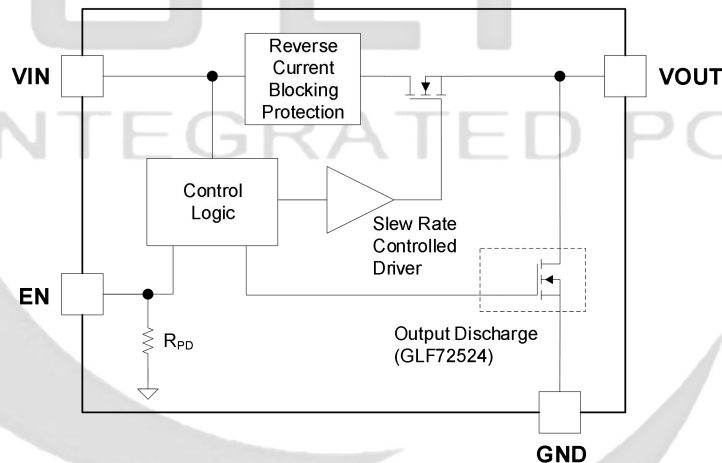
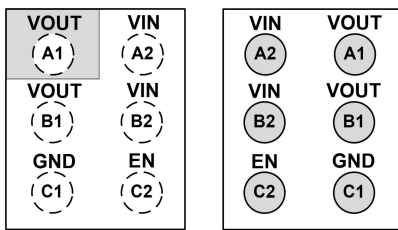


Figure 1. Functional Block Diagram

PIN CONFIGURATION

PIN DEFINITION



TOP VIEW

BOTTOM VIEW

Pin #	Name	Description
A1, B1	VOUT	Switch Output
A2, B2	VIN	Switch Input. Supply Voltage for IC
C1	GND	Ground
C2	EN	Enable to control the switch

Figure 2. 0.97 mm x 1.47 mm x 0.55 mm WLCSP

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
VIN, VOUT, EN	Each Pin Voltage Range to GND	-0.3	4	V
I _{OUT}	Maximum Continuous Switch Current		4	A
P _D	Power Dissipation at T _A = 25°C		1.2	W
T _{STG}	Storage Junction Temperature	-65	150	°C
T _A	Operating Temperature Range	-40	85	°C
θ _{JA}	Thermal Resistance, Junction to Ambient		85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6	kV
		Charged Device Model, JESD22-C101	2	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIN	Supply Voltage	0.8	3.6	V
T _A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

$V_{IN} = 0.8\text{ V to }3.6\text{ V}$ and $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units		
Basic Operation								
I_Q	Quiescent Current	EN = Enable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 0.8\text{ V}$		60		nA		
		EN = Enable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 1.0\text{ V}$		65				
		EN = Enable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 1.2\text{ V}$		70				
		I_Q	Quiescent Current	EN = Enable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 2.5\text{ V}$		2.5		μA
				EN = Enable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 3.0\text{ V}$		3.5		
				EN = Enable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 3.3\text{ V}$		5.5		
				EN = Enable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 3.6\text{ V}$		6.5		
				EN = Enable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 3.6\text{ V}$, $T_A = 85\text{ }^\circ\text{C}$		28		
I_{SD}	Shutdown Current	EN = Disable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 0.8\text{ V}$		4	20	nA		
		EN = Disable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 1.0\text{ V}$		4				
		EN = Disable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 1.2\text{ V}$		4	20			
		EN = Disable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 2.5\text{ V}$		5				
		EN = Disable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 3.0\text{ V}$		6				
		EN = Disable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 3.3\text{ V}$		6	25			
		EN = Disable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 3.6\text{ V}$		7	25			
		EN = Disable, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 3.6\text{ V}$, $T_A = 85\text{ }^\circ\text{C}$		660				
R_{ON}	On-Resistance	$V_{IN} = 0.8\text{ V to }3.6\text{ V}$	$T_A = 25\text{ }^\circ\text{C}$	10	13	m Ω		
		$I_{OUT} = 300\text{ mA}$	$T_A = 85\text{ }^\circ\text{C}$	14				
R_{DSC}	Output Discharge Resistance, GLF72524 Only	EN=Low, $I_{FORCE} = 10\text{ mA}$		85		Ω		
V_{IH}	EN Input Logic High Voltage	$V_{IN} = 0.8\text{ V} - 1.5\text{ V}$		0.9		V		
		$V_{IN} = 1.5\text{ V} - 3.6\text{ V}$		1.1		V		
V_{IL}	EN Input Logic Low Voltage	$V_{IN} = 0.8\text{ V} - 1.5\text{ V}$			0.15	V		
		$V_{IN} = 1.5\text{ V} - 3.6\text{ V}$			0.4	V		
R_{EN}	EN pull down resistance	EN=3.3 V		10		M Ω		

ELECTRICAL CHARACTERISTICS
 $V_{IN} = 0.8\text{ V to }3.6\text{ V}$ and $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Characteristics ⁽¹⁾, GLF72520						
t_{dON}	Turn-On Delay $R_{OUT} = 150\ \Omega, C_{OUT} = 1.0\ \mu\text{F}$	$V_{IN}=0.8\text{ V}$		880		μs
		$V_{IN}=1.0\text{ V}$		600		
		$V_{IN}=1.2\text{ V}$		540		
		$V_{IN}=2.5\text{ V}$		320		
		$V_{IN}=3.3\text{ V}$		270		
		$V_{IN}=3.6\text{ V}$		250		
t_R	V_{OUT} Rise Time $R_{OUT} = 150\ \Omega, C_{OUT} = 1.0\ \mu\text{F}$	$V_{IN}=0.8\text{ V}$		1150		μs
		$V_{IN}=1.0\text{ V}$		900		
		$V_{IN}=1.2\text{ V}$		990		
		$V_{IN}=2.5\text{ V}$		770		
		$V_{IN}=3.3\text{ V}$		800		
		$V_{IN}=3.6\text{ V}$		780		
t_{dOFF}	Turn-Off Delay $R_{OUT} = 150\ \Omega, C_{OUT} = 1.0\ \mu\text{F}$	$V_{IN}=0.8\text{ V}$		140		μs
		$V_{IN}=1.0\text{ V}$		25		
		$V_{IN}=1.2\text{ V}$		15		
		$V_{IN}=2.5\text{ V}$		14		
		$V_{IN}=3.3\text{ V}$		12		
		$V_{IN}=3.6\text{ V}$		12		
t_F	V_{OUT} Fall Time $R_{OUT} = 150\ \Omega, C_{OUT} = 1.0\ \mu\text{F}$	$V_{IN}=0.8\text{ V}$		290		μs
		$V_{IN}=1.0\text{ V}$		300		
		$V_{IN}=1.2\text{ V}$		300		
		$V_{IN}=2.5\text{ V}$		310		
		$V_{IN}=3.3\text{ V}$		350		
		$V_{IN}=3.6\text{ V}$		350		
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Characteristics ⁽¹⁾, GLF72524						
t_{dON}	Turn-On Delay $R_{OUT} = 150\ \Omega, C_{OUT} = 1.0\ \mu\text{F}$	$V_{IN}=0.8\text{ V}$		450		μs
		$V_{IN}=1.0\text{ V}$		270		
		$V_{IN}=1.2\text{ V}$		220		
		$V_{IN}=2.5\text{ V}$		130		
		$V_{IN}=3.3\text{ V}$		110		
		$V_{IN}=3.6\text{ V}$		100		
t_R	V_{OUT} Rise Time $R_{OUT} = 150\ \Omega, C_{OUT} = 1.0\ \mu\text{F}$	$V_{IN}=0.8\text{ V}$		460		μs
		$V_{IN}=1.0\text{ V}$		350		
		$V_{IN}=1.2\text{ V}$		345		
		$V_{IN}=2.5\text{ V}$		310		
		$V_{IN}=3.3\text{ V}$		280		
		$V_{IN}=3.6\text{ V}$		280		

t_{dOFF}	Turn-Off Delay $R_{OUT} = 150 \Omega, C_{OUT} = 1.0 \mu F$	$V_{IN} = 0.8 V$	100	μs
		$V_{IN} = 1.0 V$	20	
		$V_{IN} = 1.2 V$	12	
		$V_{IN} = 2.5 V$	5	
		$V_{IN} = 3.3 V$	5	
		$V_{IN} = 3.6 V$	5	
t_F	V_{OUT} Fall Time $R_{OUT} = 150 \Omega, C_{OUT} = 1.0 \mu F$	$V_{IN} = 0.8 V$	270	μs
		$V_{IN} = 1.0 V$	190	
		$V_{IN} = 1.2 V$	140	
		$V_{IN} = 2.5 V$	130	
		$V_{IN} = 3.3 V$	130	
		$V_{IN} = 3.6 V$	130	

Notes: 1. By design; characterized, not production tested. $t_{ON} = t_{dON} + t_r$, $t_{OFF} = t_{dOFF} + t_f$

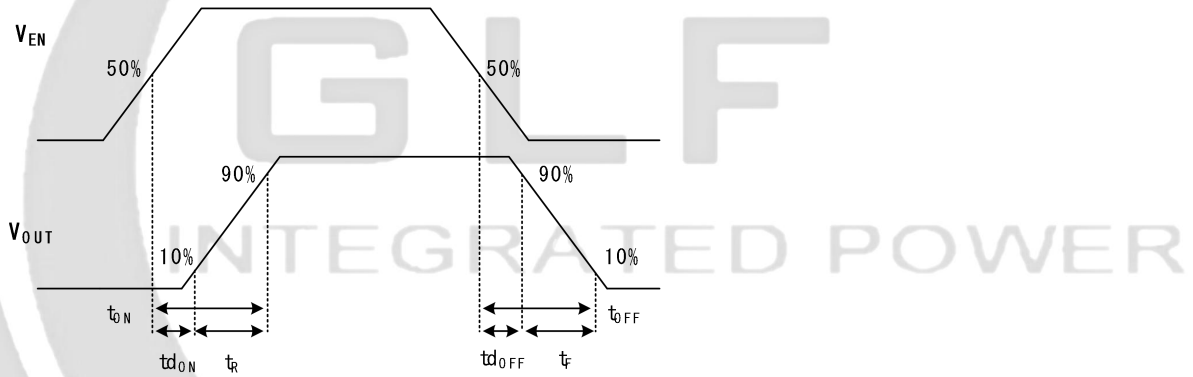


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

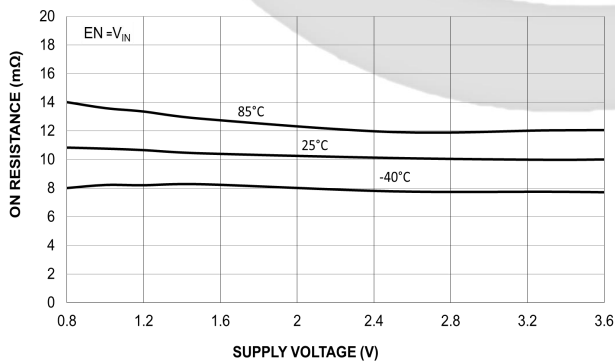


Figure 4. On-Resistance vs. Supply Voltage

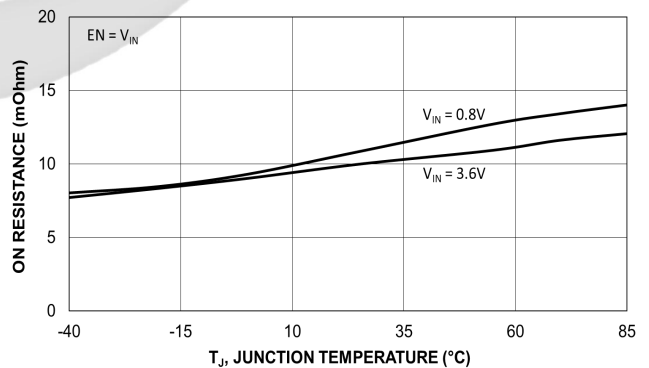


Figure 5. On-Resistance vs. Temperature

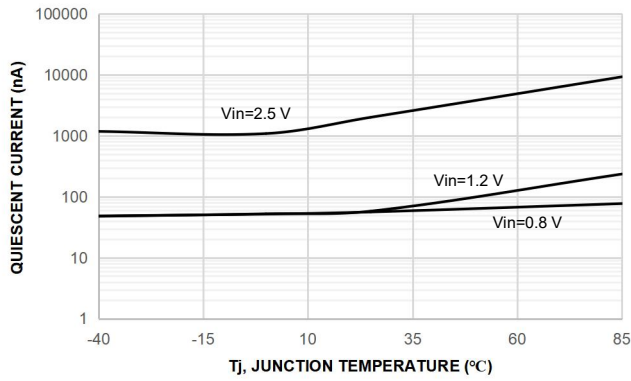


Figure 6. Quiescent Current vs. Temperature

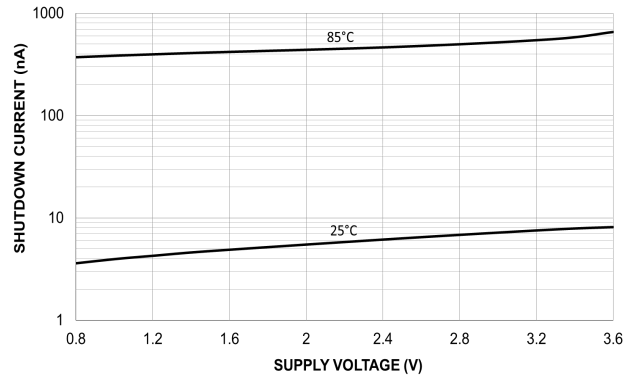


Figure 7. Shutdown Current vs. Supply Voltage

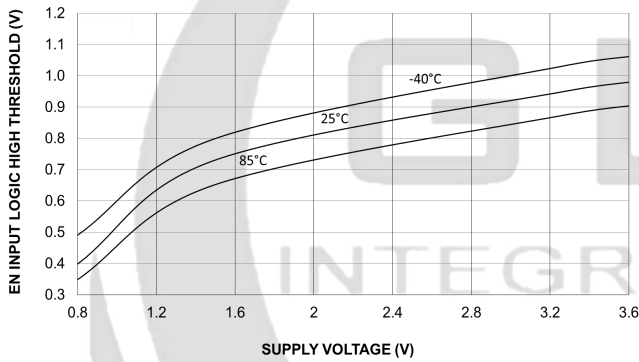


Figure 8. EN Input Logic High Threshold

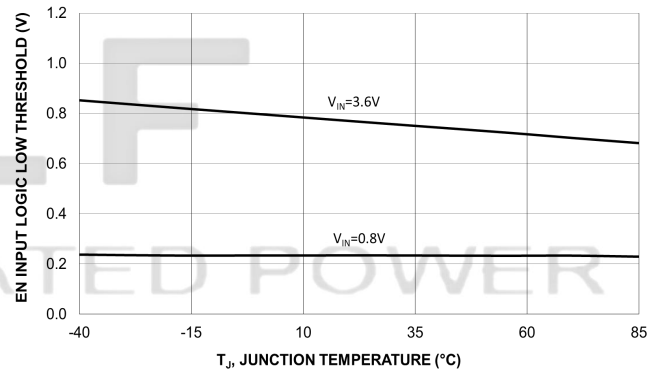


Figure 9. EN Input Logic High Threshold Vs. Temperature

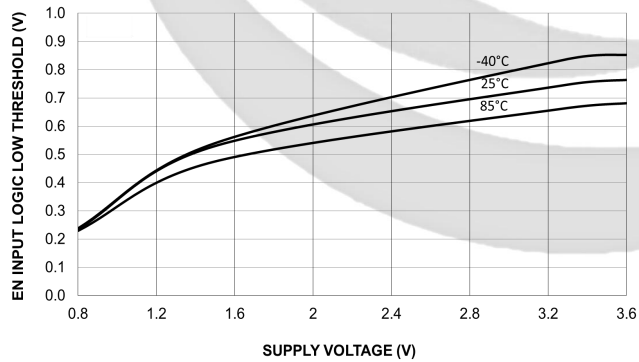


Figure 10. EN Input Logic Low Threshold

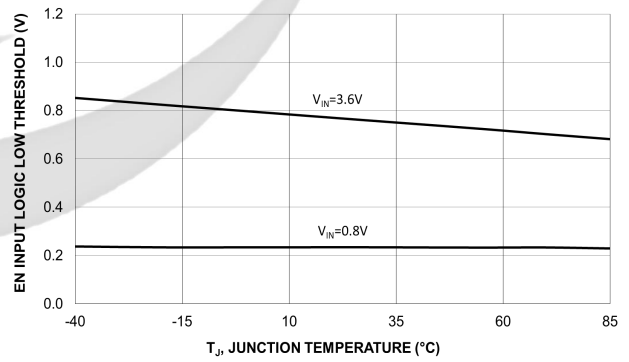


Figure 11. EN Input Logic Low Threshold Vs. Temperature

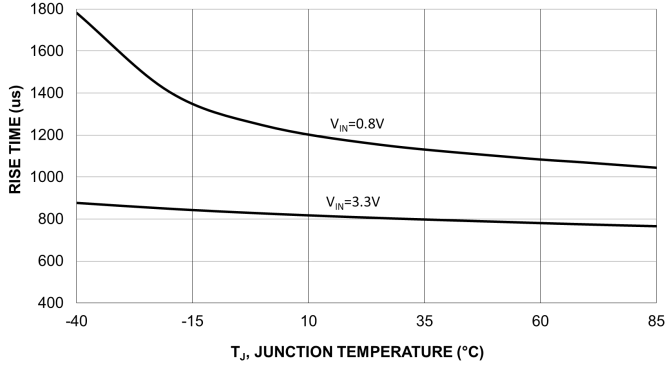


Figure 12. V_{OUT} Rise Time vs. Temperature, GLF72520

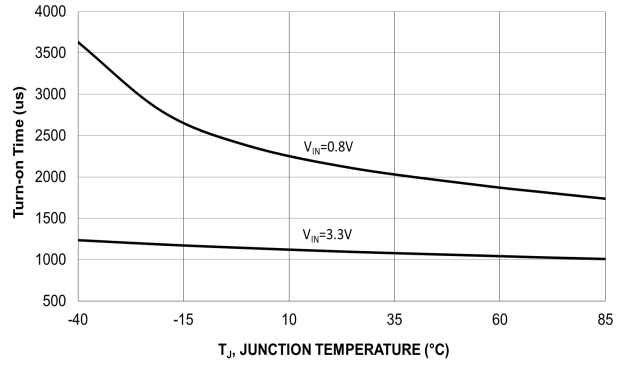


Figure 13. Turn-On Time vs. Temperature, GLF72520

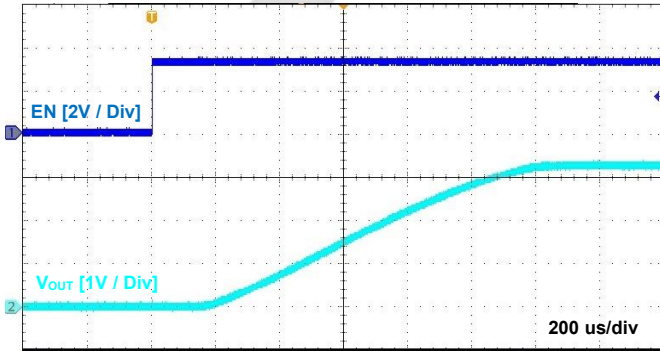


Figure 14. Turn-On Response, GLF72520
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

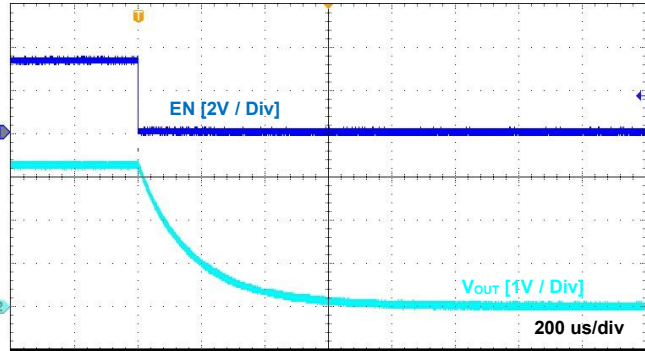


Figure 15. Turn-Off Response, GLF72520
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

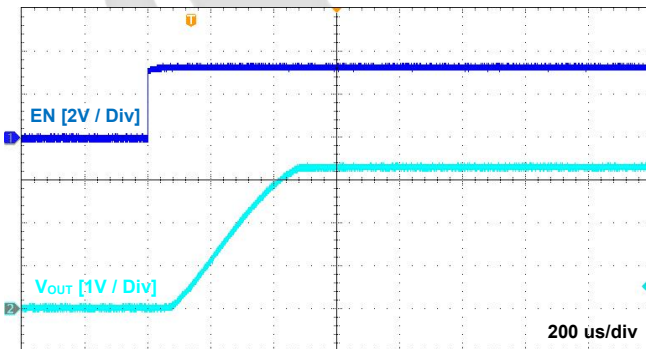


Figure 14. Turn-On Response, GLF72524
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

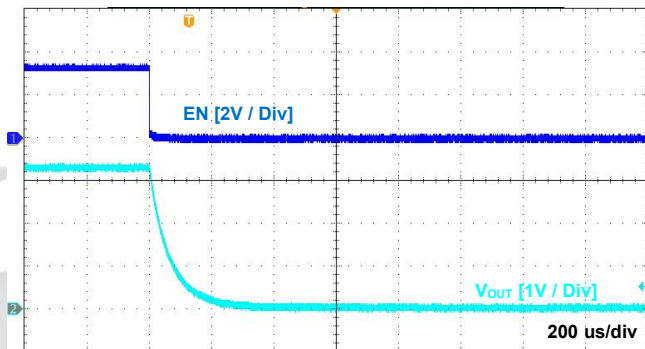


Figure 15. Turn-Off Response, GLF72524
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

APPLICATION INFORMATION

The GLF72520 / GLF72524 is a fully integrated 4 A NMOS load switch with fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 0.8 V to 3.6 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current, avoiding unwanted standby current from the input power supply. The GLF72520 / GLF72524 is available in the 0.97 mm x 1.47 mm wafer level chip scale package with 6 bumps at 0.5 mm pitch to save space in compact applications.

Input Capacitor

A capacitor is recommended to be placed close to the VIN pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

Reverse Current Blocking

The GLF72520 / GLF72524 has a built-in reverse current blocking protection. When the device is disabled, the reverse current blocking protection is activated to prevent the reverse current from the VOUT to the VIN source.

EN pin

The GLF72520 / GLF72524 can be activated by EN pin high. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller.

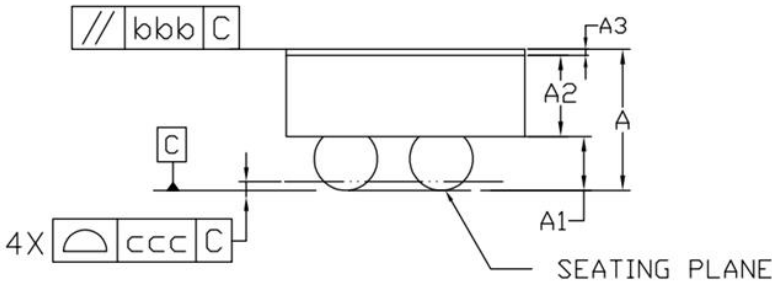
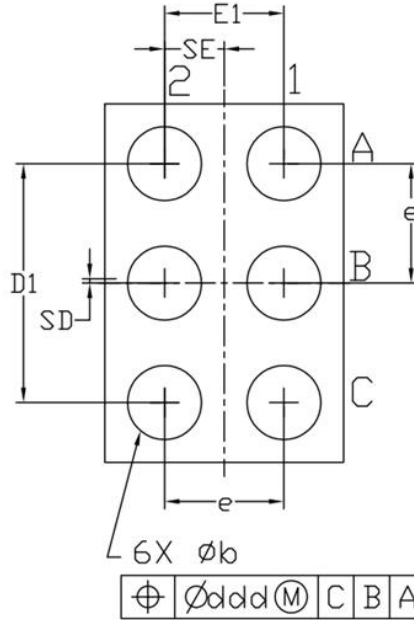
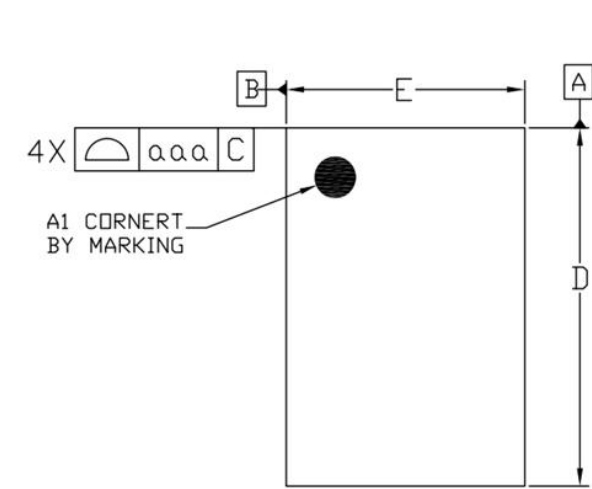
Output Discharge Function

The GLF72524 has an internal discharge N-channel FET switch on the VOUT node. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

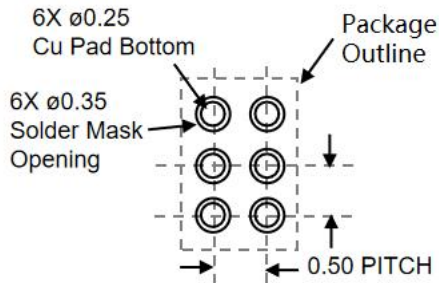
Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.

WLCSP PACKAGE OUTLINE



Recommended Footprint



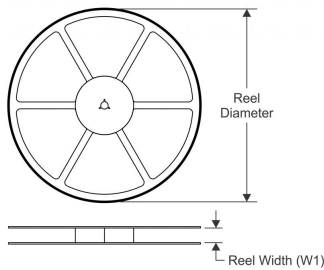
Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

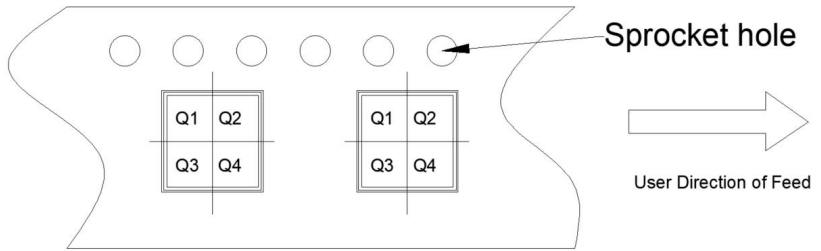
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	1.460	1.470	1.485
E	0.960	0.970	0.985
D1	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.000 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

TAPE AND REEL INFORMATION

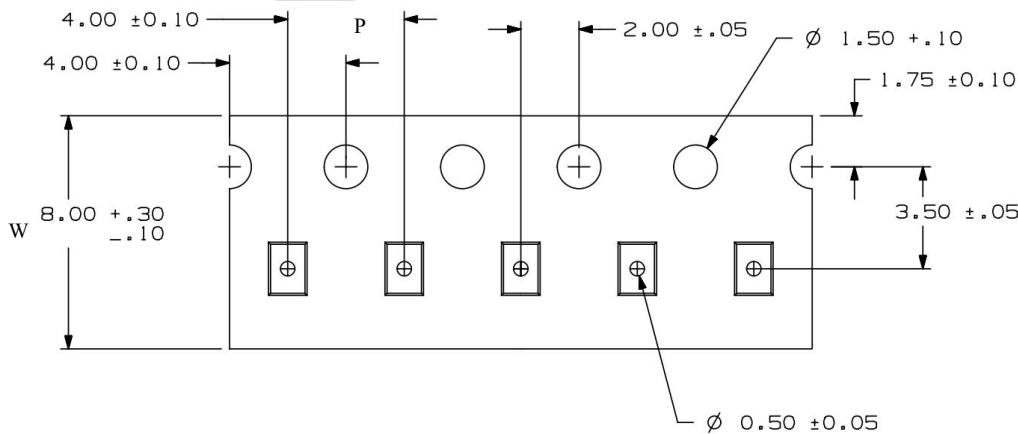
REEL DIMENSIONS



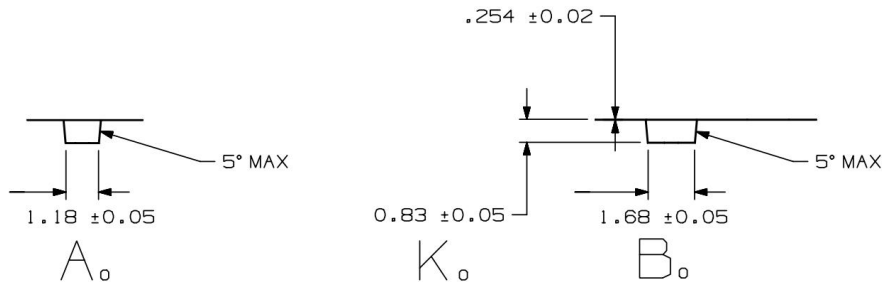
QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



POWER



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF72520	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1
GLF72524	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

DISCLAIMERS

Information in this document is believed to be accurate and reliable, however GLF assumes no liability for errors or omissions. Device performance may be impacted by testing methods and application use cases. Users are responsible to independently evaluate the applicability, usability, and suitability of GLF devices in their application. In no case will GLF be liable for incidental, indirect, or consequential damages associated with the use, mis-use, or sale of its product. Customers are wholly responsible to assure GLF devices meet their system level and end product requirements. GLF retains the right to change the information provided in this data sheet without notice.