# GLF72100, GLF72101, GLF72102, GLF72103, GLF72105, GLF72106



Nano Current Leakage I<sub>Q</sub>Smart<sup>™</sup> Load Switch with Reverse Current Blocking Protection

**Product Specification** 

#### DESCRIPTION

The GLF7210x product family is an advanced technology fully integrated  $I_QSmart^{TM}$  load switch device with reverse current blocking (RCB) protection and slew rate control of the output voltage.

The GLF7210x product family offers industry leading reverse current blocking (RCB) protection performance, featuring an ultra-low threshold voltage. The GLF7210x product family minimizes reverse current flow in the event that the VOUT voltage exceeds the VIN voltage.

The GLF7210x product family has an industry leading power efficiency. The GLF7210x product family features an on-resistance ( $R_{ON}$ ) as low as 37 m $\Omega$  typical at 5.5 V, reducing power loss during conduction. The GLF7210x product family also features ultra-low shutdown current ( $I_{SD}$ ) to reduce power loss and battery drain in the off state. When EN is pulled low, and the output is grounded, the GLF7210x product family can achieve an  $I_{SD}$  as low as 20 nA typical at 5.5 V.

The GLF7210x product family of load switch device supports an industry leading wide input voltage range that helps to improve system operating life and overall performance. One GLF7210x device can be used in multiple voltage rail applications which helps mitigate inventory management and reduces BOM cost.

The GLF7210x product family utilizes a chip scale package with 4 bumps in a 0.77 mm x 0.77 mm x 0.46 mm die size and a 0.4 mm pitch.

#### **FEATURES**

Wide Input Range: 1.5 V to 5.5 V

6 V<sub>abs</sub> max

• Ultra-Low  $I_Q$ : 0.45  $\mu A$  Typ at 5.5  $V_{IN}$ 

Ultra-Low I<sub>SD</sub>: 20 nA Typ at 5.5 V<sub>IN</sub>

• Low R<sub>ON</sub>: 37 mΩ Typ at 5.5 V<sub>IN</sub>

I<sub>OUT</sub> Max: 2 A

• Reverse Current Blocking Protection

• Controlled V<sub>OUT</sub> Rise Time

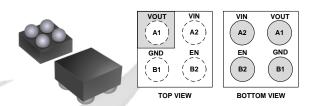
• Internal EN Pull-up/down Resistor on EN Pin

 Integrated Output Discharge Switch: GLF72101, GLF72103, GLF72105

## **APPLICATIONS**

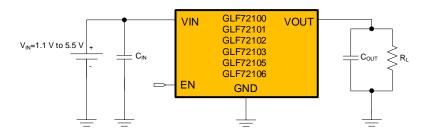
- Portable Devices
- Wearable Devices
- Low Power Subsystems
- Smart IoT Devices

# **PACKAGE**



0.77 mm x 0.77 mm x 0.46 mm WLCSP

#### **APPLICATION DIAGRAM**





## **ALTERNATE DEVICE OPTIONS**

Part Number	Top Mark	R <sub>on</sub> (Typ) at 5.5 V	Output Discharge	V <sub>OUT</sub> Rise Time t <sub>R</sub> (Typ) at 3.3 V	EN Activity	Package
GLF72100	J		NA		High	WLCSP
GLF72101	F		85 Ω 570 μs <i>NA</i>		570 μs High W	
GLF72102 *	K				Low	WLCSP
GLF72103	М	37 mΩ	85 Ω	48 µs	High	WLCSP with Backside Laminate
GLF72105	N		85 Ω	900 110	Low	WLCSP with Backside Laminate
GLF72106	d		NA	890 µs	Low	WLCSP with Backside Laminate

Note: GLF72102 is upon request

## **FUNCTIONAL BLOCK DIAGRAM**

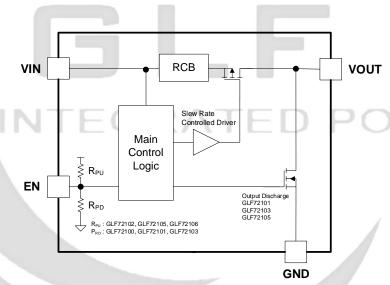
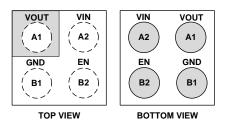


Figure 1. Functional Block Diagram

## **PIN CONFIGURATION**



## **PIN DEFINITION**

Pin#	Name	Description
A1	VOUT	Switch Output
A2	VIN	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch

Figure 2. 0.77 mm x 0.77 mm x 0.46 mm WLCSP

# GLF72100, GLF72101, GLF72102, GLF72103, GLF72105. GLF72106 Nano Current Leakage I<sub>Q</sub>Smart<sup>™</sup> Load Switch with RCB

# **ABSOLUTE MAXIMUM RATINGS**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	P	Min.	Max.	Unit	
VIN, VOUT, VEN	Each Pin Voltage Range to GND	-0.3	6	V	
Іоит	Maximum Continuous Switch Cu	rrent		2	Α
PD	Power Dissipation at T <sub>A</sub> = 25 °C		1.2	W	
TJ	Maximum Junction Temperature		150	°C	
T <sub>STG</sub>	Storage Junction Temperature	-65	150	°C	
TA	Ambient Operating Temperature	-40	85	°C	
θја	Thermal Resistance, Junction to Ambient			85	°C/W
ECD	Electrostatic Discharge	Human Body Model, JESD22-A114	±4		1417
ESD	Capability	Charged Device Model, JESD22-C101	±2		kV

# **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min.	Max.	Unit
VIN	Supply Voltage	1.5	5.5	V
TA	Ambient Operating Temperature	-40	+85	°C

INTEGRATED POW



# **ELECTRICAL CHARACTERISTICS**

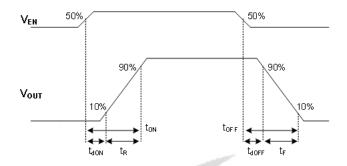
Values are at  $V_{IN} = 3.3 \text{ V}$  and  $T_A = 25 ^{\circ}\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	S	Min.	Тур.	Max.	Units
Basic Ope					, , , , , , , , , , , , , , , , , , ,		
•		EN = Enable, I <sub>OUT</sub> = 0 mA, V <sub>IN</sub> =	5.5 V		0.45	1	
ΙQ	Quiescent Current (1)	EN = Enable, I <sub>OUT</sub> = 0 mA, V <sub>IN</sub> = 5		0.5		μA	
		EN = Disable, lout= 0 mA, V <sub>IN</sub> = 1.5 V			5		
		EN = Disable, I <sub>OUT</sub> = 0 mA, V <sub>IN</sub> =		9		nA	
I <sub>SD</sub>	Shut Down Current	EN = Disable, lour= 0 mA, V <sub>IN</sub> =		12			
102		EN = Disable, I <sub>OUT</sub> = 0 mA, V <sub>IN</sub> =		20	100		
		EN = Disable, lour= 0 mA, V <sub>IN</sub> =			50		
			T <sub>A</sub> = 25 °C		37	42	
		V <sub>IN</sub> = 5.5 V, I <sub>OUT</sub> = 500 mA	$T_A = 85  ^{\circ}C^{(4)}$		43		
			T <sub>A</sub> = 25 °C		47	52	
Ron	On-Resistance	V <sub>IN</sub> = 3.3 V, I <sub>OUT</sub> = 500 mA	$T_A = 85  ^{\circ}C^{(4)}$		56	02	mΩ
		V <sub>IN</sub> = 1.8 V, I <sub>OUT</sub> = 300 mA	$T_A = 25  ^{\circ}C^{(4)}$		80		
		V <sub>IN</sub> = 1.5 V, I <sub>OUT</sub> = 100 mA	T <sub>A</sub> = 25 °C		100		
	Output Discharge	EN=Low, IFORCE= 10 mA for GLI	I .			<u> </u>	
Rosc	Resistance	EN=High , I <sub>FORCE</sub> = 10 mA for GL			85		Ω
V <sub>IH</sub>	EN Input Logic High Voltage	V <sub>IN</sub> = 1.5 V to 5.5 V		1.2			V
VIL	EN Input Logic Low Voltage	V <sub>IN</sub> = 1.5 V to 5.5 V			0.45	V	
Ren	EN Internal Resistance	Pull-down Resistance: GLF72100, G		10		ΜΩ	
		Pull-up Resistance: GLF72102, GLF					
I <sub>EN</sub>	EN Current	V <sub>EN</sub> = V <sub>IN</sub> or GND		0.5		μA	
$V_{RCB\_TH}$	RCB Protection Threshold Voltage	V <sub>OUT</sub> – V <sub>IN</sub>		25	F	mV	
V <sub>RCB_RL</sub>	RCB Protection Release Voltage	V <sub>IN</sub> - V <sub>OUT</sub>			30		mV
Switching	Characteristics (2): GLF721	00, GLF72101					
t <sub>dON</sub>	Turn-On Delay	R <sub>L</sub> = 150 Ω, C <sub>OUT</sub> = 0.1 μF, GLF7	2100 GL F72101		430		
t <sub>R</sub>	Vout Rise Time	ΝΕ= 130 Ω, Οθη= 0.1 μι , ΘΕΙ Τ	2100, OLI 72101		570		
tdOFF	Turn-Off Delay (3), (4)	R <sub>L</sub> = 150 Ω, C <sub>OUT</sub> = 0.1 μF, GLF7	2100		17		1
t⊧	Vout Fall Time (3), (4)	KL= 150 Ω, Cou1= 0.1 μF, GLF7	2100		30		μs
tdOFF	Turn-Off Delay (3), (4)	R <sub>L</sub> = 150 Ω, C <sub>OUT</sub> = 0.1 μF, GLF7	2101		17		
t⊧	Vout Fall Time (3), (4)	KL= 150 Ω, Cou1= 0.1 μF, GLF7.	2101		15		
Switching	Characteristics (2): GLF721	03					
t <sub>dON</sub>	Turn-On Delay				50		
t <sub>R</sub>	V <sub>OUT</sub> Rise Time	R <sub>L</sub> = 150 Ω, C <sub>OUT</sub> = 0.1 μF			48		110
tdOFF	Turn-Off Delay (3), (4)	Ν 130 Ω, Οουτ= 0.1 μΓ			17		μs
t <sub>F</sub>	Vout Fall Time (3), (4)				15		<u></u>
Switching	Characteristics (2): GLF721	05					
t <sub>dON</sub>	Turn-On Delay				640		
t <sub>R</sub>	V <sub>OUT</sub> Rise Time	B. = 150 O. C 0.1			890		
<b>t</b> dOFF	Turn-Off Delay (3), (4)	$R_L = 150 \Omega$ , $C_{OUT} = 0.1 \mu F$		16		μs	
t⊧	Vout Fall Time (3), (4)			10			
Switching	Characteristics (2): GLF721	06					
t <sub>dON</sub>	Turn-On Delay				640		
t <sub>R</sub>	V <sub>OUT</sub> Rise Time	B 450 0 0 04 .:E			890		.,,-
t <sub>dOFF</sub>	Turn-Off Delay (3), (4)	R <sub>L</sub> = 150 Ω, C <sub>OUT</sub> = 0.1 μF			17		μs
t <sub>F</sub>	V <sub>OUT</sub> Fall Time (3), (4)			30			
Votes.		e null down current (I) through the r	J. E7040	VC === d CI	F70400	3	

Notes:

- 1. I<sub>Q</sub> does not include the enable pull down current (I<sub>EN</sub>) through the pull-down resistor R<sub>EN</sub> of GLF72105 and GLF72106.
- 2.  $t_{ON} = t_{dON} + t_R$ ,  $t_{OFF} = t_{dOFF} + t_F$
- 3. Output discharge path is enabled during off.
- 4. By design; characterized, not production tested.

#### **TIMING DIAGRAM**



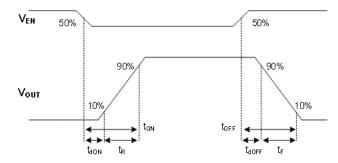
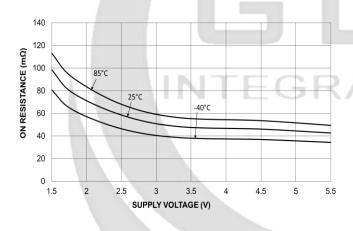


Figure 3. GLF72100, GLF72101 and GLF72103

Figure 4. GLF72102, GLF72105 and GLF72106

# TYPICAL PERFORMANCE CHARACTERISTICS



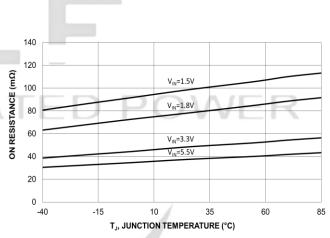


Figure 5. On-Resistance vs. Supply Voltage

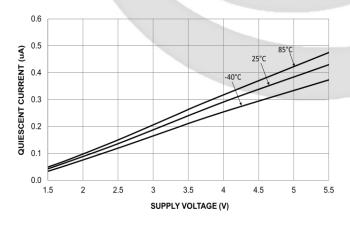


Figure 6. On-Resistance vs. Temperature

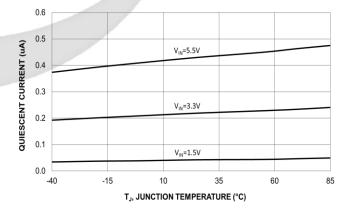
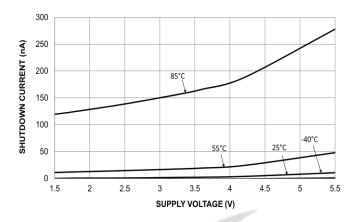


Figure 7. Quiescent Current vs. Supply Voltage

Figure 8. Quiescent Current vs. Temperature



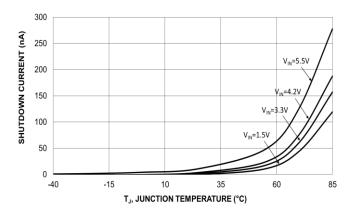
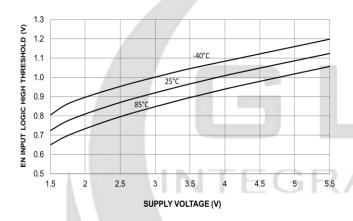


Figure 9. Shutdown Current vs. Supply Voltage

Figure 10. Shutdown Current vs. Temperature



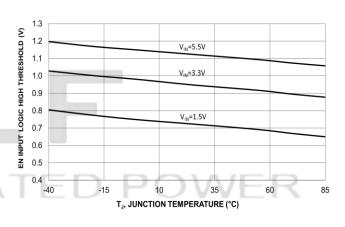
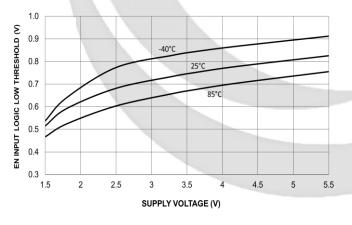


Figure 11. EN Input Logic High Threshold

Figure 12. EN Input Logic High Threshold Vs. Temperature



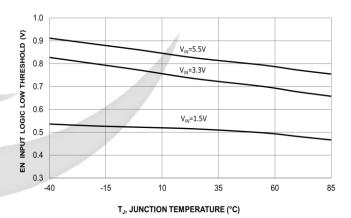


Figure 13. EN Input Logic Low Threshold

Figure 14. EN Input Logic Low Threshold Vs. Temperature



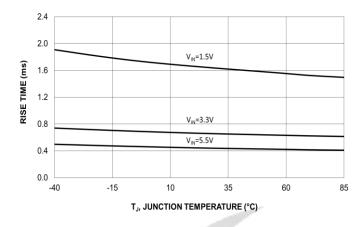


Figure 15. V<sub>OUT</sub> Rise Time vs. Temperature GLF72100 and GLF72101

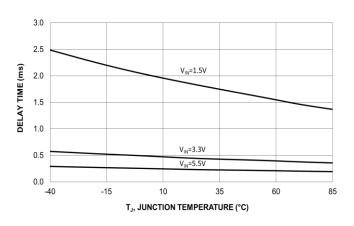


Figure 16. Turn-On Delay Time vs. Temperature GLF72100 and GLF72101

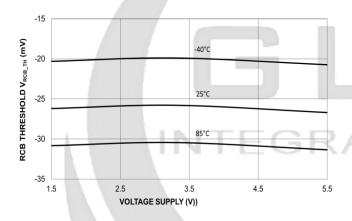


Figure 17. RCB Threshold Voltage vs. Supply Voltage

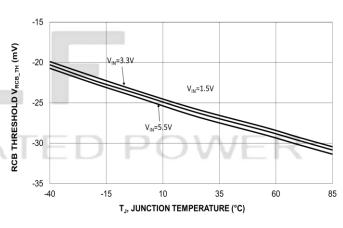


Figure 18. RCB Threshold Voltage vs. Temperature

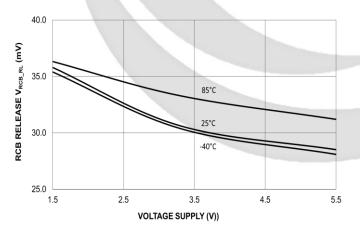


Figure 19. RCB Release Voltage vs. Supply Voltage

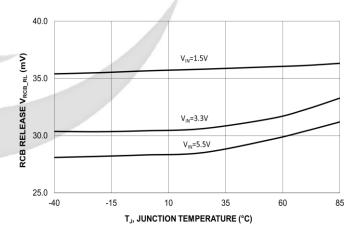


Figure 20. RCB Release Voltage vs. Temperature

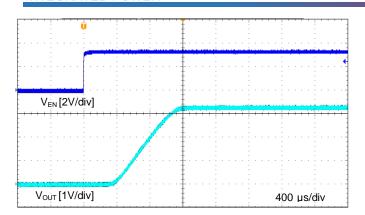


Figure 21. Turn-On Response, GLF72100  $V_{\text{IN}=3.3} \text{ V, C}_{\text{IN}=0.1} \text{ } \mu\text{F, C}_{\text{OUT}=0.1} \text{ } \mu\text{F, R}_{\text{L}=150} \text{ } \Omega$ 

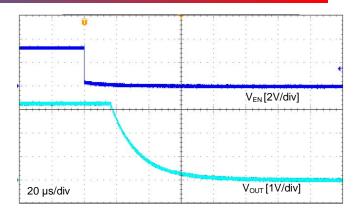


Figure 22. Turn-Off Response, GLF72100, GLF72106  $V_{\text{IN}}$ =3.3 V,  $C_{\text{IN}}$ =0.1  $\mu\text{F}$ ,  $C_{\text{OUT}}$ =0.1  $\mu\text{F}$ ,  $R_{\text{L}}$ =150  $\Omega$ 

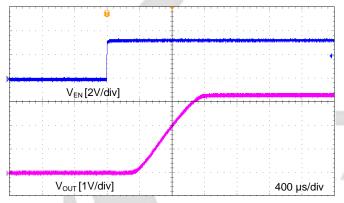


Figure 23. Turn-On Response, GLF72101  $V_{\text{IN}=3.3} \text{ V, C}_{\text{IN}=0.1} \text{ } \mu\text{F, C}_{\text{OUT}=0.1} \text{ } \mu\text{F, R}_{\text{L}=150} \text{ } \Omega$ 

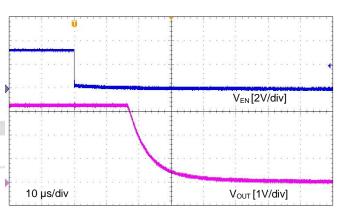


Figure 24. Turn-Off Response, GLF72101  $V_{\text{IN}}{=}3.3~V,~C_{\text{IN}}{=}0.1~\mu\text{F},~C_{\text{OUT}}{=}0.1~\mu\text{F},~R_{\text{L}}{=}150~\Omega$ 

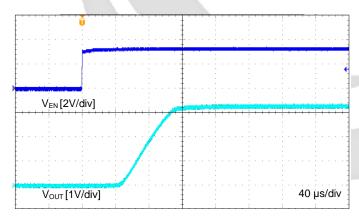


Figure 25. Turn-On Response, GLF72103  $V_{\text{IN}}{=}3.3~\text{V, C}_{\text{IN}}{=}0.1~\mu\text{F, C}_{\text{OUT}}{=}0.1~\mu\text{F, R}_{\text{L}}{=}150~\Omega$ 

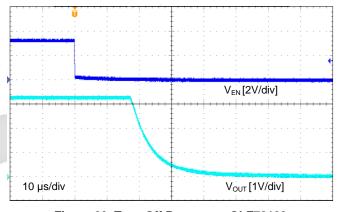


Figure 26. Turn-Off Response, GLF72103  $\label{eq:Vin=3.3} V_{\text{IN}=3.3} \; V, \; C_{\text{IN}=0.1} \; \mu\text{F}, \; C_{\text{OUT}=0.1} \; \mu\text{F}, \; R_{\text{L}=150} \; \Omega$ 

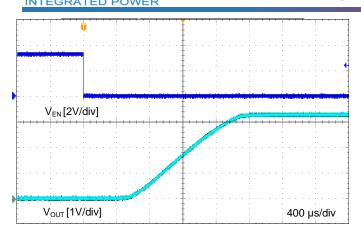


Figure 27. Turn-On Response, GLF72105, GLF72106  $V_{\text{IN}}{=}3.3 \text{ V, } C_{\text{IN}}{=}0.1 \text{ } \mu\text{F, } C_{\text{OUT}}{=}0.1 \text{ } \mu\text{F, } R_{\text{L}}{=}150 \text{ } \Omega$ 

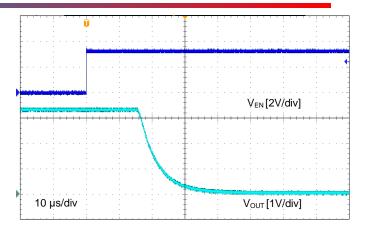


Figure 28. Turn-Off Response, GLF72105  $V_{\text{IN}=3.3} \text{ V, C}_{\text{IN}=0.1} \text{ } \mu\text{F, C}_{\text{OUT}=0.1} \text{ } \mu\text{F, R}_{\text{L}=150} \text{ } \Omega$ 

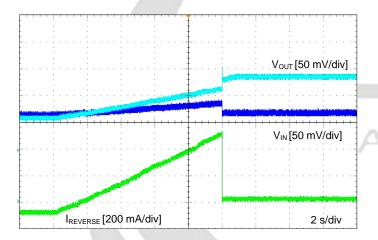


Figure 29. Reverse Current Blocking Threshold  $V_{\text{IN}}{=}3.3~\text{V},~V_{\text{OUT}}{=}\text{Up}$  to 3.4 V in  $C_{\text{IN}}{=}0.1~\mu\text{F},~C_{\text{OUT}}{=}0.1~\mu\text{F}$ 

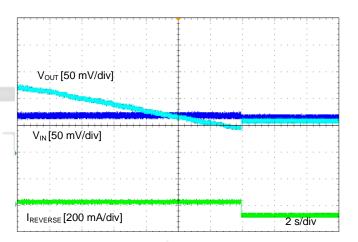


Figure 30. Reverse Current Blocking Release  $V_{IN}=3.3~V,~V_{OUT}=Down~to~3.2~V~in~C_{IN}=0.1~\mu F,~C_{OUT}=0.1~\mu F$ 

#### APPLICATION INFORMATION

The GLF7210x product family is an integrated 2 A, nano current leakage I<sub>Q</sub>Smart<sup>™</sup> load switches with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.5 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.77 mm x 0.77 mm x 0.46 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.4 mm pitch for manufacturability.

# **Input Capacitor**

The GLF7210x product family does not require an input capacitor. However, to reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1 µF capacitor is recommended to be placed close to the VIN pin. A higher input capacitor value can be used to further attenuate the input voltage drop.

## **Output Capacitor**

The GLF7210x product family does not require an output capacitor. However, use of an output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C<sub>OUT</sub> capacitor should be spaced close to the VOUT and GND pins.

#### **EN Pin**

The GLF72100, GLF72101, and GLF72103 can be activated by forcing EN pin high level and the GLF72102, GLF72105, GLF72106 by EN pin low level. Note that the EN pin has an internal pull-down/ pull-up resistor to help pull the main switch to a known "off state" when no EN signal is applied from an external controller.

# Reverse Current Blocking

The GLF7210x product family has a built-in reverse current blocking protection which always monitors the output voltage level regardless of the status of EN pin to check if it is greater than the input voltage. When the output voltage goes beyond the input voltage by 25 mV, that is the reverse current blocking protection threshold voltage ( $V_{RCB\_TH}$ ), the reverse current blocking function block turns off the switch. Note that some reverse current can occur until the  $V_{RCB\_TH}$  is triggered. The main switch will resume normal operation when the output voltage drops below the input source by the reverse current blocking protection release voltage ( $V_{RCB\_RL}$ ).

## **Output Discharge Function**

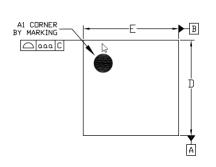
The GLF72101, GLF72103, and GLF72105 have an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

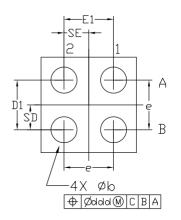
#### **Board Layout**

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.



## **PACKAGE OUTLINE**





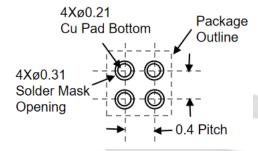
	L <sub>A3</sub>
// bbb C	1 1
	A2 A
4X 🔼 ccc C	SEATING PLANE

Dimensional Ref.							
REF.	Min.	Nom.	Max.				
Α	0.410	0.460	0.510				
Α1	0.135	0.160	0.185				
Α2	0.250	0.275	0.300				
Α3	0.020	0.025	0.030				
D	0.755	0.770	0.785				
Е	0.755	0.770	0.785				
D1	0.350	0.400	0.450				
E1	0.350	0.400	0.450				
Ь	0.170	0.210	0.250				
е	0	.400 BS	C				
SD	0	.200 BS	C				
SE	0	.200 BS	C				
To	ol. of Fo	rm&Pos	sition				
aaa	0.10						
ЬЬЬ	0.10						
ccc	0.05						
ddd		0.05					

#### Notes

- 1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
- 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
- 3. A3: BACKSIDE LAMINATION

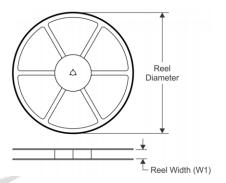
## **Recommended Footprint**



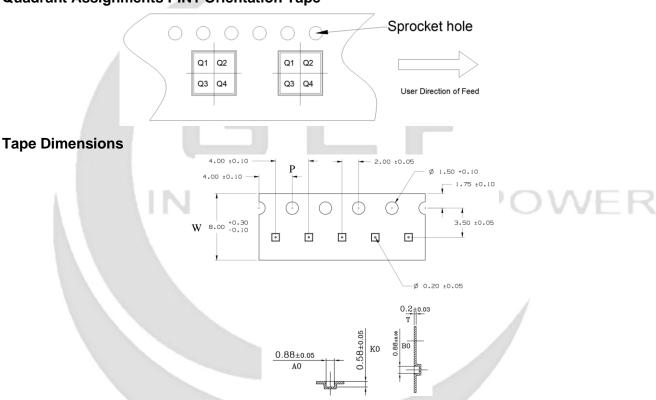


## TAPE AND REEL INFORMATION

#### **Reel Dimensions**



# **Quadrant Assignments PIN1 Orientation Tape**



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	Α0	В0	K0	Р	W	Pin1
GLF72100	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72101	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72102	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72103	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72105	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72106	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1

#### Remark:

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- C0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

# GLF72100, GLF72101, GLF72102, GLF72103, GLF72105, GLF72106

Nano Current Leakage I<sub>Q</sub>Smart<sup>™</sup> Load Switch with RCB

## **SPECIFICATION DEFINITIONS**

Document Type	Meaning	Product Status		
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development		
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification		
Product Specification	This document represents the characteristics of the device.	Production		

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