GLF71305

Nano-Current Consumed, I_QSmart™ LoadSwitch with Slew Rate Control

Product Specification

DESCRIPTION

The GLF71305 is an ultra-efficiency, 2.0 A rated, Load Switch with integrated slew rate control. The best in class efficiency makes it an ideal choice for use in IoT, mobile, and wearable electronics.

The GLF71305 features an ultra-efficient I_QSmart™ technology that supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF71305 integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF slew rate control specifically limits inrush current during turn-on to minimize voltage droop.

The GLF71305 Load Switch device supports an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

The GLF71305 Load Switch device is small utilizing a wafer level chip scale package with 4 bumps in a 0.77 mm x 0.77 mm x 0.46 mm die size and a 0.4 mm bump pitch.

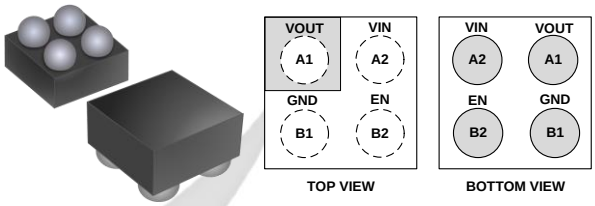
FEATURES

- Wide Input Range: 1.5 V to 5.5 V
  6 Vabs max
- Ultra-Low I_Q: 3 nA @ 5.5 V_{IN}
- Ultra-Low I_{SD}: 22 nA Typ @ 5.5 V_{IN}
- Low R_{ON} = 34 mΩ Typ. @ 5.5 V_{IN}
- I_{OUT} Max = 2.0 A
- Controlled Rise Time: 340 us at 3.3 V_{IN}
- Integrated Output Discharge Switch
- Wide Operating Temperature Range:
  -40 °C ~ 85 °C
- HBM: 6 kV, CDM: 2 kV

APPLICATIONS

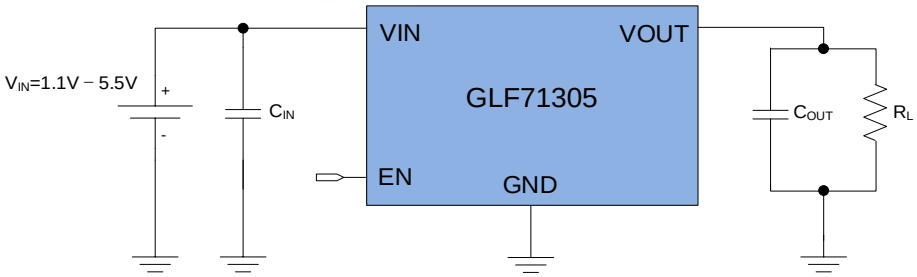
- Wearables
- Data Storage, SSD
- Mobile Devices
- Low Power Subsystems

PACKAGE



0.77 mm x 0.77 mm x 0.46 mm WLCSP

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	RON (Typ) at 5.5 V	Output Discharge	EN Activity
GLF71305	H	34 mΩ	85 Ω	High

FUNCTIONAL BLOCK DIAGRAM

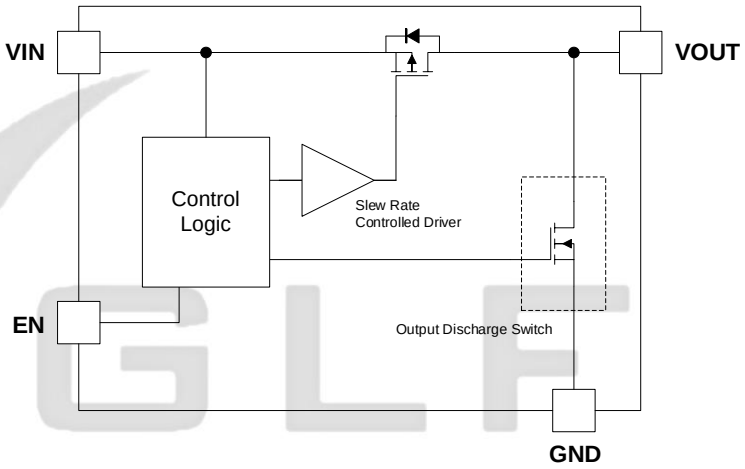


Figure 1. Functional Block Diagram

PIN CONFIGURATION

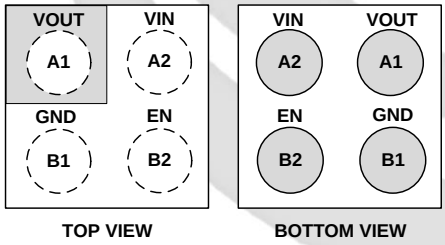


Figure 2. 0.77 mm x 0.77 mm x 0.46 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	V_{OUT}	Switch Output
A2	V_{IN}	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch. Do not leave the EN pin floating

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2	A
P_D	Power Dissipation at T_A = 25 °C			1	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (board dependent)			110	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

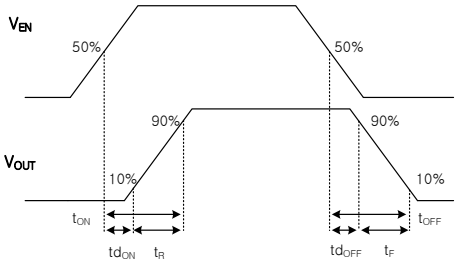
Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

Values are at V_{IN} = 3.3 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
V_{IN}	Supply Voltage			1.5		5.5	V
I_Q	Quiescent Current	V_{IN} = V_{EN} =5.5 V, I_{OUT}=0 mA			3		nA
		V_{IN} = V_{EN} =5.5 V, I_{OUT}=0 mA, Ta=85 °C (6)			7		
I_{SD}	Shutdown Current	EN = Disable, I_{OUT}=0 mA, V_{IN}=1.5 V			3		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=1.8 V			4		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=3.3 V			6		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=4.5 V			9		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V			22	50	
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=55 °C (2)			110		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5V, Ta=85 °C (2)			600		
R_{ON}	On-Resistance	V_{IN}=5.5 V, I_{OUT}= 500 mA	Ta=25 °C		34	47	mΩ
			Ta=85 °C (2)		40		
		V_{IN}=3.3 V, I_{OUT}= 500 mA	Ta=25 °C		42	56	
			Ta=85 °C (2)		50		
		V_{IN}=1.8 V, I_{OUT}= 300 mA	Ta=25 °C		68		
		V_{IN}=1.5 V, I_{OUT}= 100 mA	Ta=25 °C		75		
R_{DSC}	Output Discharge Resistance	E_N=Low , I_{FORCE}= 10 mA			85		Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}=1.5 V - 1.8 V		0.5			V
		V_{IN}=1.8 V - 5.5 V		0.6			V
V_{IL}	EN Input Logic Low Voltage	V_{IN}=1.5 V - 5.5 V				0.25	V
		V_{IN}=1.8 V - 5.5 V				0.35	V
Switching Characteristics (1)							
t_{dON}	Turn-On Delay	R_L=150 Ω, C_{OUT}=0.1 µF			245		µs
t_R	V_{OUT} Rise Time				340		
t_{dON}	Turn-On Delay (2)	R_L=500 Ω, C_{OUT}=0.1 µF			230		
t_R	V_{OUT} Rise Time (2)				330		
t_{dOFF}	Turn-Off Delay (2)	R_L=150 Ω, C_{OUT}=0.1 µF			0.89		
t_F	V_{OUT} Fall Time (2)				10		
t_{dOFF}	Turn-Off Delay (2)	R_L=500 Ω, C_{OUT}=0.1 µF			1		
t_F	V_{OUT} Fall Time (2)				13		

Notes:
1. t_{ON} = t_{dON} + t_R , t_{OFF} = t_{dOFF} + t_F
2. By design; characterized, not production tested.
3. Timing Diagram



TYPICAL PERFORMANCE CHARACTERISTICS

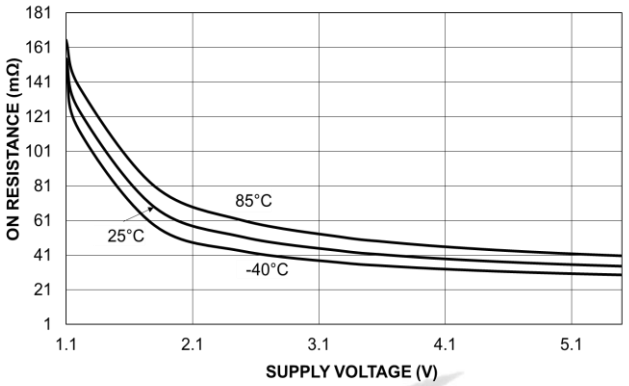


Figure 3. On-Resistance vs. Supply Voltage

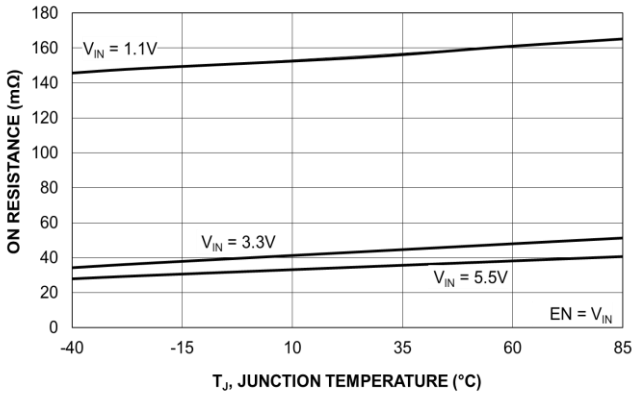


Figure 4. On-Resistance vs. Temperature

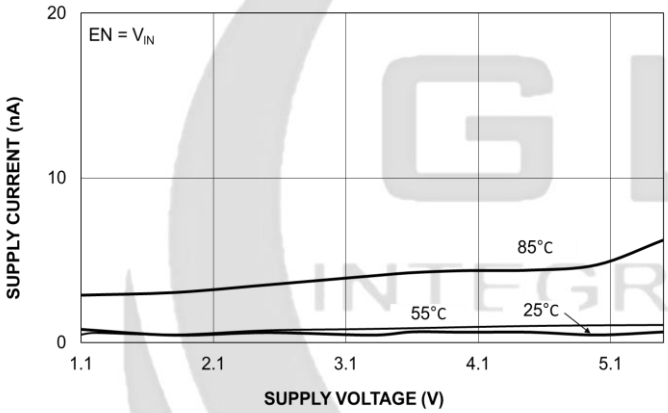


Figure 5. Quiescent Current vs. Supply Voltage

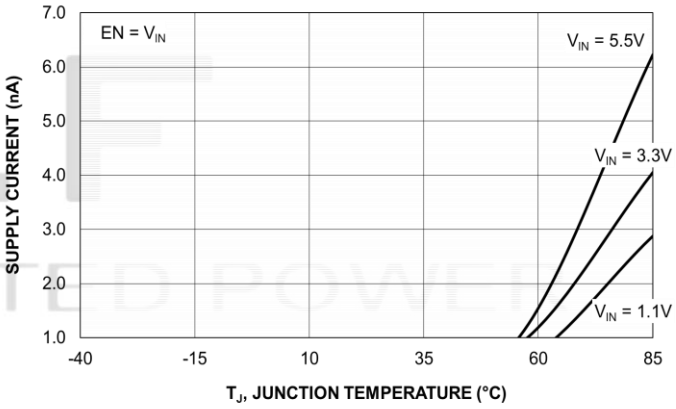


Figure 6. Quiescent Current vs. Temperature

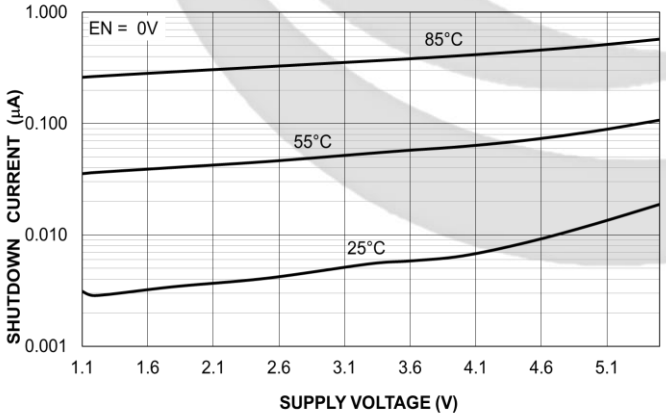


Figure 7. Shutdown Current vs. Supply Voltage

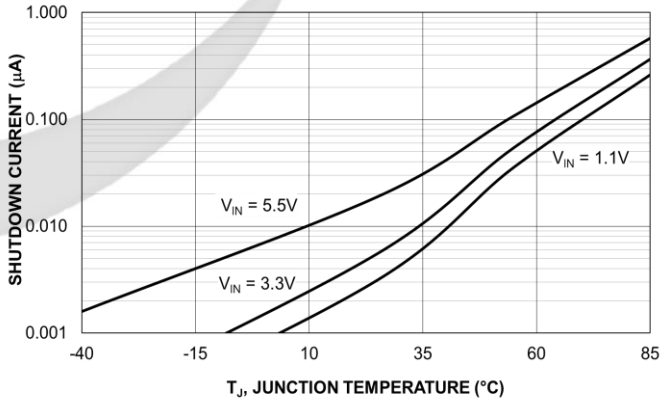


Figure 8. Shutdown Current vs. Temperature

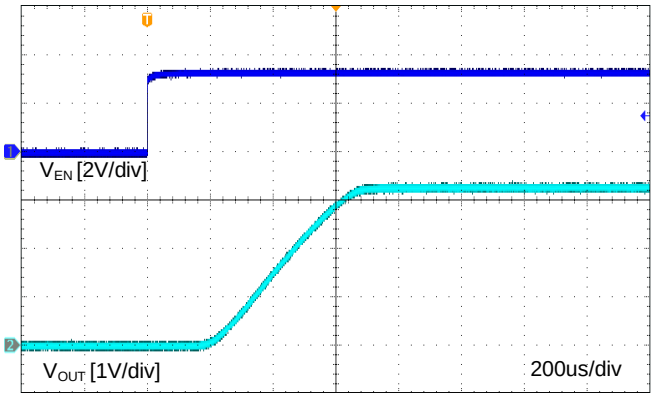


Figure 11. Turn-On Response
V_{IN}=3.3 V, C_{IN}=1.0 uF, C_{OUT}=0.1 uF, R_L=150 Ω

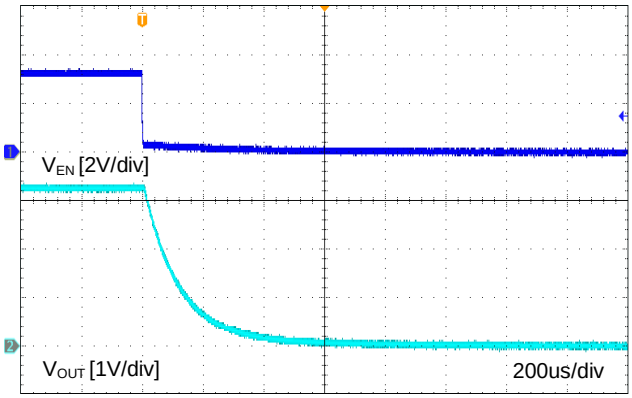


Figure 12. Turn-On Response
V_{IN}=3.3 V, C_{IN}=1.0 uF, C_{OUT}=0.1 uF, R_L=500 Ω

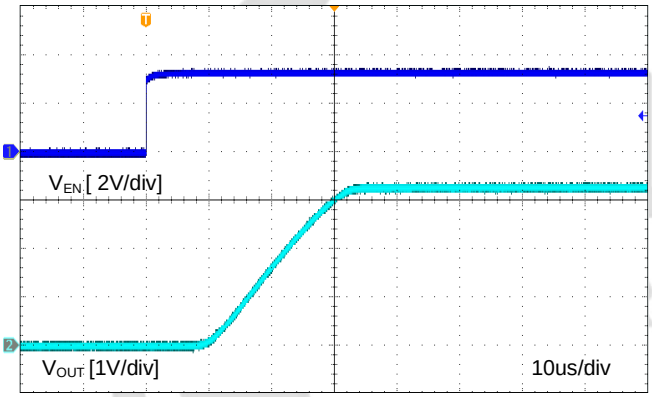


Figure 13. Turn-Off Response, Output Discharge
V_{IN}=3.3 V, C_{IN}=1.0 uF, C_{OUT}=0.1 uF, R_L=150 Ω

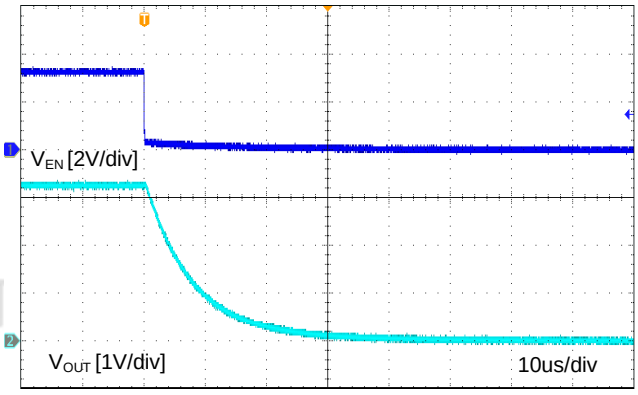


Figure 14. Turn-Off Response, Output Discharge
V_{IN}=3.3 V, C_{IN}=1.0 uF, C_{OUT}=0.1 uF, R_L=500 Ω

APPLICATION INFORMATION

The GLF71305 is a 2.0 A, Ultra-Efficient IQSmart™ LoadSwitch devices with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.5 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin the moment when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

EN pin

The GLF71305 can be activated by EN pin high level. Note that the EN pin is not allowed to be floating.

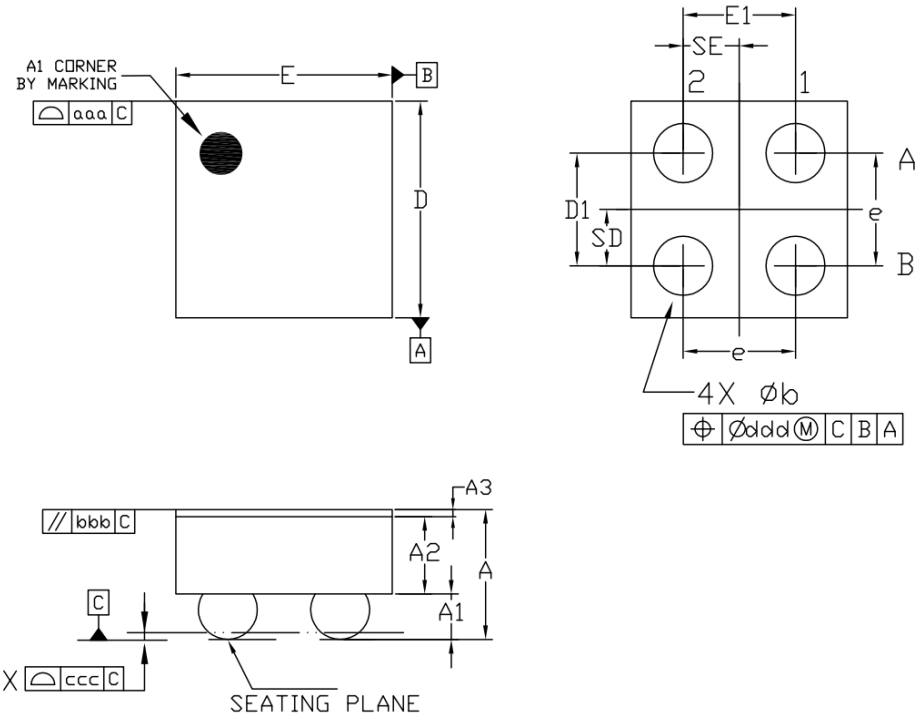
Output Discharge Function

The GLF71305 has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce voltage drops and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

PACKAGE OUTLINE



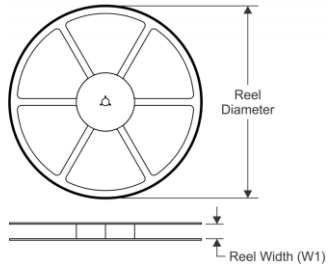
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.410	0.460	0.510
A1	0.135	0.160	0.185
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	0.755	0.770	0.785
E	0.755	0.770	0.785
D1	0.350	0.400	0.450
E1	0.350	0.400	0.450
b	0.170	0.210	0.250
e	0.400 BSC		
SD	0.200 BSC		
SE	0.200 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

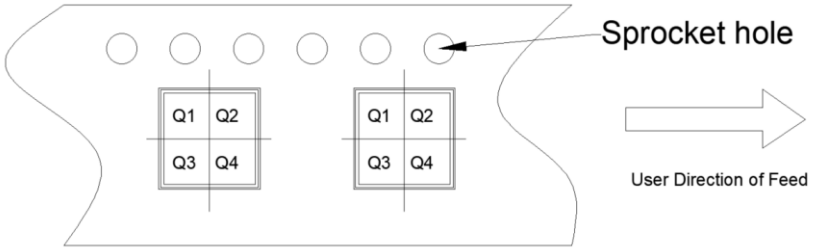
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

TAPE AND REEL INFORMATION

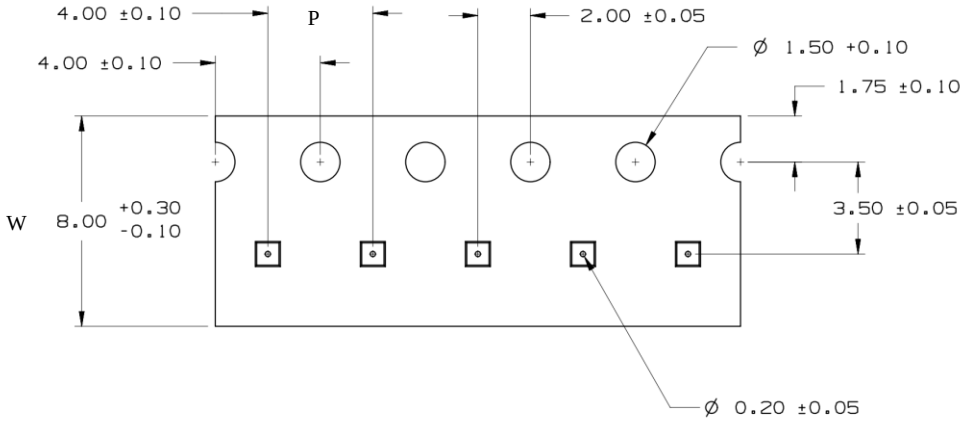
REEL DIMENSIONS

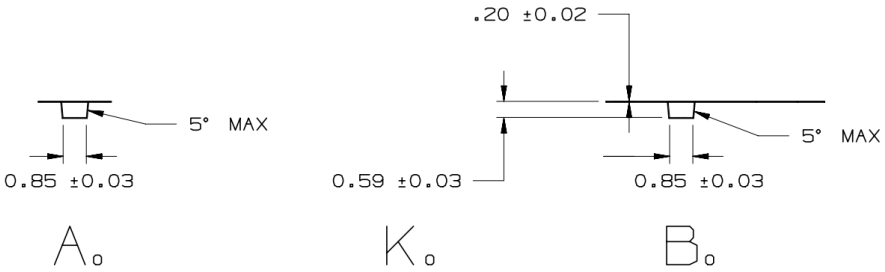


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF71305	WLCSP	4	4000	180	9	0.85	0.85	0.59	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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