GLF72120, GLF72122

4 A, Slew Rate Controlled I_QSmart™ Load Switch with True Reverse Current Blocking

Product Specification

DESCRIPTION

The GLF72120 and GLF72122 are an advanced technology fully integrated I_QSmart™ load switch device with True Reverse Current Blocking (TRCB) technology and the slew rate control of the output voltage.

The GLF72120 and GLF72122 offer industry leading True Reverse Current Blocking (TRCB) performance, featuring an ultra-low threshold voltage. It minimizes reverse current flow in the event that the VOUT pin voltage exceeds the VIN voltage.

The GLF72120 and GLF72122 have industry leading efficiency. It features a 14 mΩ R_{ON} typical at 5.5 V, reducing power loss during conduction. The device also features ultra-low shutdown current (I_{SD}) to reduce power loss and battery drain in the off state. When EN is pulled low, and the output is grounded, the GLF72120 and GLF72122 can achieve an I_{SD} as low as 56 nA typical at 5.5 V.

The GLF72120 and GLF72122 load switch device support an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

The GLF72120 and GLF72122 load switch device are in a 0.97 mm x 1.47 mm x 0.55 mm chip scale package with 6 bumps and a 0.5 mm pitch.

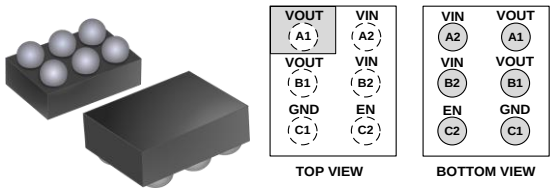
FEATURES

- True Reverse Current Blocking
- Low R_{ON}: 14 mΩ Typ at 5.5 V_{IN}
- Ultra-Low I_Q: 1.3 µA Typ at 5.5 V_{IN}
- Ultra-Low I_{SD}: 56 nA Typ at 5.5 VIN
- I_{OUT} Max: 4 A
- Supply Voltage Range: 1.5 V to 5.5 V
  6 Vabs max
- Controlled V_{OUT} Rise Time
  GLF72120: 730 µs at 3.3 V_{IN}
  GLF72122: 2000 µs at 3.3 V_{IN}
- Internal EN Pull-Down Resistor
- 0.97 mm x 1.47 mm x 0.55 mm Wafer Level Chip Scale Package

APPLICATIONS

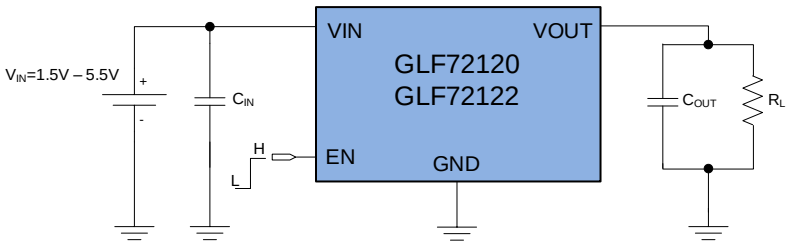
- Mobile Devices
- Wearables
- Low Power Subsystems

PACKAGE



0.97 mm x 1.47 mm x 0.55 mm, 0.5 mm Pitch

APPLICATION DIAGRAM



DEVICE INFORMATION

Part Number	Top Mark	V_{OUT} Rising Time, Tr Typ [µs] at 3.3 V_{IN}	EN Activity	Tape and Reel Packaging
GLF72120	RA	730	High	3000 Pieces on 7 inch reel
GLF72122	RC	2000		

FUNCTIONAL BLOCK DIAGRAM

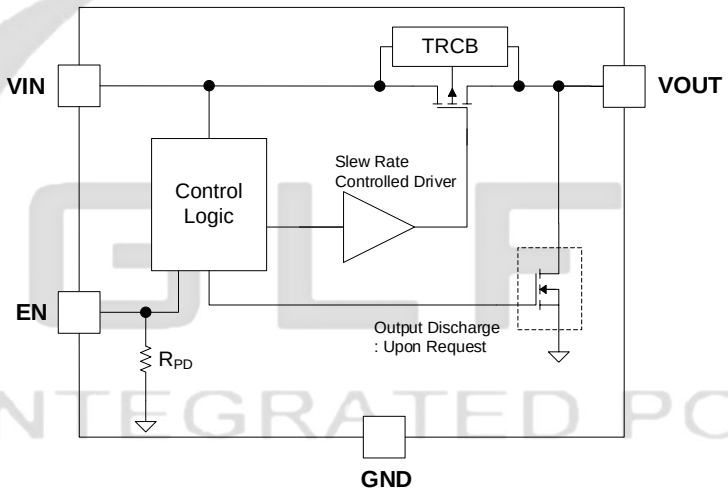


Figure 1. Functional Block Diagram

PIN CONFIGURATION

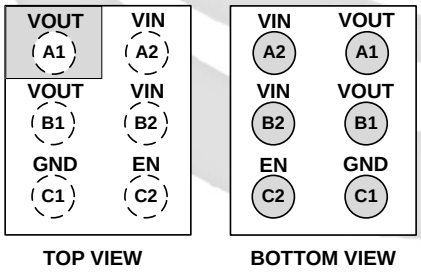


Figure 2. 0.97 mm x 1.47 mm x 0.55 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1,B1	V_{OUT}	Switch Output
A2,B2	V_{IN}	Switch Input. Supply Voltage
C1	GND	Ground
C2	EN	Enable to control the switch

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GNF		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			4	A
P_D	Power Dissipation at T_A = 25 °C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_J	Maximum Junction Temperature			150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (Measured using 2S2P JEDEC std. PCB.)			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

Typical values are at V_{IN} = 3.3 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Basic Operation							
I_Q	Supply Current	EN = Enable, I_{OUT}= 0 mA, V_{IN} = V_{EN} = 5.5 V			1.3	2	µA
		EN= Enable, I_{OUT}= 0 mA, V_{IN}=V_{EN}=5.5 V, Ta=85 °C (3)			1.4		
I_{SD}	Shutdown Current on	EN= Disable, I_{OUT}= 0 mA, V_{IN}= 1.5 V			5	20	nA
		EN= Disable, I_{OUT}= 0 mA, V_{IN}= 3.3 V			8		
		EN= Disable, I_{OUT}= 0 mA, V_{IN}= 4.2 V			12		
		EN= Disable, I_{OUT}= 0 mA, V_{IN}= 5.5 V			56	100	
		EN= Disable, I_{OUT}= 0 mA, V_{IN}= 5.5 V, Ta= 85 °C (3)			1000		
R_{ON}	On-Resistance	V_{IN}= 5.5 V I_{OUT}= 500 mA	Ta= 25 °C		14	19	mΩ
			Ta= 85 °C (3)		16		
		V_{IN}= 3.3 V, I_{OUT}= 500 mA	Ta= 25 °C		18	23	
			Ta= 85 °C (3)		21		
		V_{IN}= 1.8 V, I_{OUT}= 300 mA	Ta= 25 °C (3)		30		
		V_{IN}= 1.5 V, I_{OUT}= 100 mA	Ta= 25 °C		37	42	
V_{IH}	EN Input Logic High Voltage	V_{IN}= 1.5 - 5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN}= 1.5 - 5.5 V				0.4	
R_{EN}	EN pull down resistance	Internal Resistance			10		MΩ
I_{EN}	EN Source or Sink Current	V_{EN}= V_{IN} or GND			0.5	1	µA
V_{RCB_TH}	RCB Protection Threshold Voltage	V_{OUT} – V_{IN}			37		mV
V_{RCB_RL}	RCB Protection Release Voltage	V_{IN} – V_{OUT}			37		
Switching Characteristics (2), GLF72120							
t_{dON}	Turn-On Delay	R_{OUT}= 150 Ω, C_{OUT}= 1.0 µF			450		µs
t_R	V_{OUT} Rise Time				730		
t_{dOFF}	Turn-Off Delay (3)	R_{OUT}= 150 Ω, C_{OUT}= 1.0 µF			20		
t_F	V_{OUT} Fall Time (3)				360		
Switching Characteristics (2), GLF72122							
t_{dON}	Turn-On Delay	R_{OUT}= 150 Ω, C_{OUT}= 1.0 µF			1500		µs
t_R	V_{OUT} Rise Time				2000		
t_{dOFF}	Turn-Off Delay (3)	R_{OUT}= 150 Ω, C_{OUT}= 1.0 µF			25		
t_F	V_{OUT} Fall Time (3)				300		

Notes:
1. I_Q does not include Enable pull down current through the pull-down resistor R_{EN}.
2. t_{ON} = t_{dON} + t_R, t_{OFF} = t_{dOFF} + t_F
3. By design; characterized, not production tested

TIMING DIAGRAM

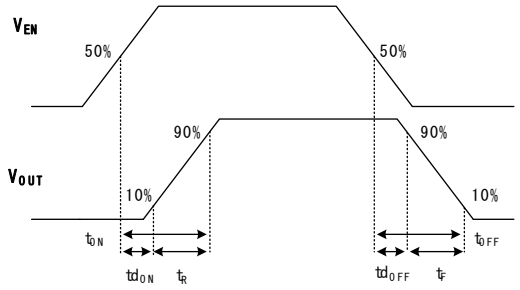


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

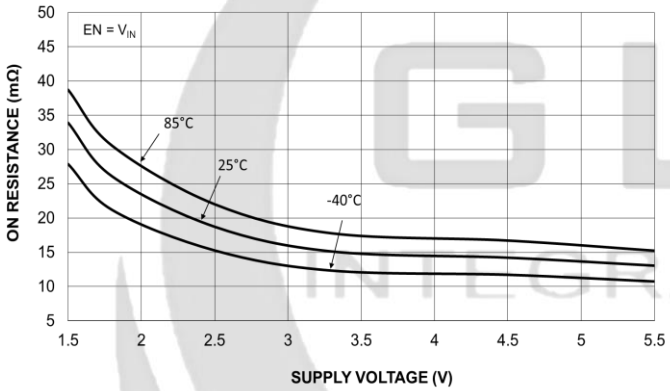


Figure 4. On-Resistance vs. Supply Voltage

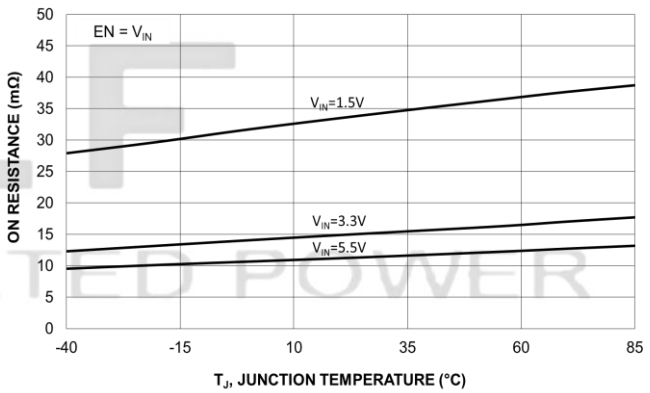


Figure 5. On-Resistance vs. Temperature

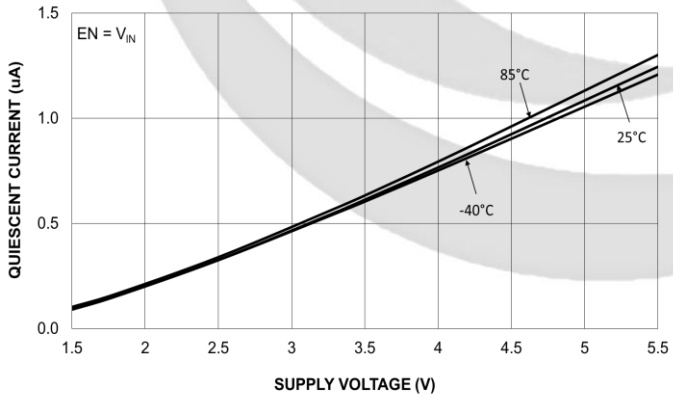


Figure 6. Quiescent Current vs. Supply Voltage

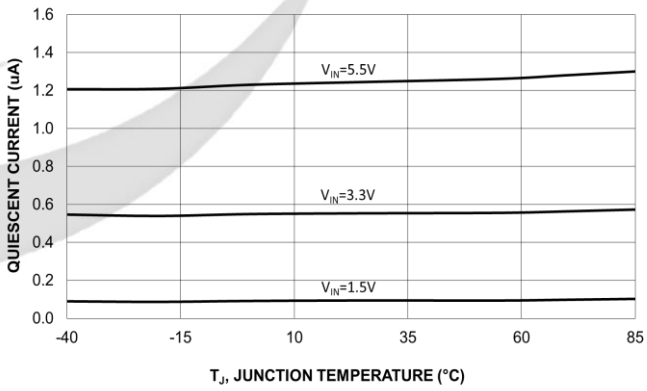


Figure 7. Quiescent Current vs. Temperature

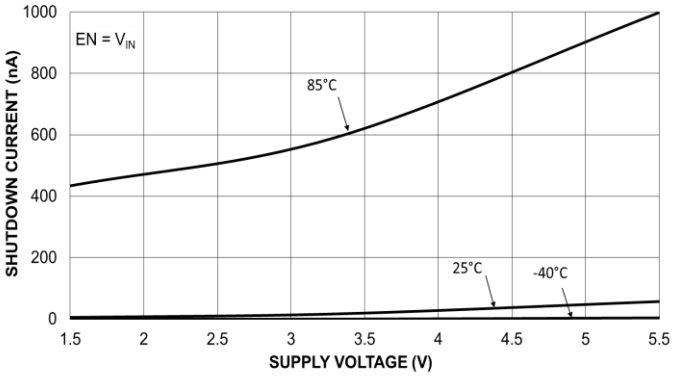


Figure 8. Shutdown Current vs. Supply Voltage

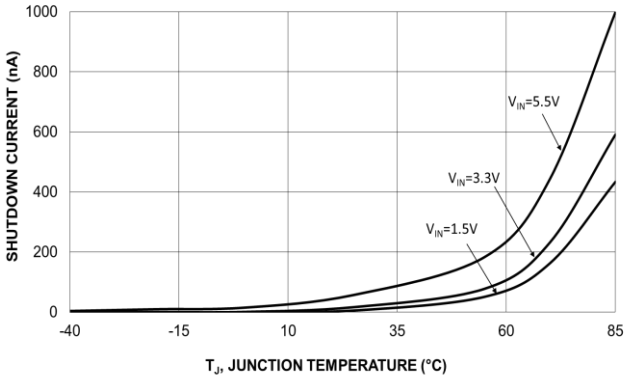


Figure 9. Shutdown Current vs. Temperature

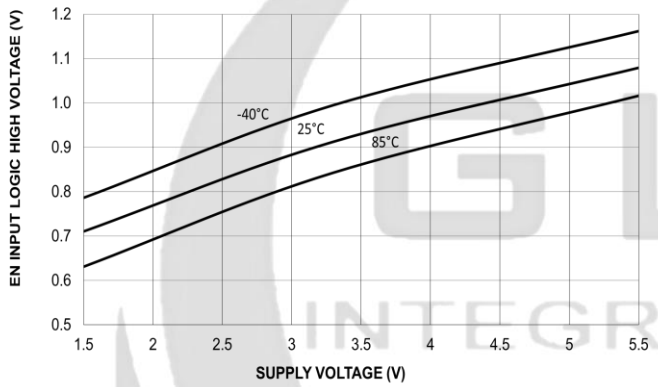


Figure 10. EN Input Logic High Threshold

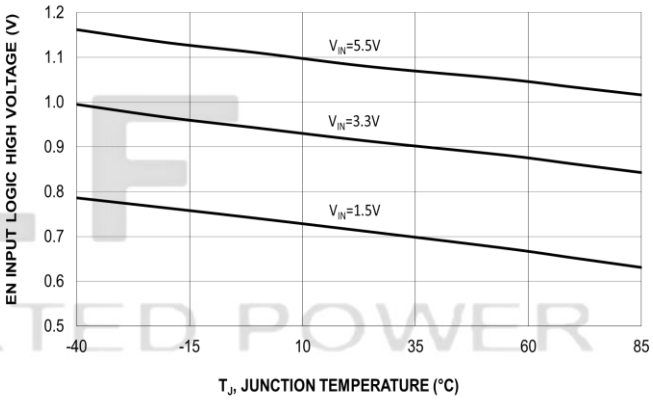


Figure 11. EN Input Logic High Threshold Vs. Temperature

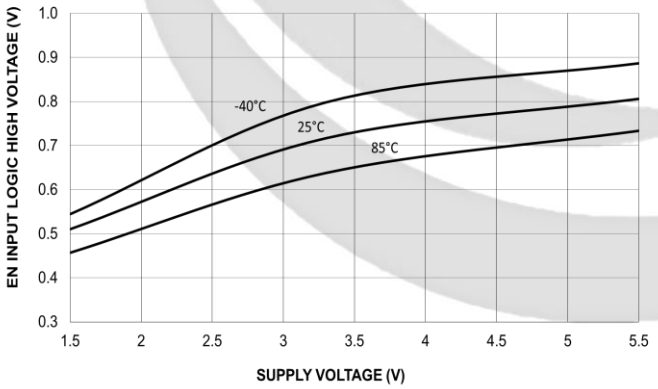


Figure 12. EN Input Logic Low Threshold

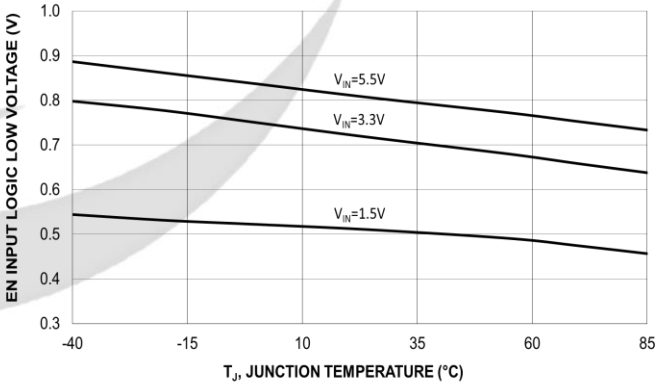


Figure 13. EN Input Logic Low Threshold Vs. Temperature

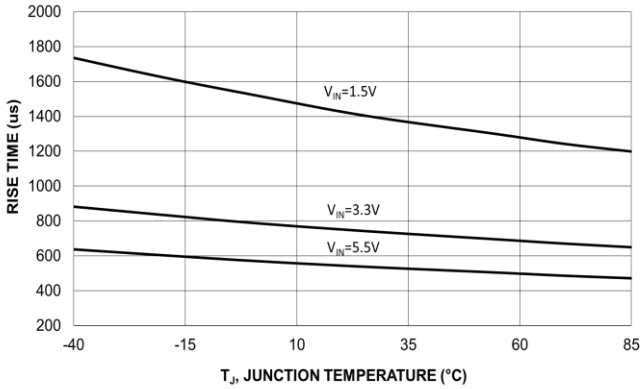


Figure 14. V_{OUT} Rise Time vs. Temperature, GLF72120

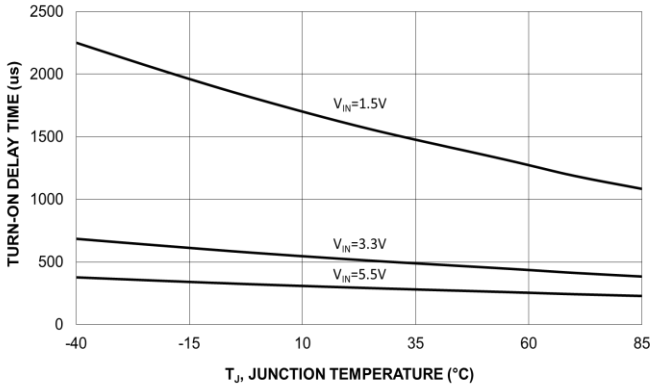


Figure 15. Turn-On Delay Time vs. Temperature, GLF72120

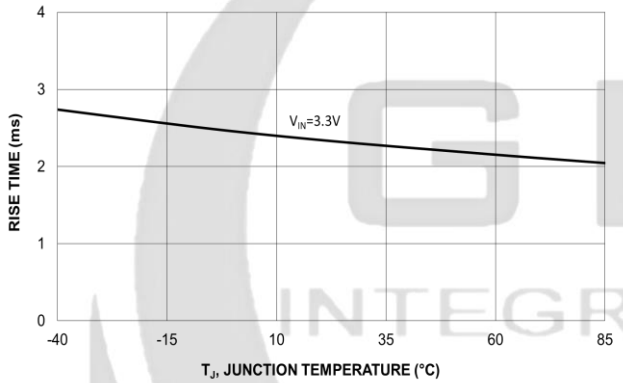


Figure 16. V_{OUT} Rise Time vs. Temperature, GLF72122

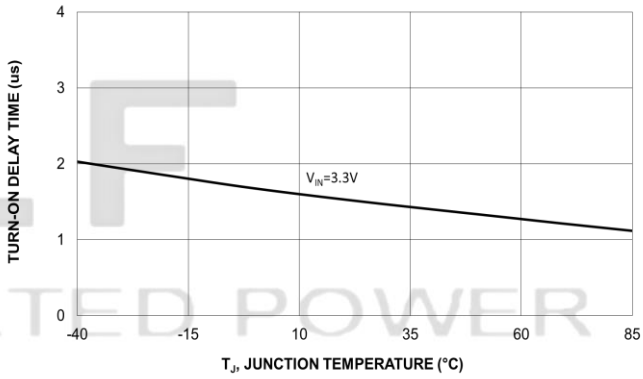


Figure 17. Turn-On Delay Time vs. Temperature, GLF72122

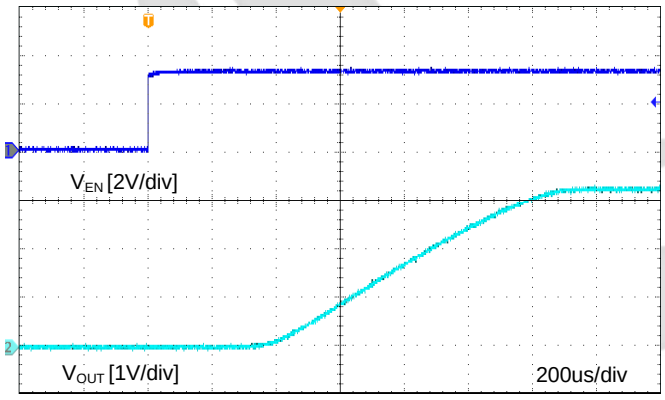


Figure 18. Turn-On Response, GLF72120
V_{IN}= 3.3 V, C_{IN}= 1.0 uF, C_{OUT}= 1.0 uF, R_L= 150 Ω

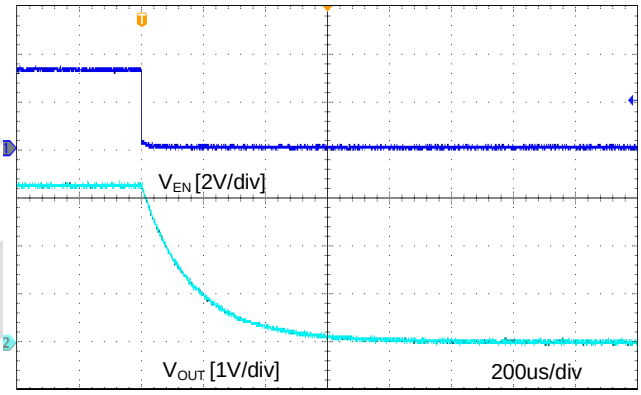


Figure 19. Turn-Off Response, GLF72120
V_{IN}= 3.3 V, C_{IN}= 1.0 uF, C_{OUT}= 1.0 uF, R_L= 150 Ω

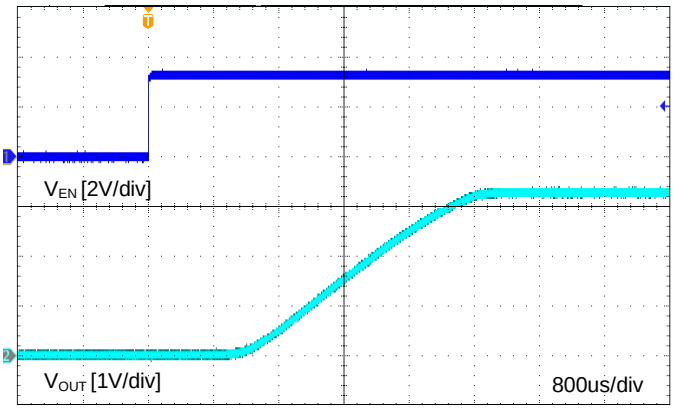


Figure 20. Turn-On Response, GLF72122
V_{IN}= 3.3 V, C_{IN}= 1.0 uF, C_{OUT}= 1.0 uF, R_L= 150 Ω

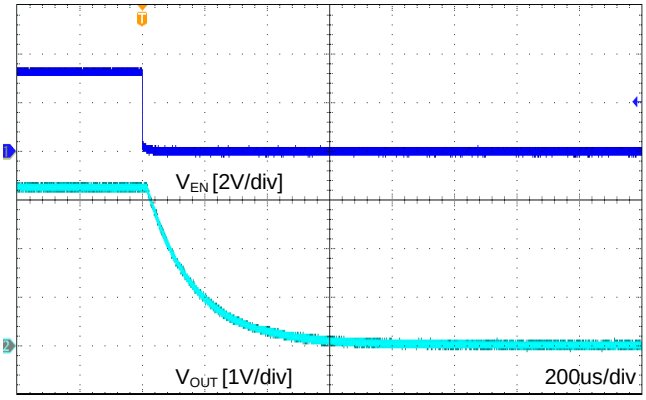


Figure 21. Turn-Off Response, GLF72122
V_{IN}= 3.3 V, C_{IN}= 1.0 uF, C_{OUT}= 1.0 uF, R_L= 150 Ω

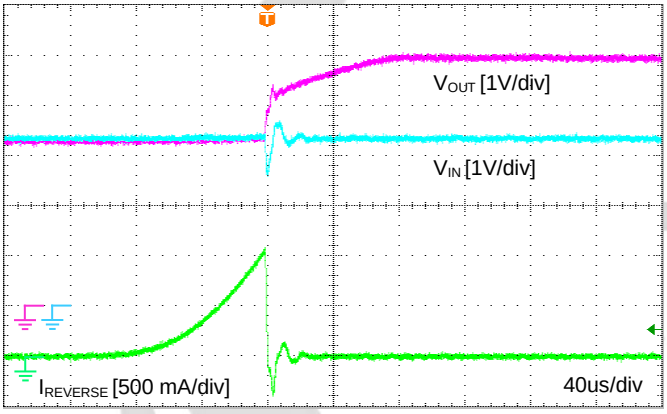


Figure 22. Reverse Current Blocking at Switch On
V_{IN}= Open, C_{IN}= 1.0 uF, C_{OUT}= 1.0 uF

APPLICATION INFORMATION

The GLF72120 and GLF72122 are an ultra-efficient integrated 4 A I_QSmart™ load switch with the slew rate control of the output voltage to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.5 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power supply. The package is 0.97 mm x 1.47 mm x 0.55 mm wafer level chip scale package saving space in compact applications and it has 6 bumps, 0.5 mm pitch for manufacturing availability.

Input Capacitor

The GLF72120 and GLF72122 require an input capacitor to function. A 1uF capacitor is recommended to be placed close to V_{IN} pin to reduce a voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to attenuate the input voltage drop.

Output Capacitor

A 0.1 uF capacitor or higher values can be able to prevent undershoot caused by parasitic inductance on board traces at switching off and improve reliability of a controlled voltage rail. The C_{OUT} should be placed close to VOUT and GND pins.

EN pin

The GLF72120 and GLF72122 can be activated by EN pin high. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller.

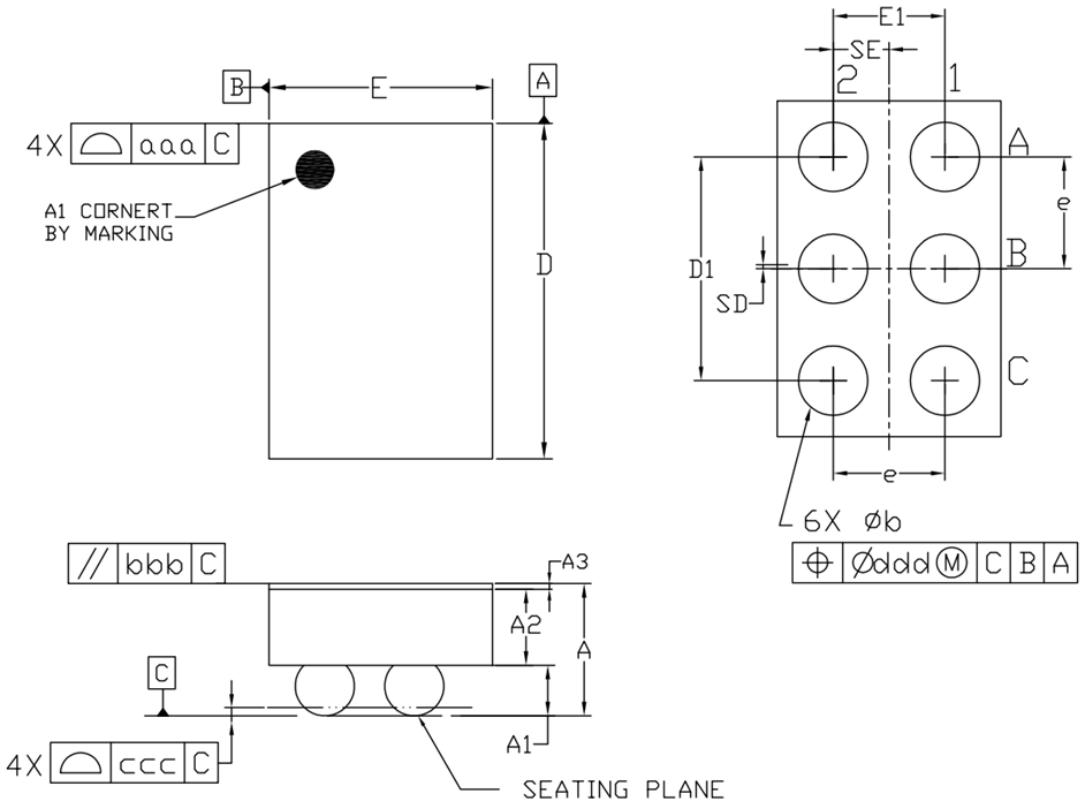
True Reverse Current Blocking

The GLF72120 and GLF72122 have a built-in reverse current blocking protection which always monitors the output voltage level regardless of the status of EN pin to check if it is greater than the input voltage. When the output voltage goes beyond the input voltage by 37 mV, that is the reverse current blocking protection trip voltage, the reverse current blocking function block turns off the switch. Note that some reverse current can occur until the V_{RCB} is triggered. The main switch will resume normal operation when the output voltage drops below the input source by the RCB protection release voltage.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will be better to reduce parasitic effects at dynamic operations and improve thermal performance at high load current.

PACKAGE OUTLINE



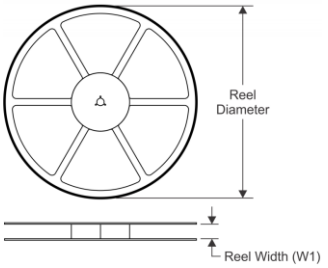
Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

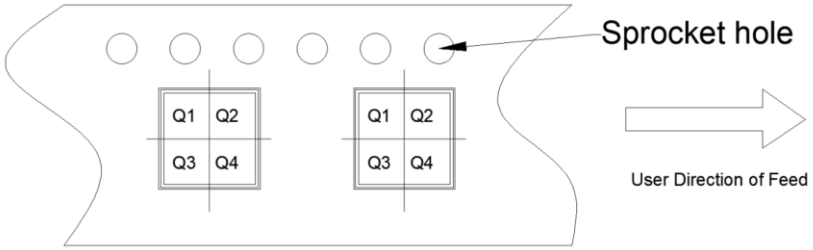
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	1.460	1.470	1.485
E	0.960	0.970	0.985
D1	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.000 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

TAPE AND REEL INFORMATION

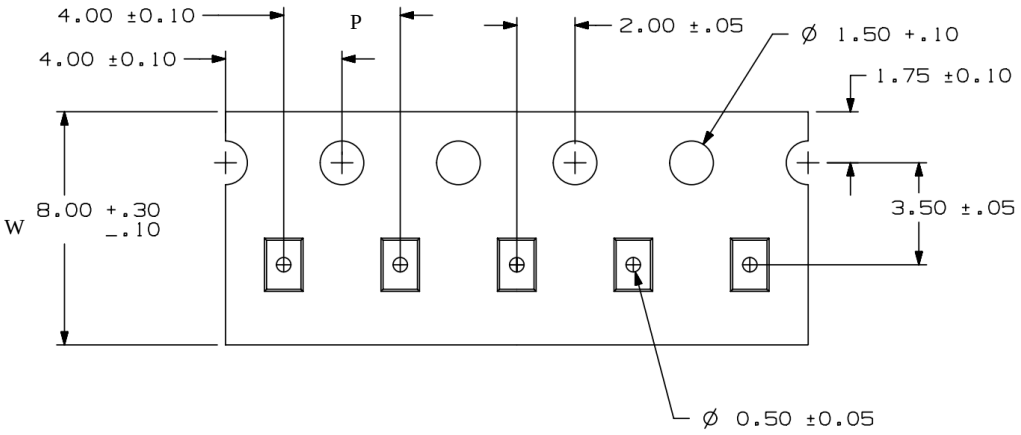
REEL DIMENSIONS

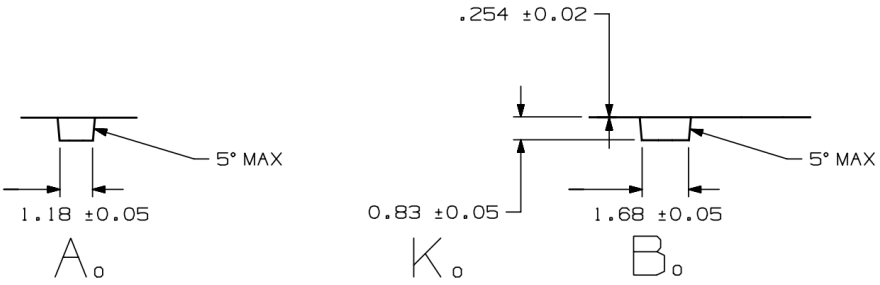


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF72120	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1
GLF72122	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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