GLF1411

Dual Channel, I_QSmart™ Load Switch with Slew Rate Control

Product Specification

DESCRIPTION

The GLF1411 is an ultra-efficient dual channel load switch with slew rate control. The devices feature the ultra-efficient I_QSmart™ technology that supports some of the low R_{ON}, quiescent currents (I_Q), and shutdown currents (I_{SD}) in an input voltage range from 1.5 V to 5.5 V.

The integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF1411 slew rate control specifically limits inrush current during turn-on to minimize voltage droop.

Each channel runs independently controlled by separate EN control pin. Both devices feature an integrated output discharge switch when they are turned off to discharge output capacitors quickly.

FEATURES

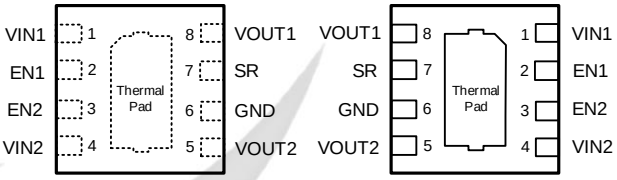
Per Channel

- Supply Voltage Range: 1.5 V to 5.5 V
- Slew Rate Control Pin of Output Rise Time
- Low R_{ON}:
  - 180 mΩ Typ. at 5.5 V_{IN}
  - 220 mΩ Typ. at 3.3 V_{IN}
  - 265 mΩ Typ. at 2.5 V_{IN}
- I_{OUT} Max: 1 A Continuous Output Current
- Ultra-Low Quiescent Current, I_Q
  - 10 nA Typ. at 5.5 V_{IN}
  - 5 nA Typ. at 3.3 V_{IN}
  - 4 nA Typ. at 2.5 V_{IN}
- Ultra-Low Stand-by Current, I_{SD}
  - 32 nA Typ. at 5.5 V_{IN}
  - 4 nA Typ. at 3.3 V_{IN}
  - 3 nA Typ. at 2.5 V_{IN}
- Output Discharge Switch When Disabled

APPLICATIONS

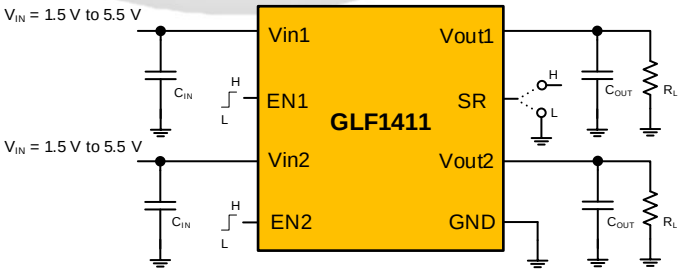
- Smart Mobile Devices
- IoT Devices
- Low Power Subsystems

PACKAGE



1.5 mm x 1.5 mm DFN-8L

APPLICATION DIAGRAM



DEVICE ORDERING INFORMATION

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V_{IN}	Output Discharge	V_{OUT} Rise Time t_R (Typ) at 3.3 V_{IN}	EN Activity
GLF1411-D1G7	DR	180 mΩ	95 Ω	390 µs at SR= High 45 µs at SR= GND	High

FUNCTIONAL BLOCK DIAGRAM

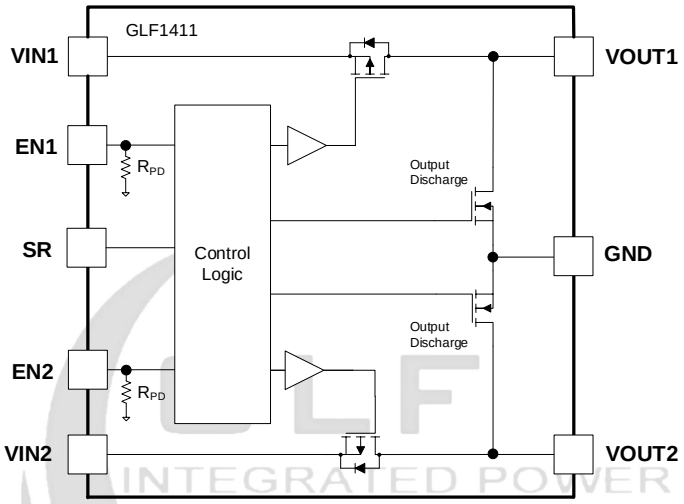


Figure 1. Functional Block Diagram

PIN CONFIGURATION

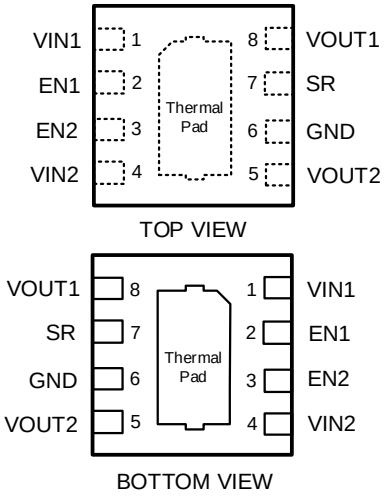


Figure 2. 1.5 mm x 1.5 mm DFN-8L

PIN DEFINITION

Pin	Name	Description
1	VIN1	Switch 1 input.
2	EN1	Active high signal to enable the switch 1
3	EN2	Active high signal to enable the switch 2
4	VIN2	Switch 2 input.
5	VOUT2	Switch 2 output
6	GND	Ground
7	SR	Slew rate control of $V_{OUT}1$ and $V_{OUT}2$. SR = High (Slow) SR = GND (Fast)
8	VOUT1	Switch 1 output
	Thermal pad	Tie to GND

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, EN, SR	Each Pin to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current	T_A = 25 °C		1	A
		T_A = 85 °C		0.8	A
T_J	Maximum Junction Temperature			150	°C
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Ambient Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			190	°C/W
θ_{JC_Top}	Thermal Resistance, Junction to Case			95	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	5		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS (Per Channel)

Values are at V_{IN} = 3.3 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Basic Operation							
I_Q	Quiescent Current (1) Each Channel	EN = V_{IN} , I_{OUT}= 0 mA, V_{IN}= 1.5 V			3		nA
		EN = V_{IN} , I_{OUT}= 0 mA, V_{IN}= 1.8 V			3.5		
		EN = V_{IN} , I_{OUT}= 0 mA, V_{IN}= 2.5 V			4		
		EN = V_{IN} , I_{OUT}= 0 mA, V_{IN}= 3.3 V			5	20	
		EN = V_{IN} , I_{OUT}= 0 mA, V_{IN} =5.5 V			10		
		EN = V_{IN} , I_{OUT}= 0 mA, V_{IN}= 5.5 V, Ta= 85 °C (4)			19		
I_{SD}	Shut Down Current Each Channel	EN = 0 V, I_{OUT}= 0 mA, V_{IN}= 1.5 V			2		nA
		EN = 0 V, I_{OUT}= 0 mA, V_{IN}= 1.8 V			2		
		EN = 0 V, I_{OUT}= 0 mA, V_{IN}= 2.5 V			3		
		EN = 0 V, I_{OUT}= 0 mA, V_{IN}= 3.3 V			4	50	
		EN = 0 V, I_{OUT}= 0 mA, V_{IN}= 5.5 V			32		
		EN = 0 V, I_{OUT}= 0 mA, V_{IN}= 5.5 V, Ta= 85 °C (4)			100		
R_{ON}	On-Resistance	V_{IN}= 5.5 V, I_{OUT}= 500 mA	Ta= 25 °C		180	240	mΩ
			Ta= 85 °C (4)		220		
		V_{IN}= 3.3 V, I_{OUT}= 500 mA			220	300	
		V_{IN}= 2.5 V, I_{OUT}= 300 mA			265		
		V_{IN}= 1.8 V, I_{OUT}= 300 mA			375		
		V_{IN}= 1.5 V, I_{OUT}= 100 mA			470		
R_{DSC}	Output Discharge Resistance	V_{EN} = 0 V, I_{FORCE}= 10 mA			95		Ω
V_{IH}	EN and SR, Logic High Voltage	V_{IN}= 1.5 V to 5.5 V		1.1			V
V_{IL}	EN and SR, Logic Low Voltage	V_{IN}= 1.5 V to 5.5 V				0.45	V
R_{EN}	EN Internal Resistance	Internal Pull-down Resistance			20		MΩ
I_{EN}	EN Current	EN= V_{IN} or 0 V			0.25		µA
Switching Characteristics (2)							
t_{dON}	Turn-On Delay (4)	SR= High	V_{IN} = 1.8 V C_{OUT}=0.1 µF, R_L=150 Ω		840		µs
t_R	V_{OUT} Rise Time(4)				570		
t_{dOFF}	Turn-Off Delay (3), (4)				19		
t_F	V_{OUT} Fall Time (3), (4)				10		
t_{dON}	Turn-On Delay (4)	SR= GND			120		
t_R	V_{OUT} Rise Time(4)				70		
t_{dOFF}	Turn-Off Delay (3), (4)				20		
t_F	V_{OUT} Fall Time (3), (4)				10		
t_{dON}	Turn-On Delay	SR= High	V_{IN} = 3.3 V C_{OUT}=0.1 µF, R_L=150 Ω		380		
t_R	V_{OUT} Rise Time				390		
t_{dOFF}	Turn-Off Delay (3), (4)				20		
t_F	V_{OUT} Fall Time (3), (4)				12		
t_{dON}	Turn-On Delay	SR= GND			60		
t_R	V_{OUT} Rise Time				45		
t_{dOFF}	Turn-Off Delay (3), (4)				20		

t_F	V_{OUT} Fall Time (3), (4)				12		
t_{dON}	Turn-On Delay (4)	SR= High	V_{IN} = 5.0 V C_{OUT}=0.1 µF, R_L=150 Ω		230		
t_R	V_{OUT} Rise Time(4)				320		
t_{dOFF}	Turn-Off Delay (3), (4)				20		
t_F	V_{OUT} Fall Time (3), (4)				12		
t_{dON}	Turn-On Delay (4)	SR= GND			43		µs
t_R	V_{OUT} Rise Time(4)				30		
t_{dOFF}	Turn-Off Delay (3), (4)				20		
t_F	V_{OUT} Fall Time (3), (4)				12		

Notes: 1. I_Q does not include the enable current (I_{EN}) through the pull-down resistor R_{EN}.
2. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$
3. Output discharge path is enabled during off.
4. By design; characterized, not production tested.

TIMING DIAGRAM

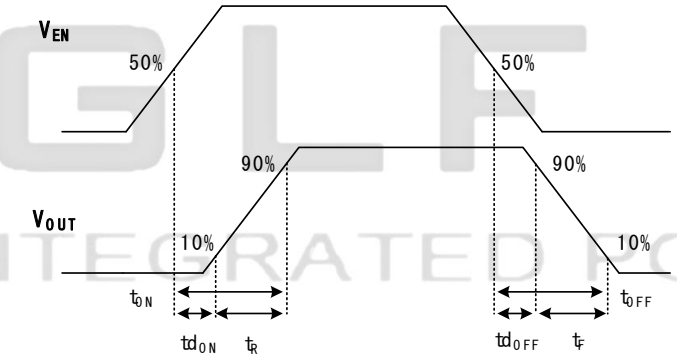


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

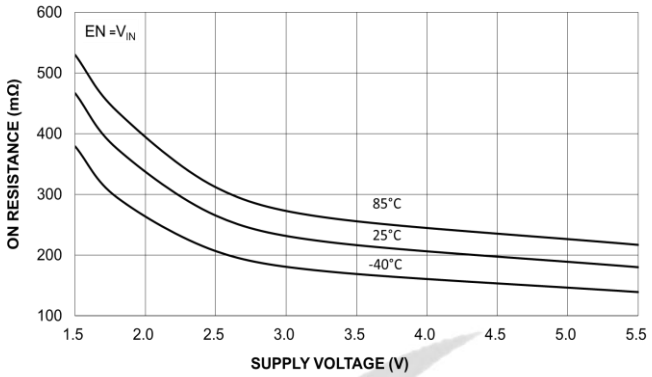


Figure 4. On-Resistance vs. Supply Voltage

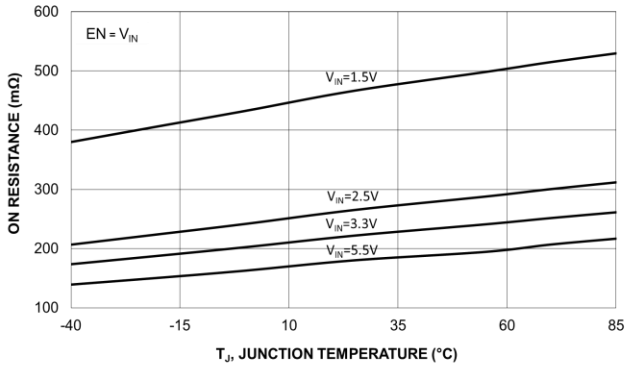


Figure 5. On-Resistance vs. Temperature

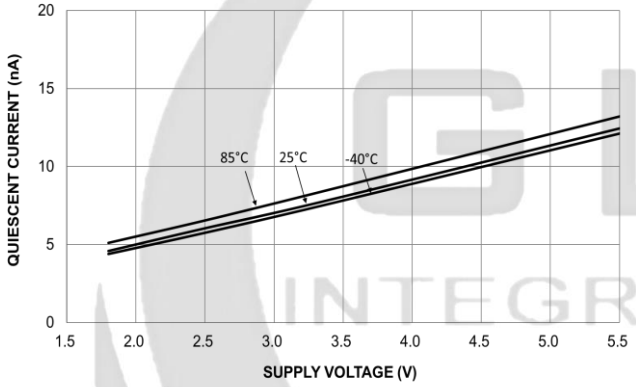


Figure 6. Quiescent Current vs. Supply Voltage

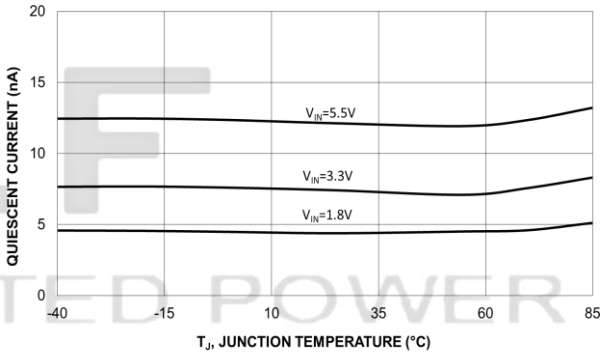


Figure 7. Quiescent Current vs. Temperature

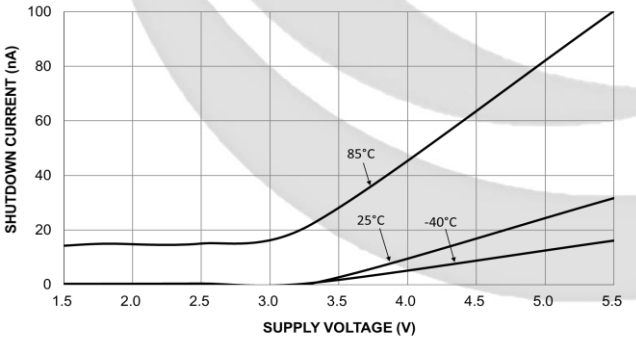


Figure 8. Shutdown Current vs. Supply Voltage

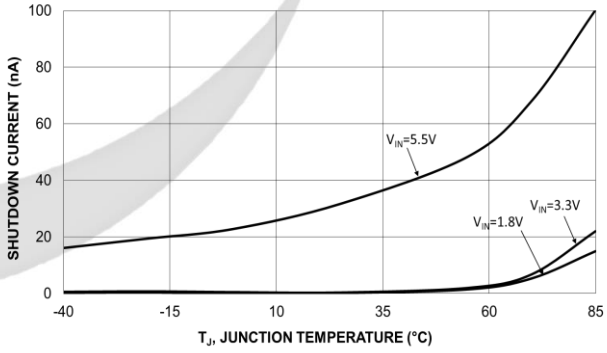


Figure 9. Shutdown Current vs. Temperature

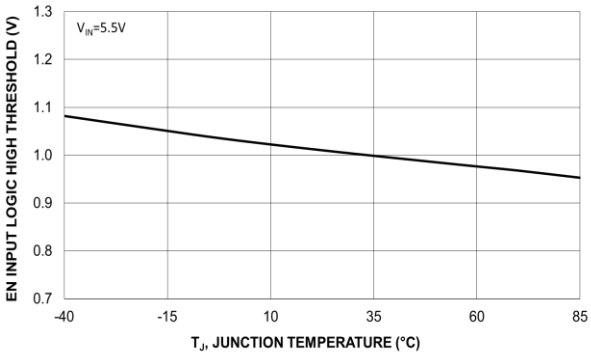


Figure 10. EN Input Logic High Threshold vs. Temperature

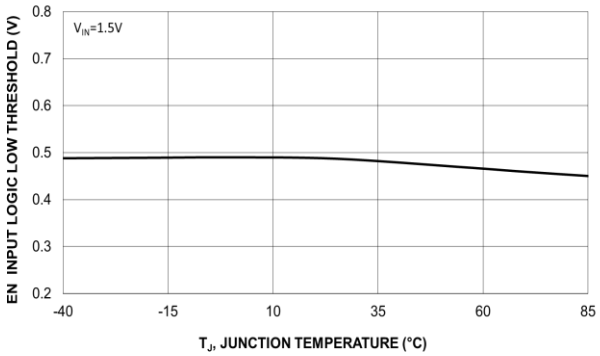


Figure 11. EN Input Logic Low Threshold vs. Temperature

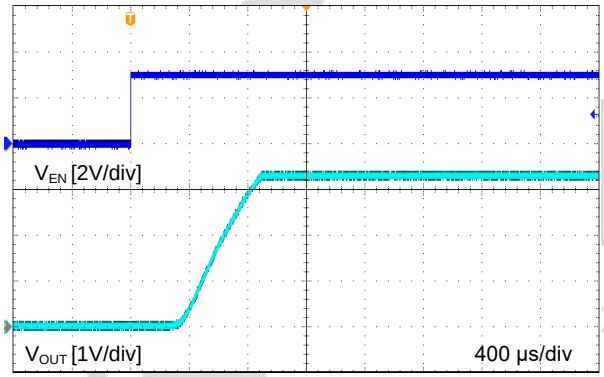


Figure 12. Turn-On Response, SR=High
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

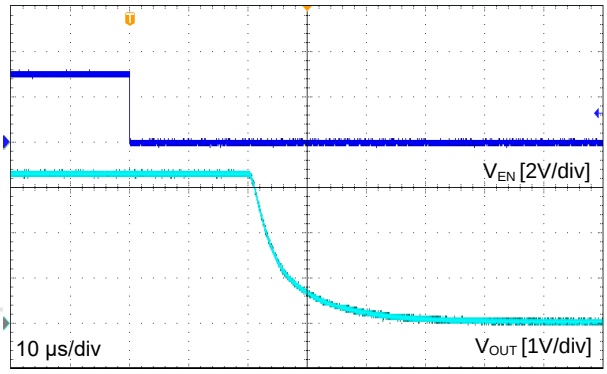


Figure 13. Turn-Off Response, SR=High
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

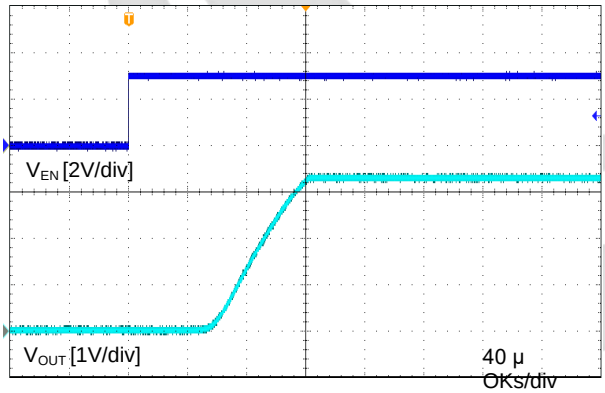


Figure 14. Turn-On Response, SR=GND
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

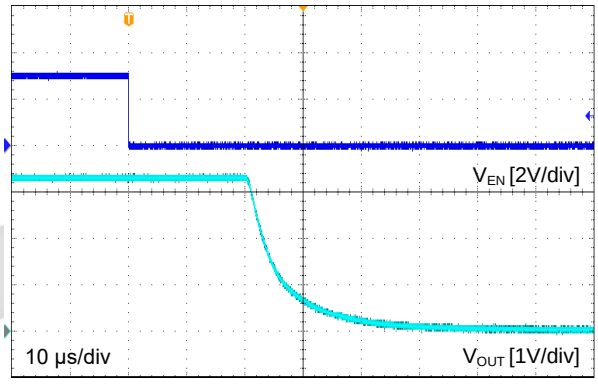


Figure 15. Turn-Off Response, SR=GND
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

APPLICATION INFORMATION

The GLF1411 is an integrated 1 A, Ultra-Efficient I_QSmart™ dual channel load switch devices with two different slew rate control to limit the inrush current during turn on. Each device is capable of operating independently over a wide input range from 1.5 V to 5.5 V with low on-resistance to reduce conduction loss. In the off state, these devices consume ultra-low leakage current to avoid unwanted standby current and save limited input power. The package is a 1.5 mm x 1.5 mm DFN-8L package, saving space in compact applications.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. The C_{OUT} capacitor should be spaced close to the VOUT and GND pins.

EN pin

The GLF1411 can be activated by forcing EN pin high level. Note that the EN pin has an internal pull-down/ pull-up resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

Slew Rate Control of Output Voltage

The slew rate of the output voltage of both channels is set by the SR pin when the GLF1411 starts up. The output voltage rise time (t_R) is slowed down with the SR pin tied to a higher potential than the logic high voltage (V_{IH}) and it becomes fast when the SR pin is grounded. See the switching performance in the electrical characteristics table as well as waveforms of Fig 12 ~ Fig 15. It provides a flexible out rising time to avoid inrush current in various applications with different output capacitance.

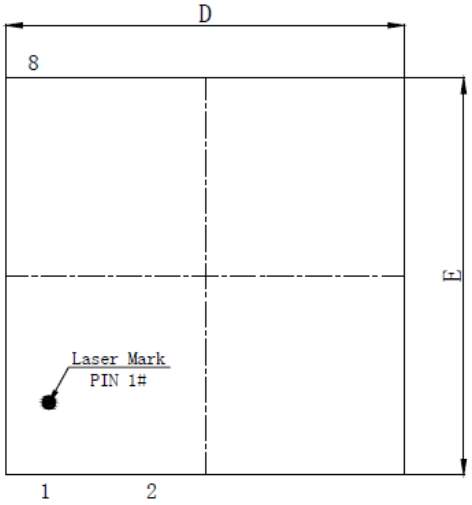
Output Discharge Function

The GLF1411 have an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly

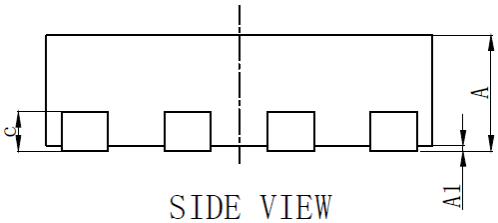
Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

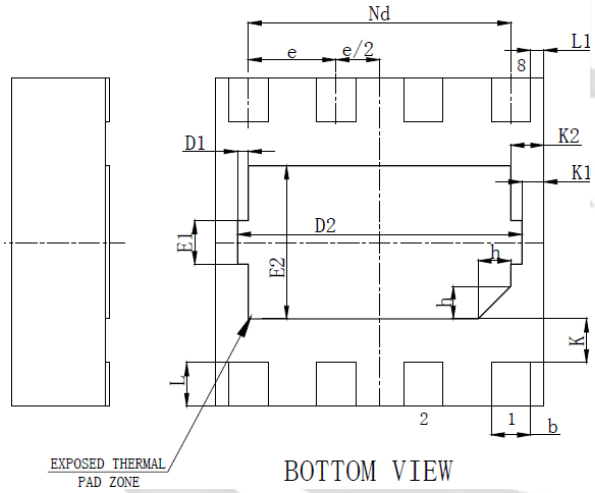
PACKAGE OUTLINE



TOP VIEW



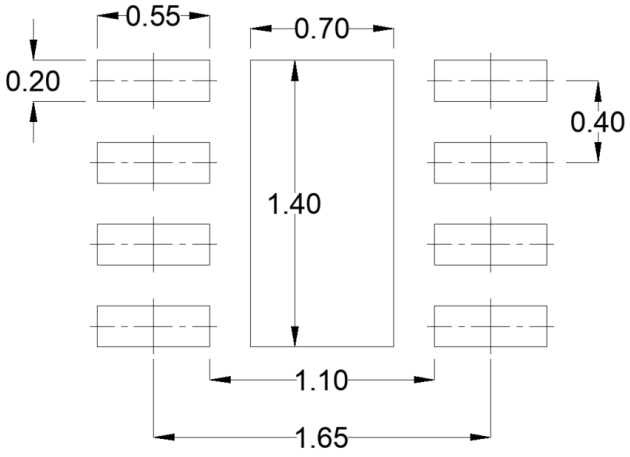
SIDE VIEW



BOTTOM VIEW

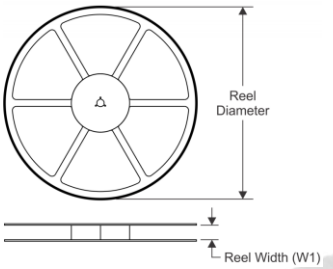
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
c	0.152REF		
D	1.45	1.50	1.55
D1	0.05REF		
D2	1.20	1.30	1.40
e	0.40BSC		
Nd	1.20BSC		
E	1.45	1.50	1.55
E1	0.20REF		
E2	0.60	0.70	0.80
L	0.15	0.20	0.25
L1	0.06REF		
K	0.20REF		
K1	0.10REF		
K2	0.15REF		
h	0.10	0.15	0.20

Recommended Footprint

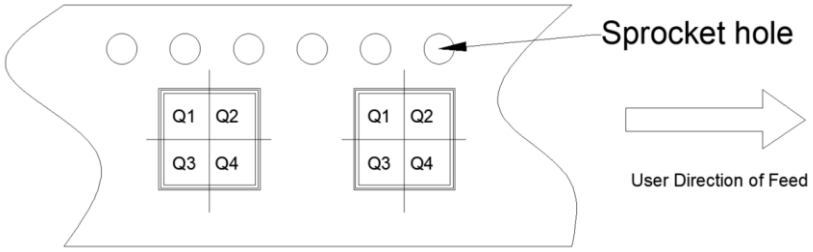


TAPE AND REEL INFORMATION

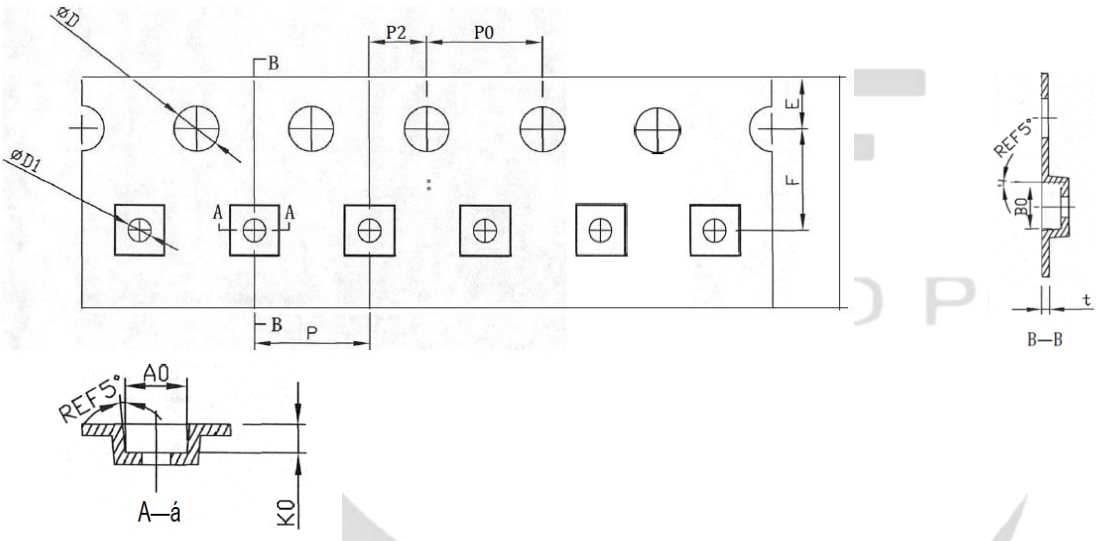
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF1411-D1G7	DFN1.5x1.5	8	3000	178	8.6	1.7	1.7	0.76	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P1: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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