

Nano-Current Consumed, I_QSmart[™] Power Load Switch with Slew Rate Control

Product Specification

DESCRIPTION

The GLF112x is an ultra-efficiency, 1.0 A rated, integrated load switch with the slew rate control. The best-in-class efficiency makes it an ideal choice for use in IoT, mobile, and wearable electronics.

The GLF112x features an ultra-efficient I_QSmart^{TM} technology that supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF112x slew rate control specifically limits inrush current during turn-on to minimize voltage droop.

FEATURES

- Wide Input Range, V_{IN} = 1.1 V to 5.5 V
 6 V_{ABS} Max
- I_{OUT} Max = 1.0 A
- Low R_{ON} = 52 m Ω Typ. at 5.5 V_{IN}
- Ultra-Low Io:

5.0 nA Typ at $5.5~V_{\text{IN}}$: GLF112xH / HN 550~nA Typ at $5.5~V_{\text{IN}}$: GLF1121L

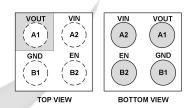
- Ultra-Low I_{SD}: 10 nA Typ at 5.5 V_{IN}
- Integrated Output Discharge Switch (Optional)
- Internal Pull-down Resistor on EN Pin: GLF112xH
- Internal Pull-up Resistor on EN Pin: GLF112xL

APPLICATIONS

- Wearables
- Mobile Devices
- Low Power Subsystems

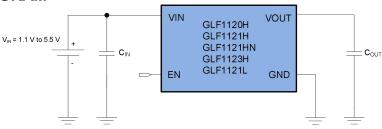
PACKAGE





0.67 mm x 0.67 mm x 0.425 mm 0.35 mm Pitch WL-CSP

APPLICATION DIAGRAM



Nano-Current Consumed, I_QSmart[™] Power Load Switch with Slew Rate Control

INTEGRATED POWER

ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R _{ON} (Typ) at V _{IN} (MAX)	V _{OUT} Rise Time at 3.3 V _{IN}	Output Discharge	EN Activity	Internal Pull up/down
GLF1120H	Т			NA		Yes
GLF1121H	U		200 up		High	Yes
GLF1121HN	V	52 mΩ	380 µs	85 Ω		NA
GLF1121L	Х			05 12	Low	Yes
GLF1123H	W		4 µs		High	Yes

FUNCTIONAL BLOCK DIAGRAM

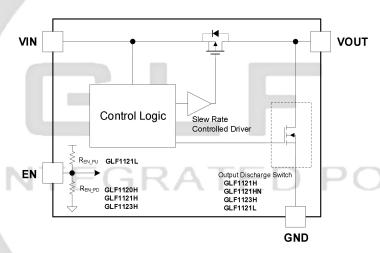
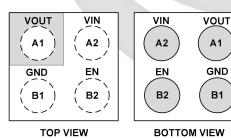


Figure 1. Functional Block Diagram

PIN CONFIGURATION



PIN DEFINITION

Pin#	Name	Description
A1	VOUT	Switch Output
A2	VIN	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch. The EN pin has an internal pull-down resistor for GLF1120H, GLF1121H, and GLF1123H and pull-up resistor for GLF1121L.

Figure 2. 0.67 mm x 0.67 mm x 0.425 mm WLCSP



ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Pa	Min.	Max.	Unit	
V _{IN} , V _{OUT} , V _{EN}	Each Pin Voltage Range to GND		-0.3	6	V
1.	Maximum Continuous Switch Current			1	Α
Іоит	Pulse, 300 us pulse and 2 % duty cycle	9		2	A
P _D	Power Dissipation at T _A = 25 °C			1	W
T _{STG}	Storage Junction Temperature			150	°C
T _A	Operating Temperature Range			85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (board dependent)			125	°C/W
ECD	Flacture static Disabarus Comphility	Human Body Model, JESD22-A114	3		147
ESD	Electrostatic Discharge Capability	Charged Device Model, JESD22-C101	2		kV

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	Supply Voltage, GLF1121x	1.1	5.5	V
TA	Ambient Operating Temperature	- 40	+ 85	°C



ELECTRICAL CHARACTERISTICS

GLF1120H, GLF1121H, GLF1121HN, GLF1123H, GLF1121L

Values are at V_{IN} = 3.3 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditi	ons	Min.	Тур.	Max.	Unit	
Basic Ope	eration					•		
V _{IN}	Supply Voltage			1.1		5.5	V	
	Quiescent Current:	V _{IN} = V _{EN} =5.5 V, I _{OUT} =0 mA			1			
. (4)	GLF1120H, GLF1121H GLF1123H, GLF1121HN	$V_{IN} = V_{EN} = 5.5 \text{ V}, I_{OUT} = 0 \text{ mA}, T$	T _A =85 °C ⁽⁴⁾		5		1	
I _Q ⁽¹⁾	Quiescent Current:	V _{IN} = 5.5 V, V _{EN} =0 V, I _{OUT} =0 mA			550		1	
	GLF1121L	V _{IN} = 5.5 V, V _{EN} =0 V, I _{OUT} =0 r	mA, T _A =85 °C ⁽⁴⁾		620		†	
		EN = Disable, I _{OUT} =0 mA, V _{IN}			2		1	
		EN = Disable, I _{OUT} =0 mA, V _{IN}			3		nA	
		EN = Disable, I _{OUT} =0 mA, V _{IN}			4		-	
I _{SD}	Shutdown Current	EN = Disable, I _{OUT} =0 mA, V _{IN}			5		1	
100		EN = Disable, I_{OUT} =0 mA, V_{IN}			10	50	-	
		EN = Disable, I _{OUT} =0 mA, V _{IN}			45	"	-	
		EN = Disable, I _{OUT} =0 mA, V _{IN}			250		-	
		Lit Biodalo, 1001 o mix, viiv	T _A =25 °C		52	60		
	On-Resistance	V_{IN} =5.5 V, I_{OUT} = 500 mA	T _A =85 °C ⁽⁴⁾		62	00	-	
			T _A =25 °C		57	65	-	
		V _{IN} =4.5 V, I _{OUT} = 500 mA	T _A =85 °C ⁽⁴⁾	117	67	00	-	
		V _{IN} =3.3 V. I _{OUT} = 500 mA		/ V	67	77	-	
Ron			T _A =85 °C ⁽⁴⁾		80	''	mΩ	
		V =2.5.V L == 200 mA	T _A =25 °C		82	92		
		V_{IN} =2.5 V, I_{OUT} = 300 mA V_{IN} =1.8 V, I_{OUT} = 300 mA	T _A =25 °C		112	125	-	
		,			142	123		
		V _{IN} =1.5 V, I _{OUT} = 100 mA	T _A =25 °C				-	
		V_{IN} =1.1 V, I_{OUT} = 100 mA V_{EN} = Low, I_{FORCE} = 10 mA, ex	T _A =25 °C		270		-	
R _{DSC}	Output Discharge Resistance	V _{EN} = High , I _{FORCE} = 10 mA for			85		Ω	
V _{IH}	EN Input Logic High Voltage	V _{IN} =1.1 V to 1.8 V V _{IN} =1.8 V to 5.5 V		0.9 1.2			V	
V _{IL}	EN Input Logic Low Voltage	V _{IN} =1.1 V to 5.5 V		1.2		0.3	, v	
R _{EN}	EN Internal resistance	Internal Pull-down Resistance			10		МΩ	
I _{EN}	EN Current	Internal Pull-up Resistance: O V _{EN} = 5.5 V GLF112xH Only	3LF1121L		0.55	0.8	μA	
	Characteristics (2)	VEN - 5.5 V GLI 112XII OIIIY			0.55	0.0	μΛ	
t _{dON}	Turn-On Delay				290		T	
t _R	V _{OUT} Rise Time	 R _L =150 Ω, C _{OUT} =0.1 μF			380		-	
t _{dOFF}	Turn-Off Delay (3), (4)	GLF1121H, GLF1121HN			16		-	
t _F	V _{OUT} Fall Time (3), (4)	_GLFT121L	GLF1121L		11			
t _{dON}	Turn-On Delay				290		μs	
t _R	V _{OUT} Rise Time				380	1	1	
t _{dOFF}	Turn-Off Delay (3), (4)	GLF1120H	·		16		-	
t _F	V _{OUT} Fall Time (3), (4)				28		†	

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t _{dON}	Turn-On Delay		15	
t _R	V _{OUT} Rise Time	R_L =150 Ω, C_{OUT} =0.1 μF	4	
t _{dOFF}	Turn-Off Delay (3), (4)	GLF1123H	15	μs
t _F	V _{OUT} Fall Time (3), (4)		11	

Notes:

- 1. I_Q does not include the EN pin current through the pull-down resistor R_{EN} .
- 2. $t_{ON} = t_{dON} + t_{R}$, $t_{OFF} = t_{dOFF} + t_{F}$
- 3. Output discharge path is enabled during off.
- 4. By design; characterized, not production tested.

TIMING DIAGRAM

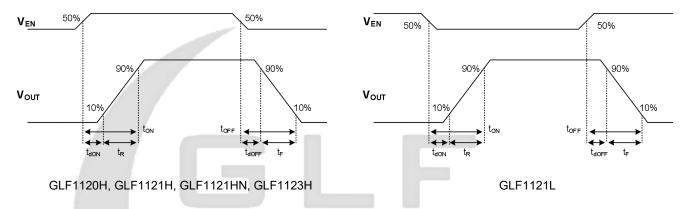


Figure 3. Timing Diagram

INTEGRATED POWER

TYPICAL PERFORMANCE CHARACTERISTICS

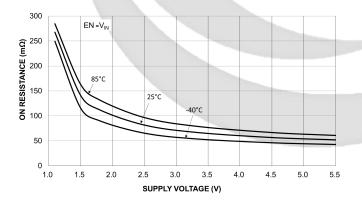


Figure 4. On-Resistance vs. Supply Voltage GLF112xH and GLF112xHN

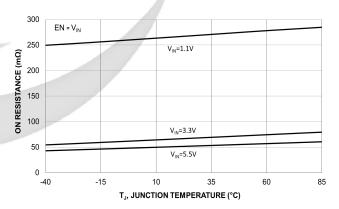


Figure 5. On-Resistance vs. Temperature GLF112xH and GLF112xHN

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INTEGRATED POWER

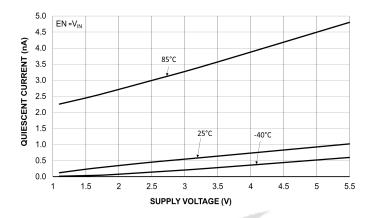


Figure 6. Quiescent Current vs. Supply Voltage GLF112xH and GLF112xHN

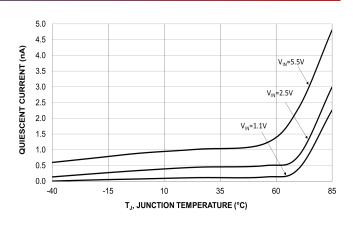


Figure 7. Quiescent Current vs. Temperature GLF112xH and GLF112xHN

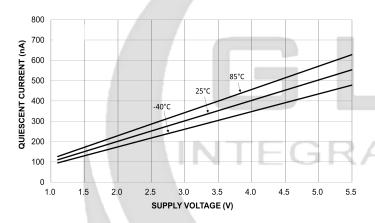


Figure 8. Quiescent Current vs. Supply Voltage GLF1121L

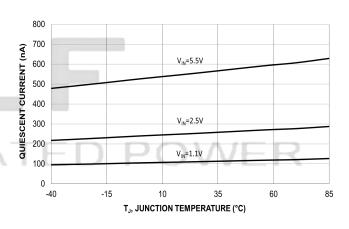


Figure 9. Quiescent Current vs. Temperature GLF1121L

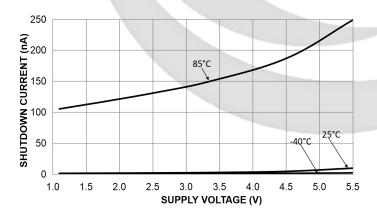


Figure 10. Shutdown Current vs. Supply Voltage

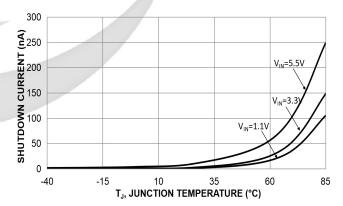


Figure 11. Shutdown Current vs. Temperature

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INTEGRATED POWER

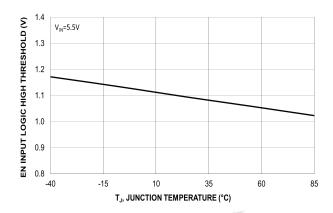
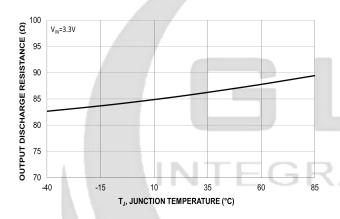


Figure 12. EN Input Logic High Threshold vs. Temperature

Figure 13. EN Input Logic Low Threshold Vs. Temperature



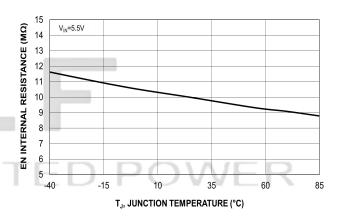
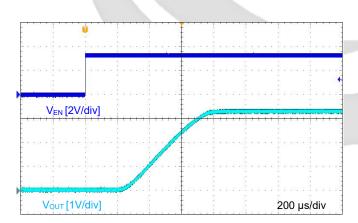


Figure 14. Output Discharge Resistance Vs. Temperature

Figure 15. EN Internal Resistance Vs. Temperature



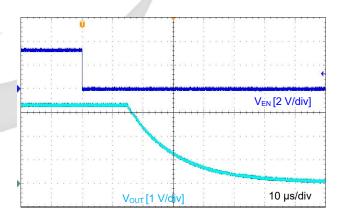


Figure 16. Turn-On Response GLF1120H V_{IN} =3.3 V, C_{IN} =1.0 μ F, C_{OUT} =0.1 μ F, R_L =150 Ω

Figure 17. Turn-Off Response, GLF1120H V_{IN} =3.3 V, C_{IN} =1.0 μF , C_{OUT} =0.1 μF , R_L =150 Ω

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INTEGRATED POWER

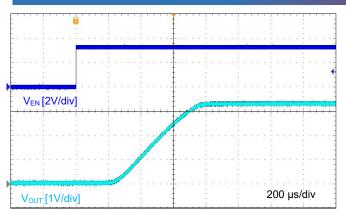


Figure 18. Turn-On Response, GLF1121H/HN V_{IN} =3.3 V, C_{IN} =1.0 μ F, C_{OUT} =0.1 μ F, R_L =150 Ω

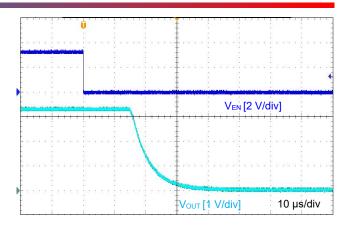


Figure 19. Turn-Off Response, GLF1121H/HN V_{IN} =3.3 V, C_{IN} =1.0 μ F, C_{OUT} =0.1 μ F, R_L =150 Ω

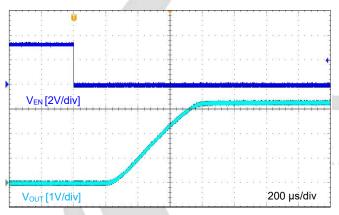


Figure 20. Turn-On Response, GLF1121L $V_{IN}\text{=}3.3~V,~C_{IN}\text{=}1.0~\mu\text{F},~C_{OUT}\text{=}0.1~\mu\text{F},~R_{L}\text{=}150~\Omega$

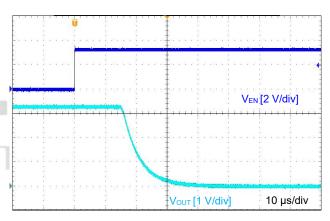


Figure 21. Turn-Off Response, GLF1121L $$V_{\text{IN}}$=3.3~V, C_{IN}=1.0~\mu\text{F}, C_{OUT}=0.1~\mu\text{F}, R_{L}=150~Ω}$

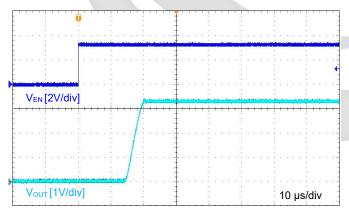


Figure 22. Turn-On Response, GLF1123H $V_{IN}\text{=}3.3~V,~C_{IN}\text{=}1.0~\mu\text{F},~C_{OUT}\text{=}0.1~\mu\text{F},~R_{L}\text{=}150~\Omega$

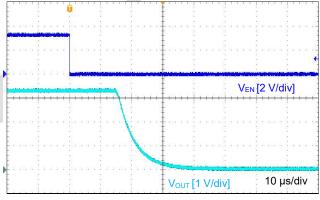


Figure 23. Turn-Off Response, GLF1123H V_{IN} =3.3 V, C_{IN} =1.0 μ F, C_{OUT} =0.1 μ F, R_L =150 Ω

Nano-Current Consumed, I_QSmart[™] Power Load Switch with Slew Rate Control

APPLICATION INFORMATION

The GLF112x product family are an integrated 1 A, ultra-efficient I_QSmart^{TM} load switch devices with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.67 mm x 0.425 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with 0.35 mm pitch for manufacturability.

Input Capacitor

The GLF112x product family do not require an input capacitor. However, to reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1 µF capacitor is recommended to be placed close to the VIN pin. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

The GLF112x product family do not require an output capacitor. However, use of an output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be spaced close to the VOUT and GND pins.

EN pin

The GLF112xH can be activated by forcing EN pin high level and the GLF112xL is activated by EN pin low level. Note that the EN pin of GLF112xH/L products has an internal pull-down/pull-up resistor to help pull the main switch to a known "off state" when no EN signal is applied from an external controller. The GLF1121HN does not have the internal pull-down resistor.

Output Discharge Function

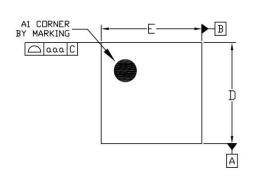
The GLF1121H, GLF1121HN, GLF1123H and GLF1121L have an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

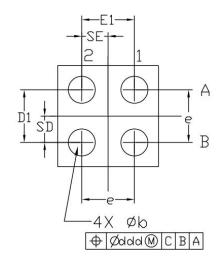
Board Layout

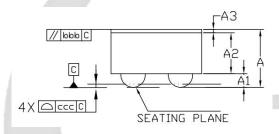
All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

Nano-Current Consumed, I_QSmart[™] Power Load Switch with Slew Rate Control

PACKAGE OUTLINE







Α	0.380	0.425	0.470			
Α1	0.085	0.100	0.115			
Α2	0.275	0.300	0.325			
Α3	0.020	0.025	0.030			
D	0.655	0.670	0.685			
Е	0.655	0.670	0.685			
D1	0.300	0.350	0.400			
E1	0.300	0.350	0.400			
Ь	0.145	0.180	0.215			
е	0.350 BSC					
SD	0.175 BSC					

0.175 BSC

0.10

0.10

0.05

0.05

Tol. of Form&Position

Dimensional Ref

Nom.

Min.

REF.

SE

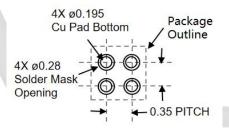
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ЬЬЬ

ccc

ddd

Recommended Footprint



Notes

- 1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
- 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
- 3. A3: BACKSIDE LAMINATION

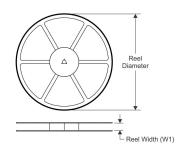


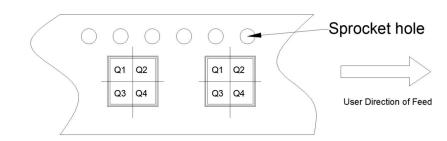
Nano-Current Consumed, I_QSmart[™] Power Load Switch with Slew Rate Control

TAPE AND REEL INFORMATION

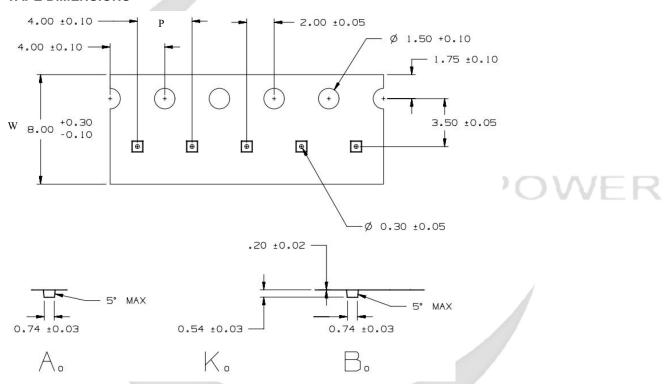
REEL DIMENSIONS

QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE





TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	Α0	В0	K0	Р	w	Pin1
GLF1120H	WLCSP	4	4000	180	9	0.74	0.74	0.54	4	8	Q1
GLF1121H	WLCSP	4	4000	180	9	0.74	0.74	0.54	4	8	Q1
GLF1121HN	WLCSP	4	4000	180	9	0.74	0.74	0.54	4	8	Q1
GLF1121L	WLCSP	4	4000	180	9	0.74	0.74	0.54	4	8	Q1
GLF1123H	WLCSP	4	4000	180	9	0.74	0.74	0.54	4	8	Q1

Remark:

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- C0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P: Pitch between successive cavity centers



SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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