GLF1401 / GLF1403

6 A Dual Channel Programmable Slew Rate Power Switch

Product Specification

DESCRIPTION

The GLF1401 / GLF1403 is a dual channel integrated load switch with the VariRise™ technology which provides the programmable slew rate of variable output voltage rising times.

Each channel of the GLF1401 / GLF1403 operates independently over an input range from 0.6 V to 5.5 V and supports 6 A maximum continuous output current per channel. The GLF1401 / GLF1403 feature supports some of the lowest R_{ON}, quiescent currents (I_Q) and shutdown currents (I_{SD}) in the industry. Low R_{ON} reduces conduction losses, while low I_Q and I_{SD} solutions help designers to improve system efficiency.

The SR input pin allows the user to add an external capacitor to set the slew rate of the switch output voltage to a specific value for a given output capacitance. It limits inrush currents during turn-on, helping to minimize voltage drop.

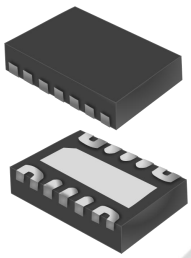
FEATURES

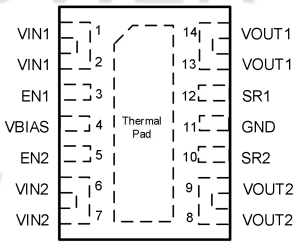
- Input Voltage Range: 0.6 V to 5.5 V
- V_{BIAS} Voltage Range: 2.5 V to 5.5 V
- 6 A Continuous Output Current Per Channel
- Low R_{ON}: 19 mΩ Typ. at V_{IN} = V_{BIAS} = 5 V
- Low Quiescent Current, I_{Q_BIAS}
  - 15 µA Typ. at $V_{IN1\ or\ 2}$ = V_{BIAS} = 5 V, Single Channel
  - 18 µA Typ. at $V_{IN1\&2}$ = V_{BIAS} = 5 V, Both Channel
- Low Shutdown Current of VIN, I_{SD_VIN}
  - 8 nA Typ. at V_{IN} = 5.5 V, Per Channel
- Programmable VOUT Rising Time
- Output Discharge Switch When Disabled
- Reverse Current Blocking Protection When Disabled
- Thermal Shutdown Protection

APPLICATIONS

- Notebook and Computing Devices
- Communication / Network System
- Storage Devices

PACKAGE





TOP VIEW

2 mm x 3 mm DFN-14L

APPLICATION DIAGRAM

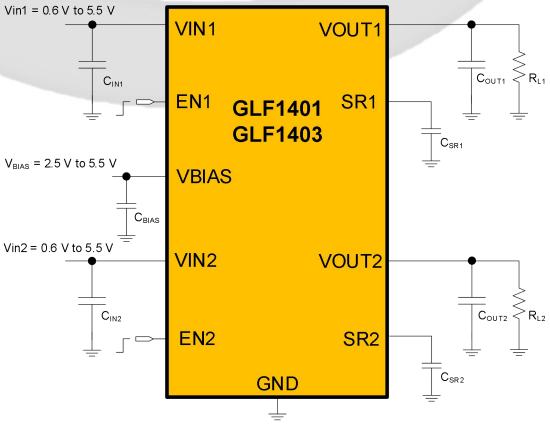
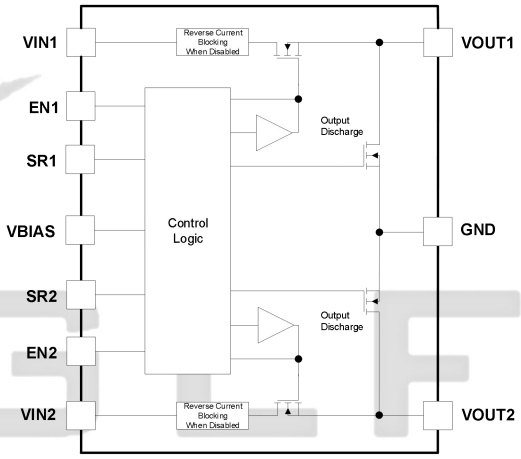


Figure 1. Functional Block Diagram

DEVICE ORDERING INFORMATION

Part Number	Top Mark	R_{ON} (Typ) at 5 V_{IN}	Output Discharge	V_{OUT} Rise Time, t_R (Typ) at 5 V_{IN}	EN Activity
GLF1401-D3G7	HD	19 mΩ	200 Ω	1.97 ms	High
GLF1403-D3G7	EG	19 mΩ	200 Ω	1 ms	High

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

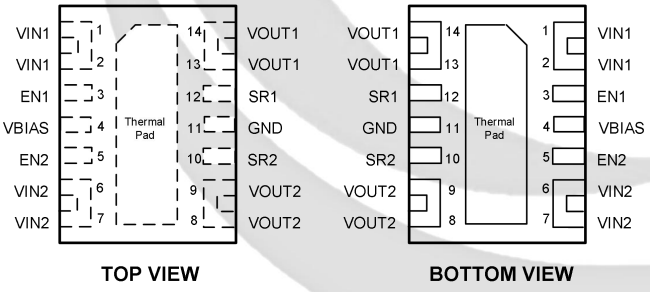


Figure 2. 2 mm x 3 mm DFN-14L

PIN DEFINITION

Pin No.	Name	Description
1, 2	VIN1	Switch 1 input.
3	EN1	Active high signal to enable switch 1 V_{EN} is recommended to be same as V_{BIAS} or no more than 1 V lower
4	VBIAS	Supply voltage for IC
5	EN2	Active high signal to enable switch 2 V_{EN} is recommended to be same as V_{BIAS} or no more than 1 V lower
6, 7	VIN2	Switch 2 input.
8, 9	VOUT2	Switch 2 output
10	SR2	Switch 2 slew rate control, connect external capacitor
11	GND	Ground
12	SR1	Switch 1 slew rate control, connect external capacitor
13, 14	VOUT1	Switch 1 output
	Thermal pad	Tie to GND

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}, V_{BIAS}	Each Pin to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			6	A
T_{STG}	Storage Junction Temperature		-65	150	°C
T_J	Operating Temperature Range			150	°C
θ_{JC}	Thermal Resistance, Junction to Case (Bottom)			10	°C/W
θ_{JA}	Thermal Resistance, Junction to Ambient			51	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	4		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	0.6	5.5	V
V_{BIAS}	Bias Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS (Per Channel)

V_{IN} = 0.6 V to 5.5 V, V_{BIAS} = 5 V, T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
I_{Q_BIAS}	V_{BIAS} Quiescent Current	$V_{IN1,2}$ = $V_{EN1,2}$ = V_{BIAS} = 5 V $I_{OUT1,2}$ = 0 mA, Both Channels			18	24	µA
		$V_{IN1,2}$ = V_{EN1} = V_{BIAS} = 5 V, V_{EN2} = 0 V $I_{OUT1,2}$ = 0 mA, Single Channel			15	20	
I_{SD_BIAS}	V_{BIAS} Shutdown Current Both Channels	$V_{EN1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V			1	2	µA
$I_{SD\_VIN1,2}$	V_{IN} Shutdown Current	$V_{IN1,2}$ = 5.5 V, $V_{EN1\&2}$ =$V_{IN2,1}$=0 V, V_{OUT} = 0 V			8	30	nA
		$V_{IN1,2}$ = 3.3 V, $V_{EN1\&2}$ =$V_{IN2,1}$=0 V, V_{OUT} = 0 V			5		
		$V_{IN1,2}$ = 1.8 V, $V_{EN1\&2}$ =$V_{IN2,1}$=0 V, V_{OUT} = 0 V			4		
		$V_{IN1,2}$ = 0.6 V, $V_{EN1\&2}$ =$V_{IN2,1}$=0 V, V_{OUT} = 0 V			3		
R_{ON}	On-Resistance	V_{IN} = 5.0 V, I_{OUT} = 200 mA	T_A = 25 °C		19	25	mΩ
			T_A = 85 °C (3)		26		
		V_{IN} = 3.3 V, I_{OUT}= 200 mA	T_A = 25 °C		19	24	
			T_A = 85 °C (3)		25		
		V_{IN} = 1.8 V, I_{OUT}= 200 mA	T_A = 25 °C		19	24	
		V_{IN} = 0.6 V, I_{OUT} = 200 mA	T_A = 25 °C		18	24	
R_{DSC}	Output Discharge Resistance (1)	V_{IN} = V_{BIAS} = 5 V, V_{EN} = 0 V			200		Ω
V_{IH}	EN Input Logic High Voltage	V_{BIAS} = 2.5 V		1.3			V
		V_{BIAS} = 5.5 V		2.1			
V_{IL}	EN Input Logic Low Voltage	V_{BIAS} = 2.5 V				0.7	
		V_{BIAS} = 5.5 V				1.4	
$I_{EN1,2}$	EN Pin Leakage	GLF1401				1.5	µA
		GLF1403				30	nA
TSD	Thermal Shutdown	30 °C Hysteresis			140		°C
Switching Characteristics (2), (3)							
t_{ON}	Turn-On Time	GLF1401 V_{IN} = 0.6 V, V_{EN} = V_{BIAS} = 5 V R_{OUT} = 10 Ω, C_{OUT} = 0.1 µF, C_{SR} = 1 nF			700		µs
t_{OFF}	Turn-Off Time				2.3		
t_R	V_{OUT} Rise Time				340		
t_F	V_{OUT} Fall Time				2		
t_{dON}	Turn-On Delay				360		
t_{ON}	Turn-On Time	GLF1401 V_{IN} = V_{EN} = V_{BIAS} = 5 V R_{OUT} = 10 Ω, C_{OUT} = 0.1 µF, C_{SR} = 1 nF			2370		
t_{OFF}	Turn-Off Time				2.3		
t_R	V_{OUT} Rise Time				1970		
t_F	V_{OUT} Fall Time				2		
t_{dON}	Turn-On Delay				400		
t_{ON}	Turn-On Time	GLF1401 V_{IN} = V_{EN} = V_{BIAS} = 3.3 V R_{OUT} = 10 Ω, C_{OUT} = 0.1 µF, C_{SR} = 1 nF			1796		
t_{OFF}	Turn-Off Time				2.3		
t_R	V_{OUT} Rise Time				1397		
t_F	V_{OUT} Fall Time				1.6		
t_{dON}	Turn-On Delay				399		

t_{ON}	Turn-On Time	GLF1403 V_{IN} = 0.6 V, V_{EN} = V_{BIAS} = 5 V R_{OUT} = 10 Ω, C_{OUT} = 0.1 μF, C_{SR} = 1 nF		469		μs
t_{OFF}	Turn-Off Time			2.4		
t_R	V_{OUT} Rise Time			221		
t_F	V_{OUT} Fall Time			1.8		
t_{dON}	Turn-On Delay			248		
t_{ON}	Turn-On Time	GLF1403 V_{IN} = V_{EN} = V_{BIAS} = 5 V R_{OUT} = 10 Ω, C_{OUT} = 0.1 μF, C_{SR} = 1 nF		1265		
t_{OFF}	Turn-Off Time			2.4		
t_R	V_{OUT} Rise Time			1002		
t_F	V_{OUT} Fall Time			1.9		
t_{dON}	Turn-On Delay			263		
t_{ON}	Turn-On Time	GLF1403 V_{IN} = V_{EN} = V_{BIAS} = 3.3 V R_{OUT} = 10 Ω, C_{OUT} = 0.1 μF, C_{SR} = 1 nF		1035		
t_{OFF}	Turn-Off Time			2.3		
t_R	V_{OUT} Rise Time			774		
t_F	V_{OUT} Fall Time			1.6		
t_{dON}	Turn-On Delay			261		

Notes: 1. Output discharge path is enabled during off.
2. t_{ON} = t_{dON} + t_R , t_{OFF} = t_{dOFF} + t_F.
3. By design; characterized, not production tested.

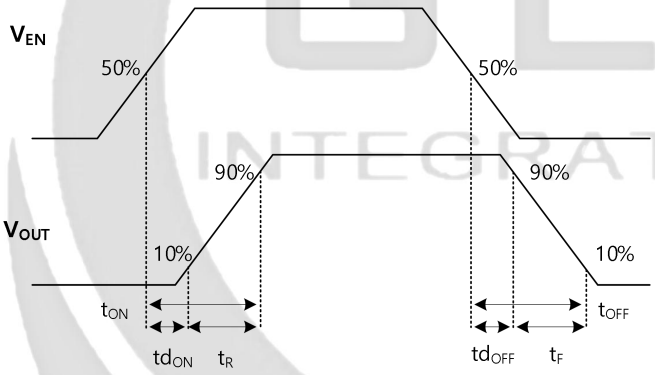


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS (Per Single Channel)

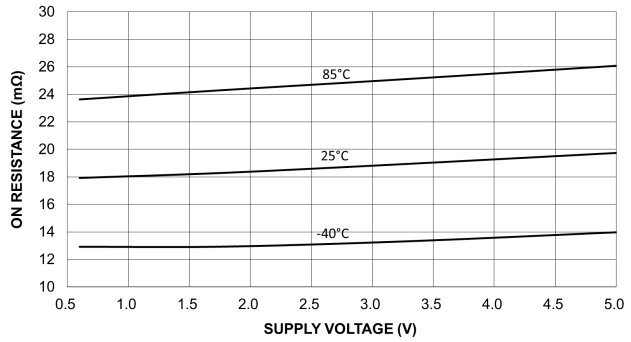


Figure 4. On-Resistance vs. Supply Voltage
V_{BIAS}= 5 V, I_{OUT}= 200 mA

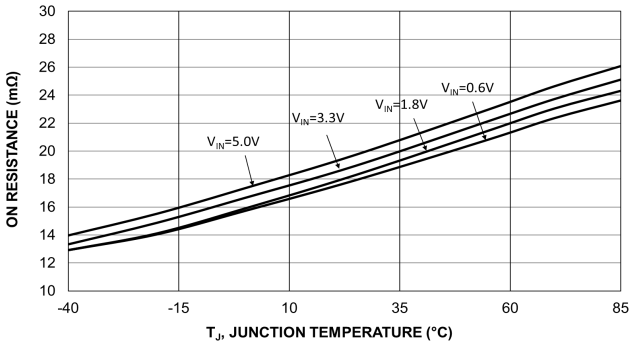


Figure 5. On-Resistance vs. Temperature
V_{BIAS}= 5 V, I_{OUT}= 200 mA

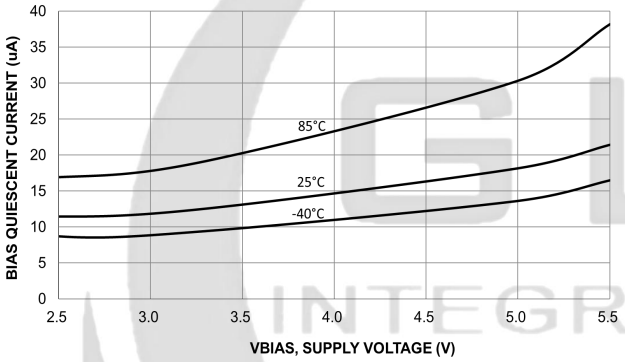


Figure 6. Quiescent Current vs. V_{BIAS} (Both Channel)
V_{IN1}=V_{IN2}=V_{BIAS}, V_{OUT}=Open

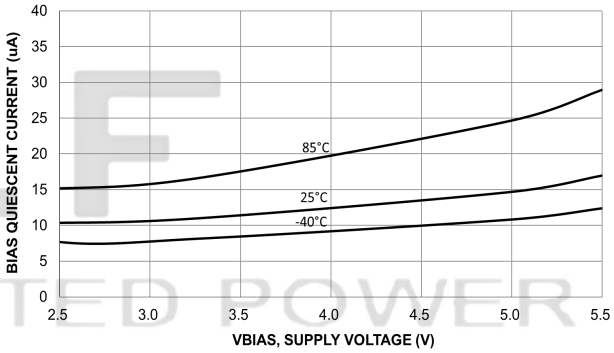


Figure 7. Quiescent Current vs. V_{BIAS} (Single Channel) V_{IN}=V_{BIAS}, V_{OUT}=Open

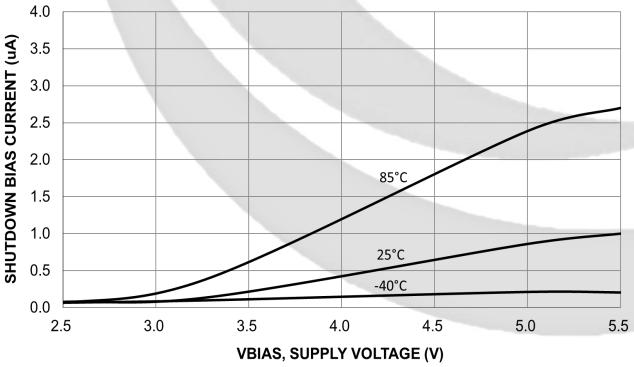


Figure 8. V_{BIAS} Shutdown Current (Both Channel)
V_{IN1}=V_{IN2}=0 V, V_{EN1}=V_{EN} =0 V, V_{OUT}=Open

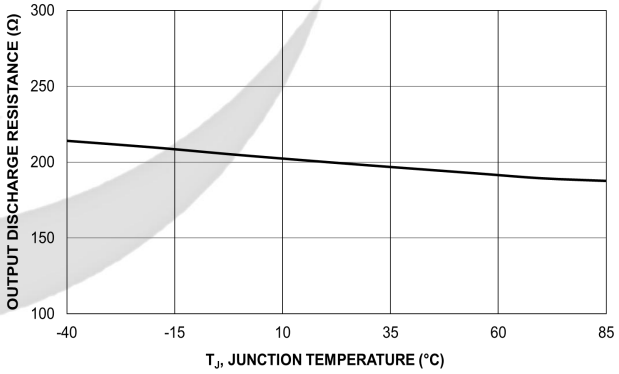


Figure 9. Output Discharge Resistance vs. Temperature

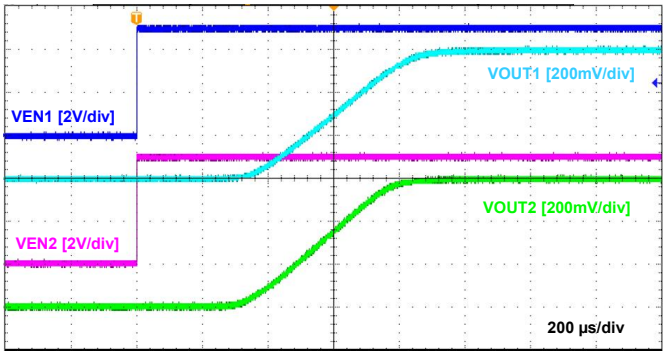


Figure 10. Turn-On Response, GLF1401

V_{IN}=0.6 V, V_{EN}=V_{BIAS}=5 V, C_{IN}=C_{OUT}= 0.1 µF, C_{SR}=1 nF, R_L=10 Ω

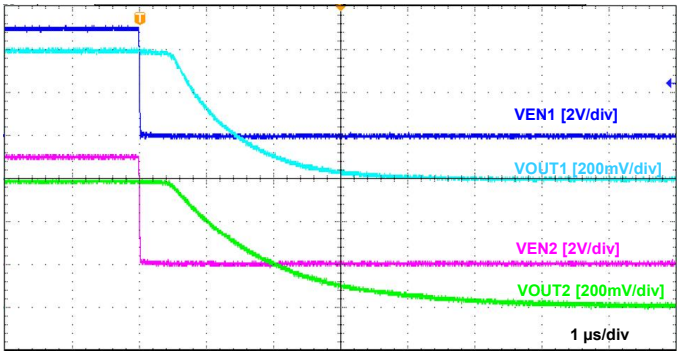


Figure 11. Turn-Off Response, GLF1401

V_{IN}=0.6 V, V_{EN}=V_{BIAS}=5 V, C_{IN}=C_{OUT}= 0.1 µF, C_{SR}=1 nF, R_L=10 Ω

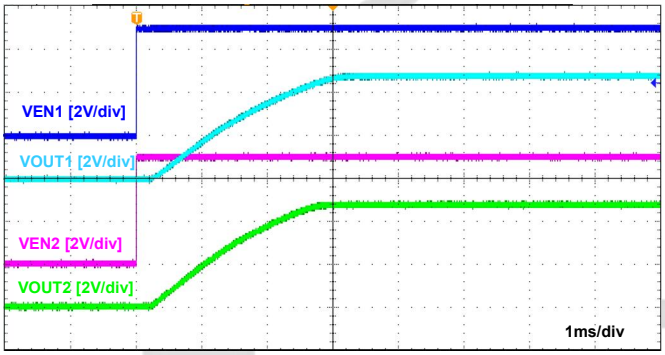


Figure 12. Turn-On Response, GLF1401

V_{IN}=V_{EN}=V_{BIAS}=5 V, C_{IN}=C_{OUT}= 0.1 µF, C_{SR}=1 nF, R_L=10 Ω

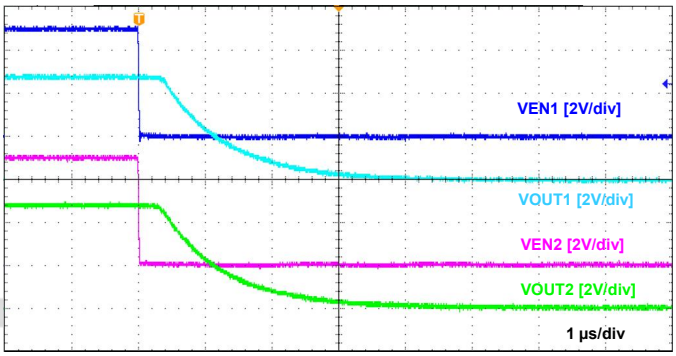


Figure 13. Turn-Off Response, GLF1401

V_{IN}=V_{EN}=V_{BIAS}=5 V, C_{IN}=C_{OUT}= 0.1 µF, C_{SR}=1 nF, R_L=10 Ω

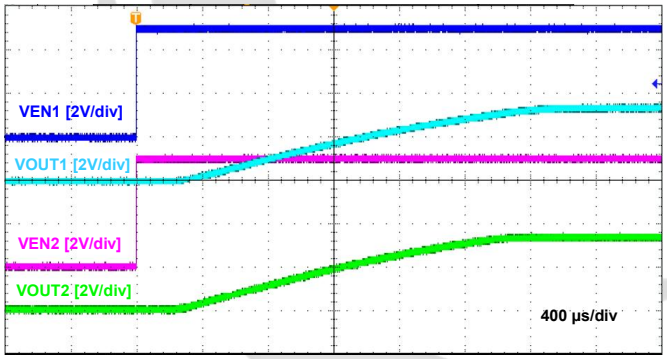


Figure 14. Turn-On Response, GLF1401

V_{IN}=V_{EN}=V_{BIAS}=3.3 V, C_{IN}=C_{OUT}=0.1 µF, C_{SR}=1 nF, R_L=10 Ω

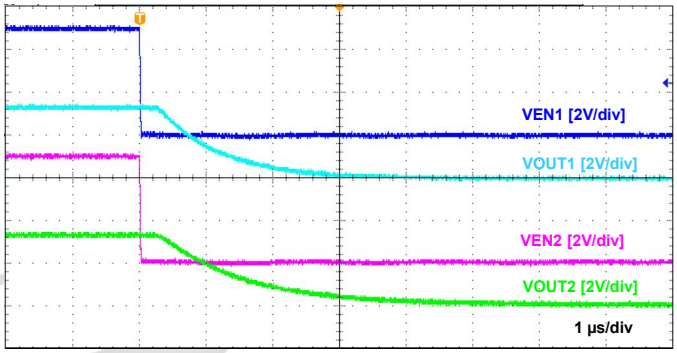


Figure 15. Turn-Off Response, GLF1401

V_{IN}=V_{EN}=V_{BIAS}=3.3 V, C_{IN}=C_{OUT}=0.1 µF, C_{SR}=1 nF, R_L=10 Ω

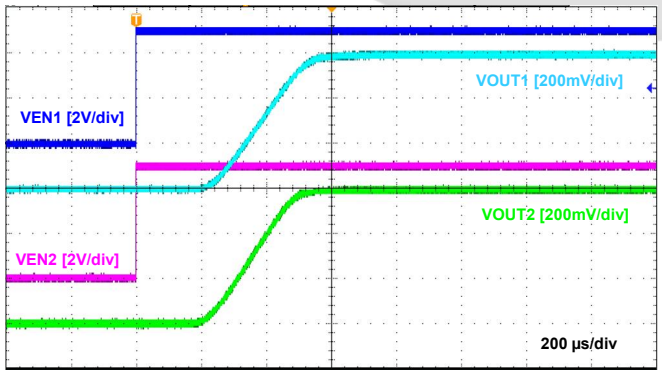


Figure 16. Turn-On Response, GLF1403

V_{IN}=0.6 V, V_{EN}=V_{BIAS}=5 V, C_{IN}=C_{OUT}= 0.1 µF, C_{SR}=1 nF, R_L=10 Ω

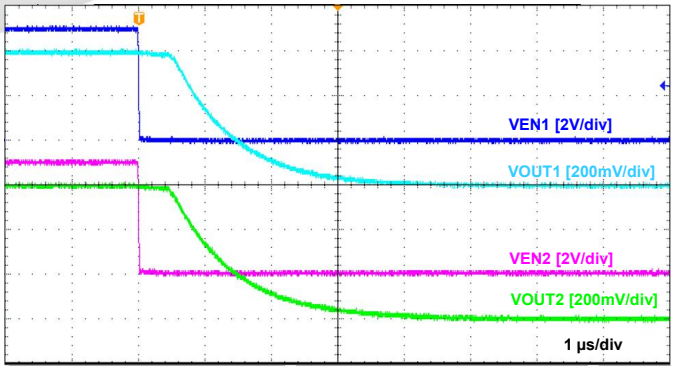


Figure 17. Turn-Off Response, GLF1403

V_{IN}=0.6 V, V_{EN}=V_{BIAS}=5 V, C_{IN}=C_{OUT}= 0.1 µF, C_{SR}=1 nF, R_L=10 Ω

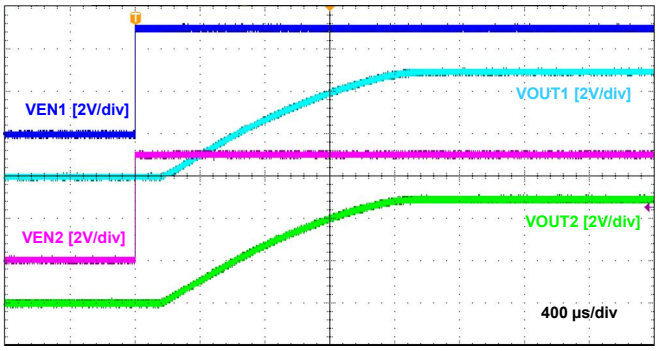


Figure 18. Turn-On Response, GLF1403
V_{IN}=V_{EN}=V_{BIAS}=5 V, C_{IN}=C_{OUT}= 0.1 µF, C_{SR}=1 nF, R_L=10 Ω

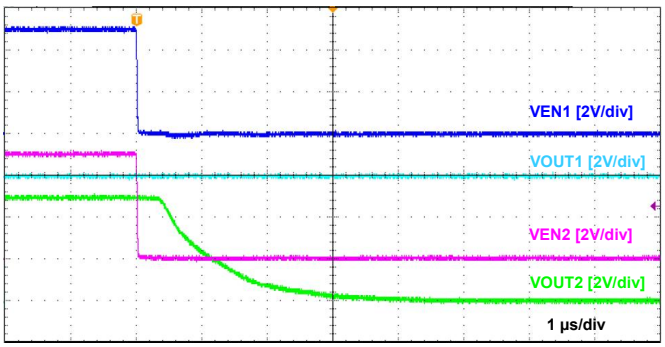


Figure 19. Turn-Off Response, GLF1403
V_{IN}=V_{EN}=V_{BIAS}=5 V, C_{IN}=C_{OUT}= 0.1 µF, C_{SR}=1 nF, R_L=10 Ω

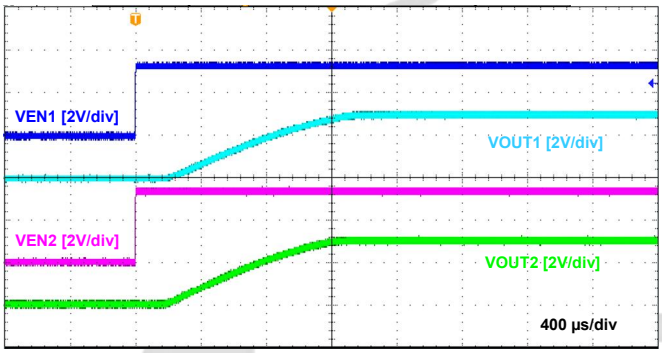


Figure 20. Turn-On Response, GLF1403
V_{IN}=V_{EN}=V_{BIAS}=3.3 V, C_{IN}=C_{OUT}=0.1 µF, C_{SR}=1 nF, R_L=10 Ω

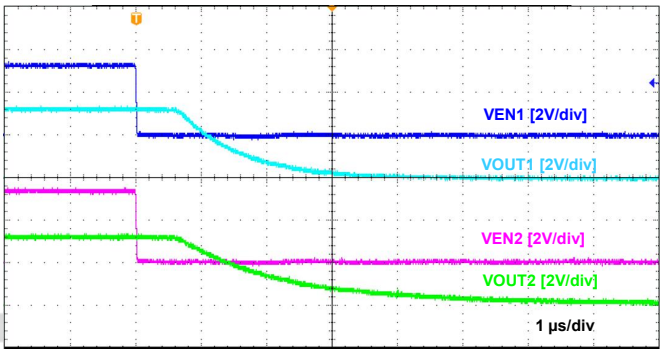


Figure 21. Turn-Off Response, GLF1403
V_{IN}=V_{EN}=V_{BIAS}=3.3 V, C_{IN}=C_{OUT}=0.1 µF, C_{SR}=1 nF, R_L=10 Ω

APPLICATION INFORMATION

The GLF1401 / GLF1403 is a 6 A fully integrated load switch with the VariRise™ programmable slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range which from 0.6 V to 5.5 V with very low on-resistance to reduce conduction loss. At off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power supply.

Programmable Slew Rate of Output Voltage

An external capacitor between the SR and GND pin sets the output voltage slew rate of each channel individually. The SR pin is not recommended to be open. The table 1 and table 2 can also be used to choose C_{SR} value quickly.

C_{SR} (pF)	**Input Voltage, V_{IN}** V_{EN}=V_{BIAS} = 5 V, C_{OUT} = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, T_A = 25 °C						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.6 V
0	265	214	157	138	113	100	71
220	597	450	297	260	207	192	120
470	870	613	448	390	298	300	173
1000	1970	1378	860	755	571	540	340
2200	3386	2538	1579	1358	1045	1022	580
4700	8477	5994	3587	2986	2234	2240	1234
10000	15130	11200	6994	5845	4343	4167	2498

Table 1. GLF1401 V_{OUT} Rise Time (us) vs. C_{SR}

C_{SR} (pF)	Input Voltage, V_{IN} V_{EN}=V_{BIAS} = 5 V, C_{OUT} = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, T_A = 25 °C						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.6 V
0	158	140	97	96	83	71	54
220	371	304	194	175	149	132	91
470	554	446	274	237	215	185	128
1000	1002	809	480	429	395	340	221
2200	2262	1762	1074	922	818	683	457
4700	4291	3395	2013	1743	1538	1324	846
10000	9495	7317	4402	3628	3296	2789	1840

Table 2. GLF1403 V_{OUT} Rise Time (us) vs. C_{SR}

Input and Output Capacitor

A minimum 0.1 µF input capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop. Also, a minimum 0.1 µF output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

EN pin

The GLF1401 / GLF1403 can be activated by EN pin high. Note that the EN pin of the GLF1401 has an internal pull-down resistor that maintains a reliable status without EN signal applied from an external controller. The EN pin of the GLF1403 doesn't have this resistor. V_{EN} is recommended to be same as V_{BIAS} or no more than 1 V lower to keep a low VBIAS quiescent current (I_{Q_BIAS}).

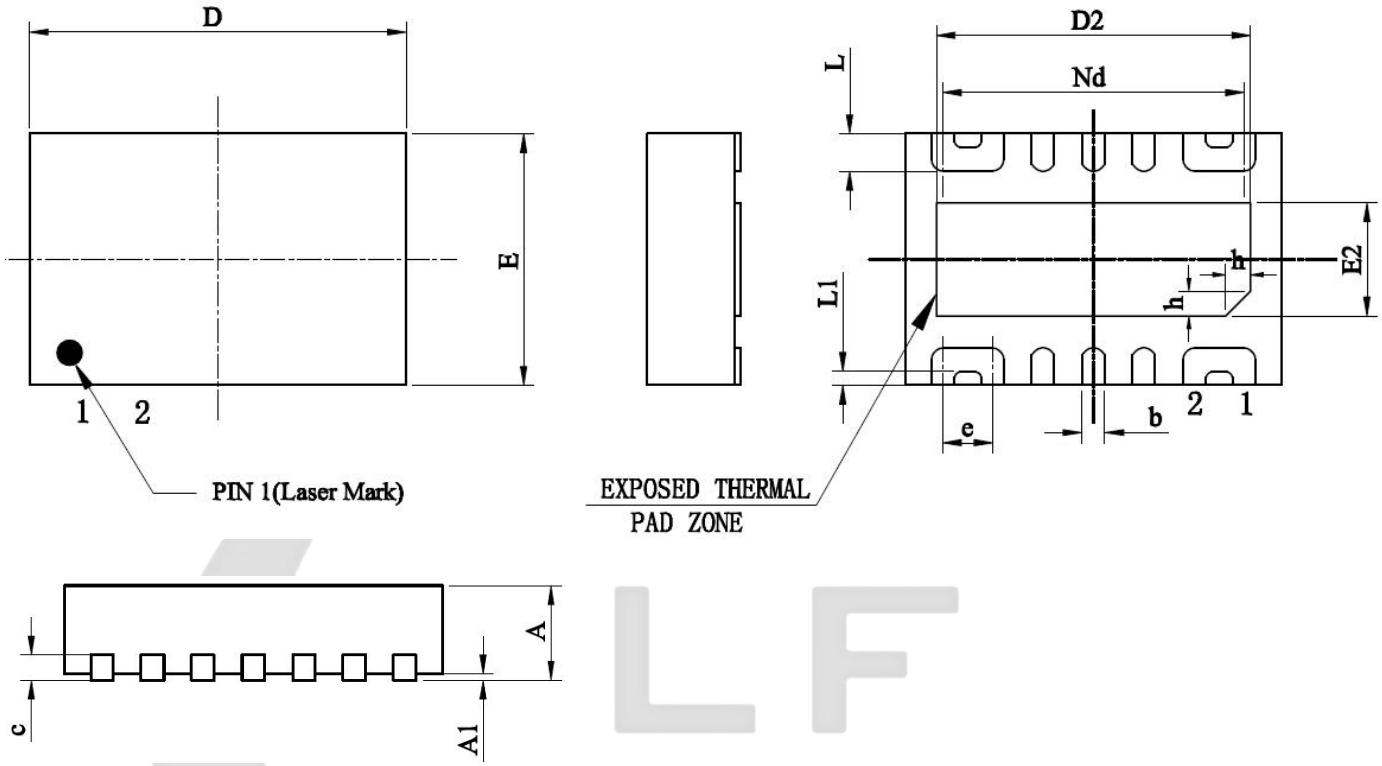
Output Discharge Function

When the EN signal of the GLF1401 / GLF1403 turns into an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

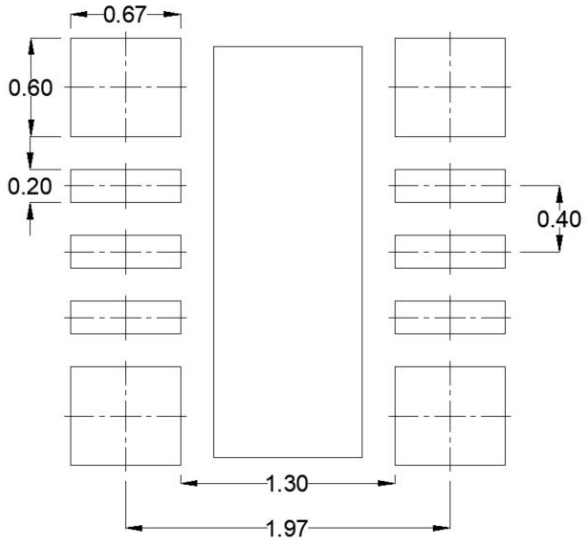
All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT and GND reduce parasitic effects at dynamic operations and improve thermal performance at high load current. Thermal vias under the exposed thermal pad of the GLF1401 / GLF1403 enhances power dissipation along with a ground plane.

PACKAGE OUTLINE



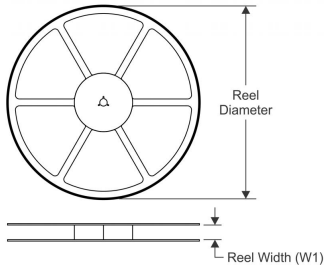
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.01	0.02	0.05
b	0.13	0.18	0.23
c	0.15	0.20	0.25
D	2.95	3.00	3.05
D2	2.45	2.50	2.55
e	0.40BSC		
Nd	2.40BSC		
E	1.95	2.00	2.05
E2	0.85	0.90	0.95
L	0.25	0.30	0.35
L1	0.06	0.11	0.16
h	0.20REF		

Recommended Footprint

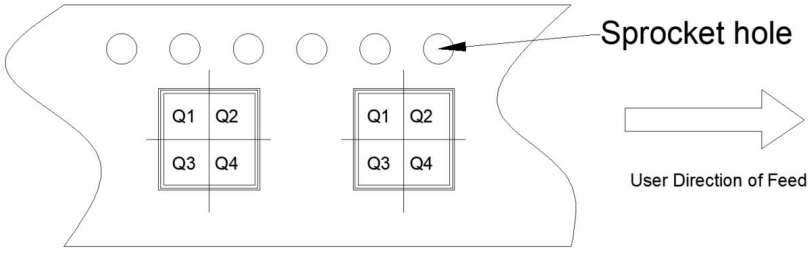


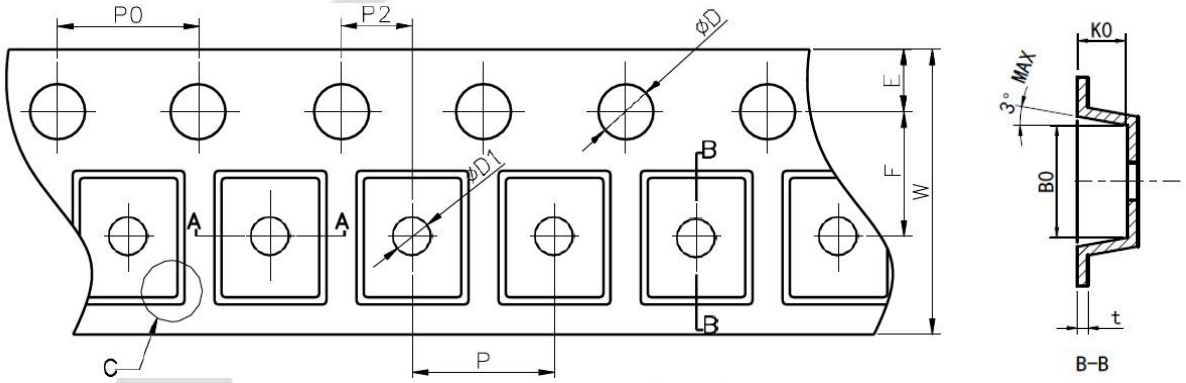
TAPE AND REEL INFORMATION

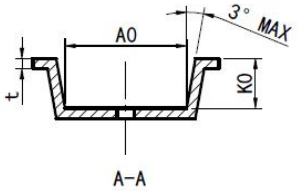
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE







Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF1401-D3G7	DFN2x3	14	3000	178	8.6	2.3	3.3	0.95	4	8	Q1
GLF1403-D3G7	DFN2x3	14	3000	178	8.6	2.3	3.3	0.95	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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