GLF4003

Ultra-low I_Q, Asymmetrical Power Mux IC with Priority, Auto & Manual Input Selection

Product Specification

DESCRIPTION

The GLF4003 is an integrated power multiplexer IC with dual independent power switches connected to a single output pin to enable seamless transition between two input sources. The GLF4003 features asymmetrical power FET characteristics. Channel 1 (VIN1) provides lower conduction resistance to support 2.0 A continuous current capability. The current rating of another channel (VIN2) is 1.5 A. It is an ideal solution for a power system with an internal back up power source.

The GLF4003 provides an automatic selection, a manual selection and VIN1 priority selection mode. The switching of these three modes is executed by combining the EN and SEL pin settings. The EN input pin has an internal threshold voltage to offer a preference to select the channel 1 (VIN1) power source. In the automatic input selection mode, the GLF4003 automatically selects a higher input voltage source between two input power sources.

The GLF4003 prevents cross conduction current between two input sources. When VOUT is higher than VIN, the GLF4003 prevents the reverse current from the output to the input, no matter which input supply is applied.

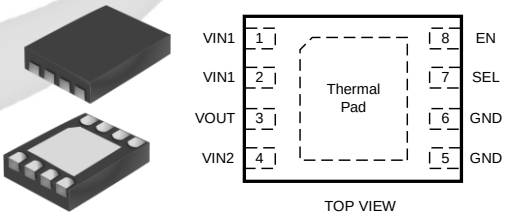
FEATURES

- Two-Input and Single-Output Power Multiplexer IC
- Auto and Manual Input Selection Mode
- VIN1 Priority Selection Mode
- Wide Input Range: 1.5 V to 4.8 V
- Low R_{ON}
  - Channel 1, VIN1 = 45 mΩ Typ at 4.8 V_{IN1}
  - Channel 2, VIN2 = 77 mΩ Typ at 4.8 V_{IN2}
- I_{OUT} Max
  - Channel 1 = 2.0 A
  - Channel 2 = 1.5 A
- Ultra-Low Supply Current at Operation
  - I_Q : 1.1 µA Typ at 4.8 V_{IN}
- Ultra-Low Stand-by Current
  - I_{SD} : 400 nA Typ at 4.8 V_{IN}
- Reverse Current Blocking Protection
- Operating Temperature Range:
  -40 °C to 85 °C

APPLICATIONS

- Smart Devices
- Subsystem with Backup Power
- IoT Tracking System
- Communication / Network System
- E-Meters and Motor Drives

PACKAGE



2 mm x 3 mm DFN-8L

PRODUCT INFORMATION

Part Number	Top Mark	Channel 1 (VIN1)		Channel 2 (VIN2)		Package
		R_{ON1} at 4.8 V_{IN}	I_{OUT}	R_{ON2} at 4.8 V_{IN}	I_{OUT}	
GLF4003-D3G7	HG	45 mΩ	2.0 A	77 mΩ	1.5 A	DFN 2x3-8L

FUNCTIONAL BLOCK DIAGRAM

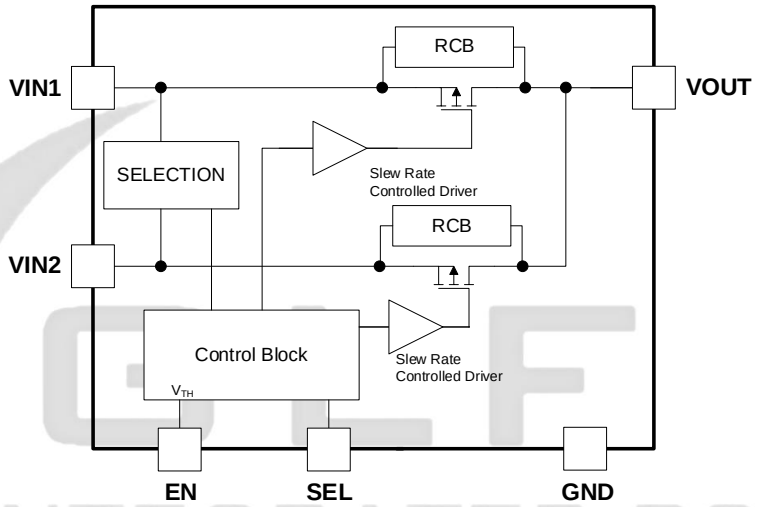


Figure 1. Functional Block Diagram

PIN CONFIGURATION

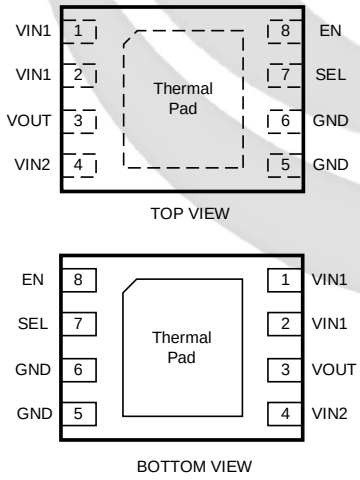


Figure 2. 2 mm x 3mm DFN-8L

PIN DEFINITION

Pin #	Name	Description
1, 2	VIN1	IC Input 1
3	VOUT	IC Output
4	VIN2	IC Input 2
5, 6	GND	Ground
7, 8	SEL, EN	Logic control, SEL and EN high and low combinations determine the selection mode. Refer to table 1.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN1}, V_{IN2}, V_{OUT}	Each Pin Voltage Range to GND		-0.3	6	V
V_{EN}, V_{SEL}	Control Pin Voltage		-0.3	6	V
I_{OUT}	Continuous Current through VIN1			2.0	A
	Continuous Current through VIN2			1.5	A
T_J	Maximum Junction Temperature			125	°C
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Ambient Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			110	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	±2		kV
		Charged Device Model, JESD22-C101	±2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN1}, V_{IN2}	Input Voltage	1.5	4.8	V
V_{EN}, V_{SEL}	Control Pin Voltage	0	4.8	V

ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = 1.5 V to 4.8 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Basic Operation							
$I_{STBY\_VIN1,2}$	VIN Unselect Channel Standby Current	V_{IN1} = 4.8 V, I_{OUT} = 0 mA SEL=VIN1, EN= 0 V, VOUT=VIN2 or V_{IN2} = 4.8 V, I_{OUT} = 0 mA EN=SEL=VIN2, VOUT=VIN1	T_A = 25 °C		0.9	1.1	µA
			T_A = 85 °C		1.2		
$I_{Q\_VIN1,2}$	VIN Quiescent Current	V_{IN1} = 4.8 V, I_{OUT} = 0 mA EN=SEL=VIN1, VOUT=VIN1 or V_{IN2} = 4.8 V, I_{OUT} = 0 mA EN=VIN1, SEL= 0 V, VOUT=VIN2	T_A = 25 °C		1.1	1.6	
			T_A = 85 °C		1.5		
$I_{SD\_VIN1,2}$	VIN Shutdown Current	$V_{IN1,2}$= 4.8 V, V_{SEL}= 0 V, V_{EN}= 4.8 V V_{OUT} = High-Z	T_A = 25 °C		0.4	0.7	µA
			T_A = 85 °C		0.9		
I_{EN}, I_{SEL}	EN and SEL Pin Leakage	V_{EN} = V_{SEL} = 4.8 V			4		nA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{ON}	Channel 1 On-Resistance	V_{IN1} = 4.8 V, I_{OUT} = 200 mA	T_A = 25 °C		45	52	mΩ
			T_A = 85 °C		54		
		V_{IN1} = 3.3 V, I_{OUT} = 200 mA	T_A = 25 °C		49	56	
			T_A = 85 °C		58		
		V_{IN1} = 1.8 V, I_{OUT} = 200 mA	T_A = 25 °C		62	70	
			T_A = 85 °C		75		
		V_{IN1} = 1.5 V, I_{OUT} = 200 mA	T_A = 25 °C		71	79	
			T_A = 85 °C		83		
	Channel 2 On-Resistance	V_{IN2} = 4.8 V, I_{OUT} = 200 mA	T_A = 25 °C		77	84	
			T_A = 85 °C		91		
		V_{IN2} = 3.3 V, I_{OUT} = 200 mA	T_A = 25 °C		84	90	
			T_A = 85 °C		99		
		V_{IN2} = 1.8 V, I_{OUT} = 200 mA	T_A = 25 °C		109	115	
			T_A = 85 °C		132		
		V_{IN2} = 1.5 V, I_{OUT} = 200 mA	T_A = 25 °C		125	132	
			T_A = 85 °C		145		
V_{TH}	EN Pin Threshold Voltage	V_{IN1} or V_{IN2} = 1.5 V to 4.8 V			1.0	1.1	V
		Hysteresis			50		mV
V_{IH}	SEL Input Logic High Voltage	V_{IN1} or V_{IN2} = 1.5 V to 4.8 V		1.2			V
V_{IL}	SEL Input Logic Low Voltage	V_{IN1} or V_{IN2} = 1.5 V to 4.8 V				0.3	
Reverse Current Blocking Protection							
t_{RCB}	RCB Response Time (1)	V_{OUT} > Selected V_{IN} + 1 V			2		µs
V_{RCB_TH}	RCB Protection Threshold	V_{OUT} – V_{IN}			110		mV
V_{RCB_RL}	RCB Protection Release	V_{IN} – V_{OUT}			45		mV
I_{RCB}	RCB activation current (1)				1.44		A
Switching Characteristics							
V_{TR}	Auto Input Selection Trigger(1)	V_{INX} – V_{INY}, In automatic selection mode			120		mV
t_{SW}	Switching Over time In Manual Mode (1)	V_{IN1} to V_{IN2}	V_{IN1} = 4.2 V, V_{IN2} = 3.6 V, C_{OUT} = 10 µF, R_L = 10 Ω		35		µs
		V_{IN2} to V_{IN1}			17		
t_{dON}	Turn-On Delay time Channel 1	V_{IN1} = 4.2 V	C_{OUT} = 10 µF, R_L = 100 Ω		1123		
		V_{IN1} = 3.3 V			1107		
		V_{IN1} = 1.8 V			1102		
	Turn-On Delay time Channel 2	V_{IN2} = 4.2 V			718		
		V_{IN2} = 3.3 V			712		
		V_{IN2} = 1.8 V			711		
t_R	VOUT Rise Time Channel 1	V_{IN1} = 4.2 V			1480		
		V_{IN1} = 3.3 V			1226		
		V_{IN1} = 1.8 V			828		
	VOUT Rise Time Channel 2	V_{IN2} = 4.2 V			872		
		V_{IN2} = 3.3 V			729		
		V_{IN2} = 1.8 V			506		

Notes: 1. By design; characterized, not production tested.

APPLICATION DIAGRAM

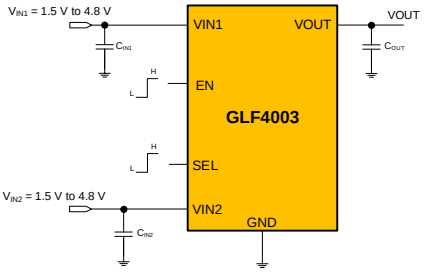


Figure 3. Manual Selection Mode

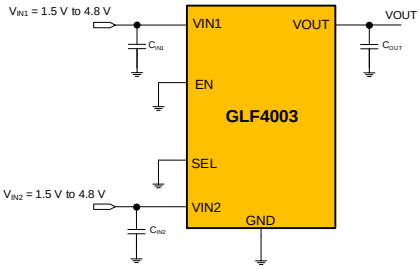


Figure 4. Auto Selection Mode

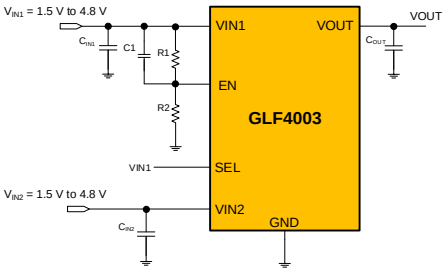


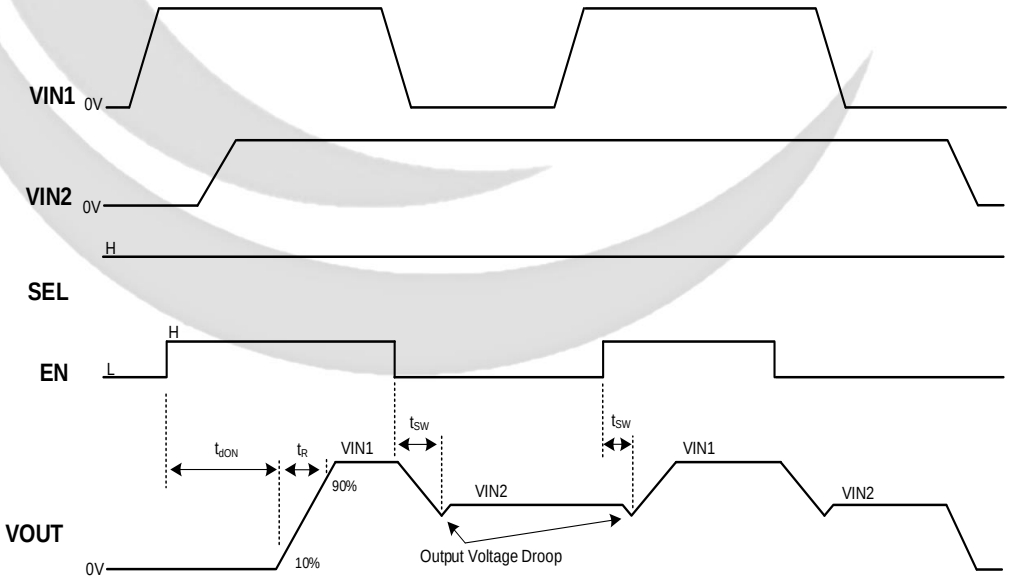
Figure 5. VIN1 Priority Selection Mode

TRUTH TABLE AND TIMING DIAGRAM

Mode	SEL	EN	VOUT	Function
Manual	High	> V_{TH}	VIN1	VIN1 is selected
	High	< V_{TH}	VIN2	VIN2 is selected
	Low	> V_{TH}	High-Z	Both channels are off
Auto	Low	< V_{TH}	Higher voltage between VIN1 and VIN2	Auto-Input selection
VIN1 Priority	Connect to VIN1	> V_{TH} by resistor divider from VIN1	VIN1	VIN1 is selected
		< V_{TH} by resistor divider from VIN1	VIN2	VIN2 is selected

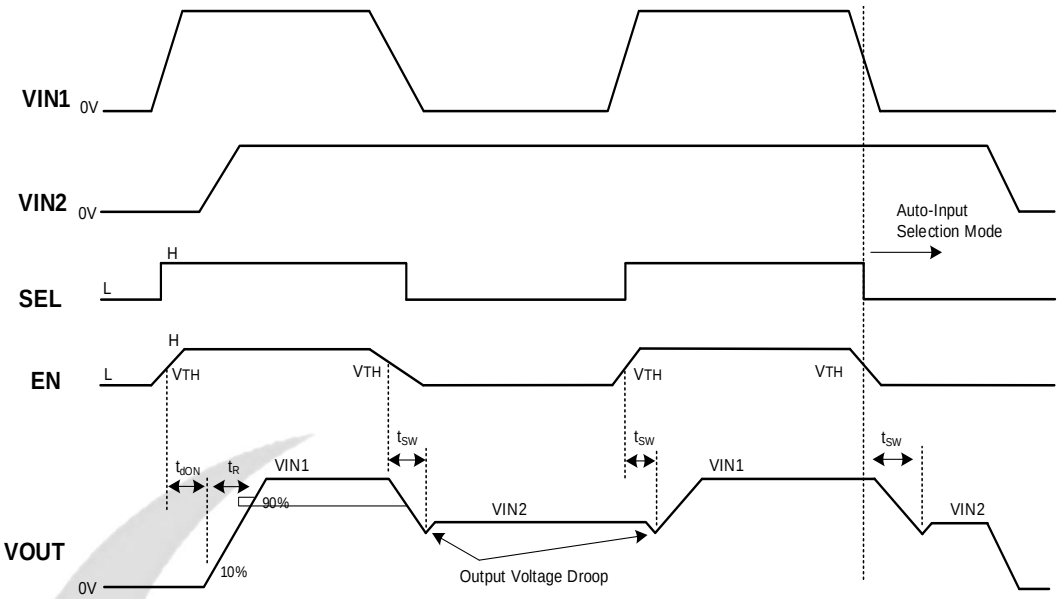
Note) V_{INX} or V_{INY} ≥ 1.5 V, High = V_{SEL} > V_{IH}, Low = V_{SEL} < V_{IL}

Table 1. Truth Table of Input Source Selection



Note) High = V_{SEL} > V_{IH}, V_{EN} > V_{TH}; Low = V_{SEL} < V_{IL}, V_{EN} < V_{TH}

Figure 6. Timing Diagram, Manual Mode (Figure 3) with EN controlled by GPIO



Note) High = $V_{SEL} > V_{IH}$, $V_{EN} > V_{TH}$; Low = $V_{SEL} < V_{IL}$, $V_{EN} < V_{TH}$

Figure 7. Timing Diagram, VIN1 Priority Selection Mode (Figure 5) with SEL tied to VIN1

TYPICAL PERFORMANCE CHARACTERISTICS

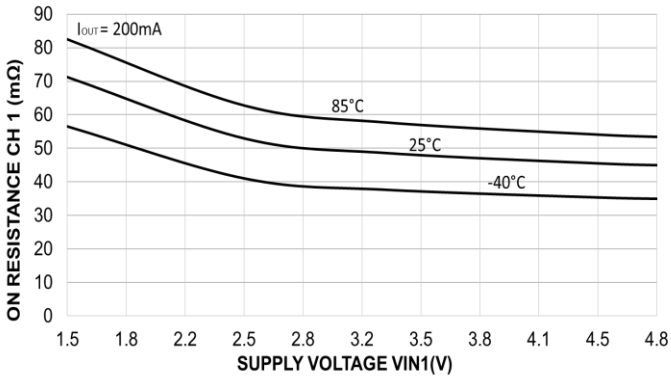


Figure 8. On-Resistance vs. Supply Voltage, Channel 1

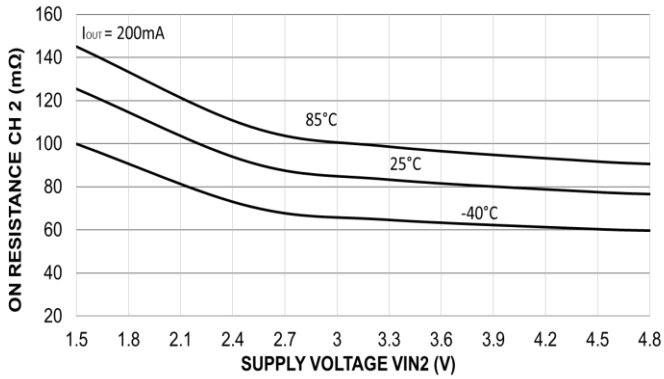


Figure 9. On-Resistance vs. Supply Voltage, Channel 2

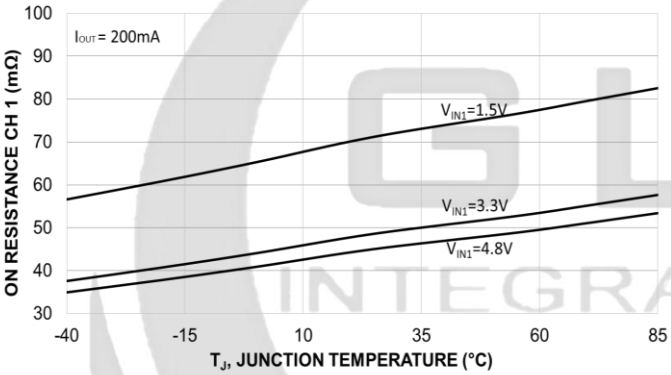


Figure 10. On-Resistance vs. Temperature, Channel 1

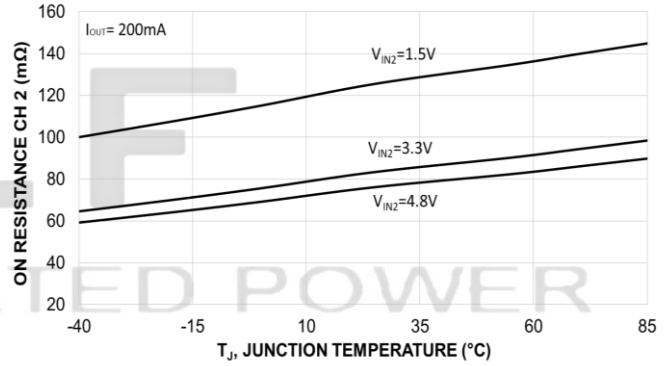


Figure 11. On-Resistance vs. Temperature, Channel 2

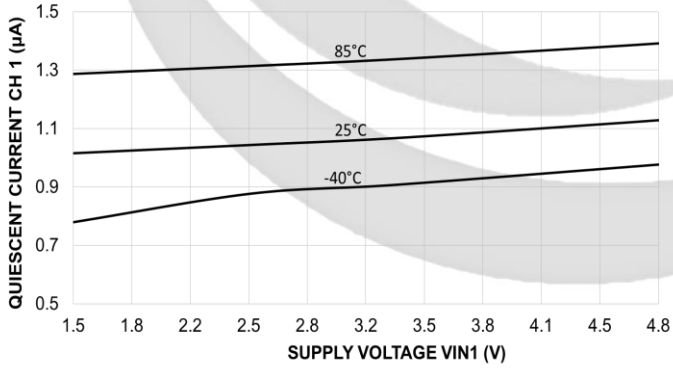


Figure 12. VIN1 Quiescent Current vs. Supply Voltage

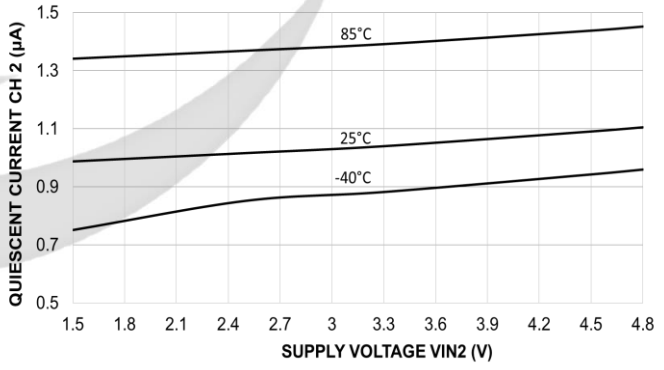


Figure 13. VIN2 Quiescent Current vs. Supply Voltage

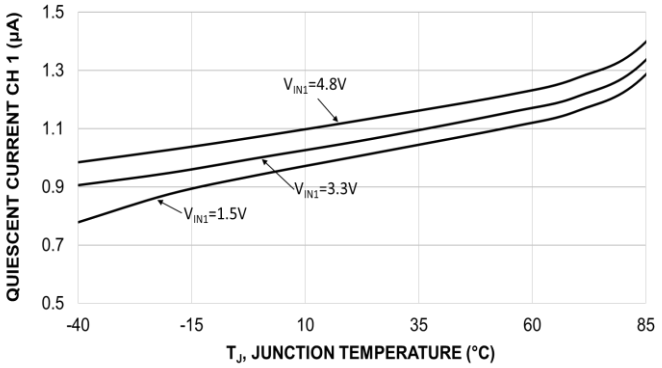


Figure 14. VIN1 Quiescent Current vs. Temperature

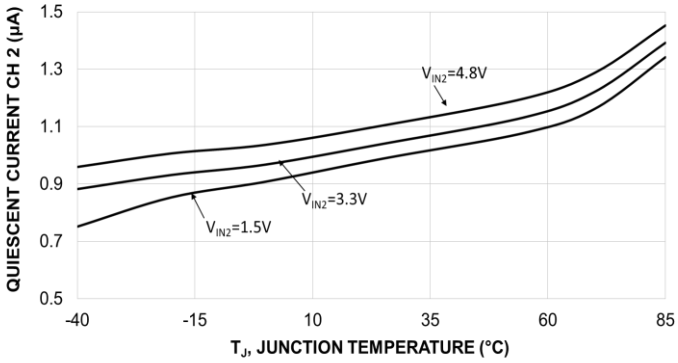


Figure 15. VIN2 Quiescent Current vs. Temperature

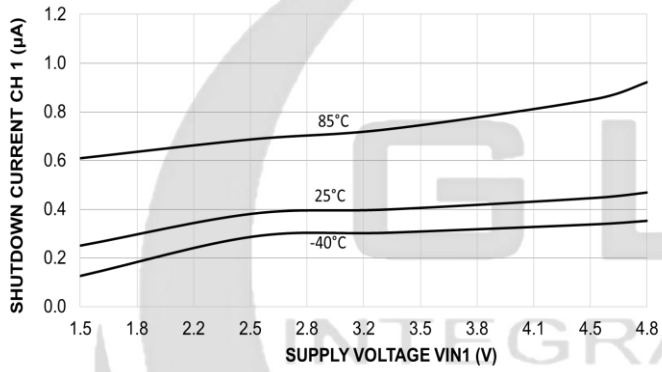


Figure 16. VIN1 Shutdown Current vs. Supply Voltage

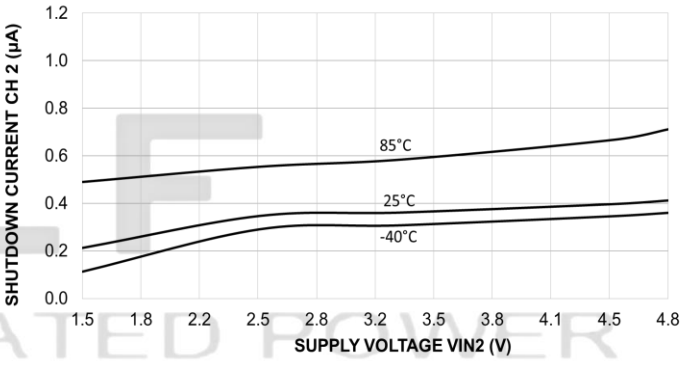


Figure 17. VIN2 Shutdown Current vs. Supply Voltage

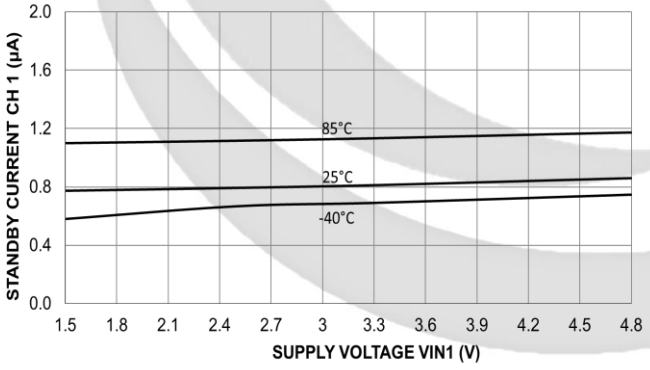


Figure 18. VIN1 Standby Current vs. Supply Voltage

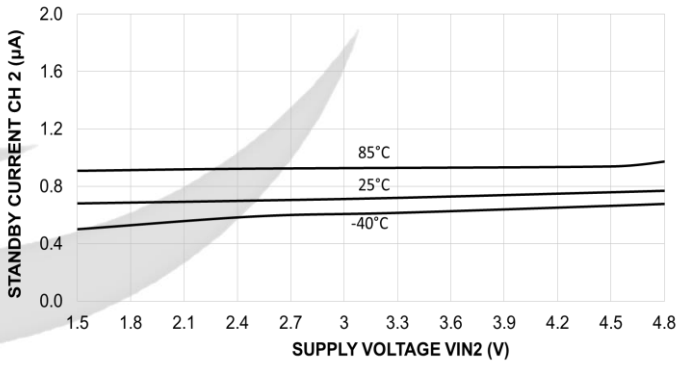


Figure 19. VIN2 Standby Current vs. Supply Voltage

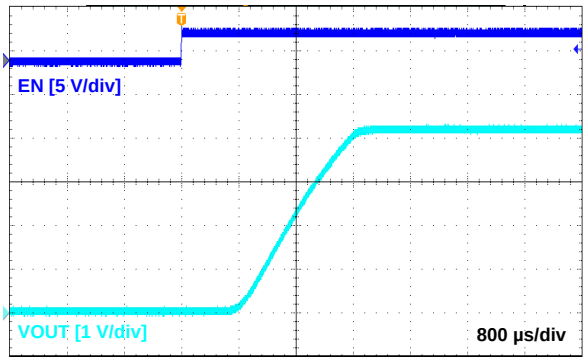


Figure 20. Turn-On Response, Channel 1
V_{IN1}=4.2 V, C_{IN}=C_{OUT} =10 µF, R_L=100 Ω, SEL=High

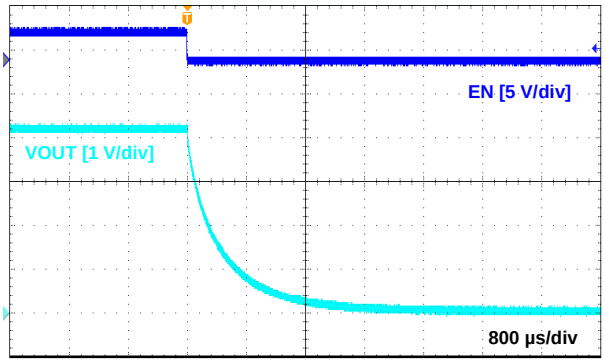


Figure 21. Turn-Off Response, Channel 1
V_{IN1}=4.2 V, C_{IN}=C_{OUT} =10 µF, R_L=100 Ω, SEL=High

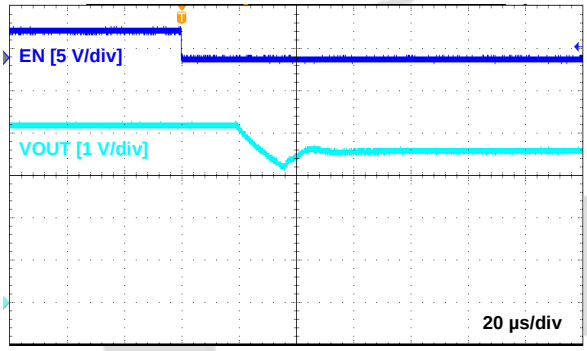


Figure 22. VOUT Switchover from 4.2 V to 3.6 V
V_{IN1}=4.2 V, V_{IN2}=3.6 V, C_{IN}=C_{OUT}=10 µF, R_L=10 Ω
SEL = VIN1, EN controlled by GPIO

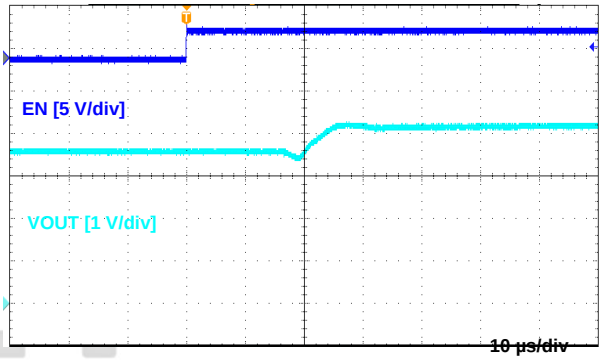


Figure 23. VOUT Switchover from 3.6 V to 4.2 V
V_{IN1}=4.2 V, V_{IN2}=3.6 V, C_{IN}=C_{OUT}=10 µF, R_L=10 Ω
SEL = VIN1, EN controlled by GPIO

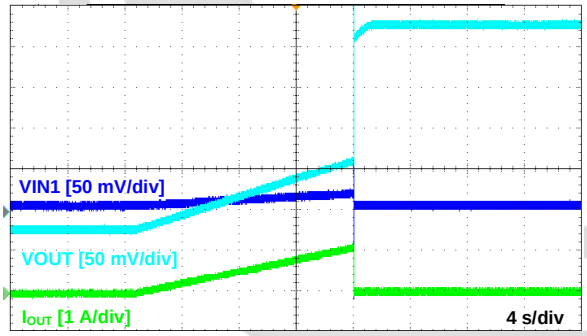


Figure 24. Reverse Current Blocking on Each VIN
V_{IN1}=3.3 V, V_{OUT}= 3 V to 3.4 V, C_{IN}=C_{OUT}=10 µF

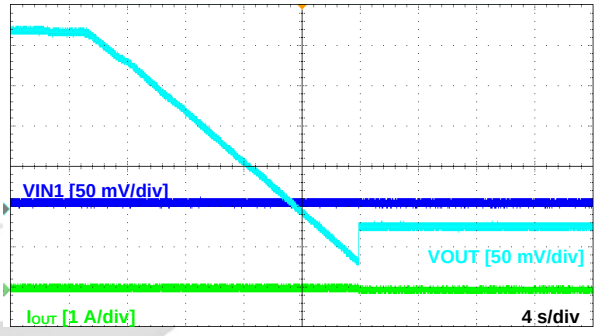


Figure 25. Reverse Current Blocking Release
V_{IN1}=3.3 V, V_{OUT}= 3.4 V to 3 V, C_{IN}=C_{OUT}=10 µF

APPLICATION INFORMATION

The GLF4003 is a fully integrated power mux IC with the input voltage range from 1.5 V to 4.8 V. It has asymmetrical two channels and a fixed slew rate control to limit the inrush current during turn on. It also has very low on-resistance to reduce conduction loss. In the off state, it consumes very low leakage current to avoid unwanted standby current and save input power supply.

Input Source Selection

According to the state of SEL and EN pins, the GLF4003 offers an automatic selection, a manual selection and VIN1 priority selection mode. In each mode, the VOUT connects to one input source. Do not leave both SEL and EN pins floating.

Mode	SEL	EN	VOUT
Manual	High	> V_{TH}	VIN1
	High	< V_{TH}	VIN2
	Low	> V_{TH}	High-Z
Auto	Low	< V_{TH}	Higher voltage between VIN1 and VIN2

Table 2. Manual and Automatic Selection Mode

For applications, where a General-Purpose Input/Output (GPIO) pin is used to select the input source (refer to Figure 3), the GPIO pin connects directly to the EN pin, and the SEL pin is set high. When the GPIO pin is high, VIN1 is selected as the input. Conversely, when the GPIO pin is low, VIN2 is selected.

For applications, If both EN & SEL are low (refer to Figure 4), the GLF4003 will choose a higher input voltage source to VOUT automatically.

In VIN1 priority selection mode (refer to Figure 5 and Table 3), the SEL pin is connected to VIN 1 node and the EN pin is connected to the midpoint of a voltage divider formed by two resistors. The VIN1 priority selection mode operates without GPIO control. The C1 is used to stabilize the EN pin state at around V_{TH}. 1 µF capacitor is recommended for the C1. When VIN1 is applied and the EN pin voltage is higher than the threshold voltage (V_{TH}), the VOUT is powered by VIN1. As the VIN1 voltage drops, if the voltage at the EN pin falls below V_{TH}, VOUT automatically switches over to the backup channel VIN2.

Mode	VIN1	VIN2	SEL	EN	VOUT
VIN1 Priority	≥ 1.5 V	X	Connect to VIN1	> V_{TH} by resistor divider from VIN1	VIN1
	≥ 1.5 V	≥ 1.5 V		< V_{TH} by resistor divider from VIN1	VIN2

Table 3. VIN1 Priority Selection

Design Example for Switching-Over Trigger Voltage Calculation:

Parameter	Value
VIN1	4.5 V
VIN2	1 cell Lithium Battery
Selection Mode	VIN1 Priority Selection

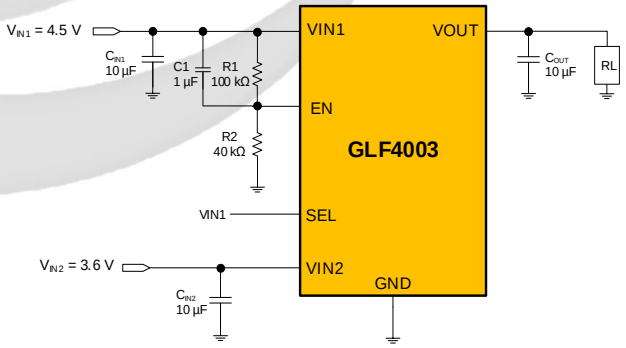


Figure 26. Design Example for V_{SW_TRG} Calculation

The value of the switching-over trigger voltage is determined by the following equation.

$V_{SW\_TRG} = V_{TH} \times (1 + R1 / R2)$

Where, V_{SW_TRG}: Switching-over trigger voltage when VIN1 is unplugged

V_{TH}: EN pin threshold voltage

For downstream systems requiring power supply switching with minimal output voltage drop, the GL4003 can reduces the voltage drop during transition from the primary input (VIN1) to the secondary input (VIN2) upon removal of VIN1. In this example, the switching trigger voltage is set to 3.5 V (when 4.5 V is removed) using resistors R1 (100 kΩ) and R2 (40 kΩ).

Output Voltage Drop at Switching Over

During the switching event, the output voltage drop is influenced by both the load resistance and the output capacitance. A lower load resistance at the switching point will result in a larger voltage drop. To mitigate this drop when a significant load current is needed during the transition, a sufficiently large bulk output capacitor is recommended.

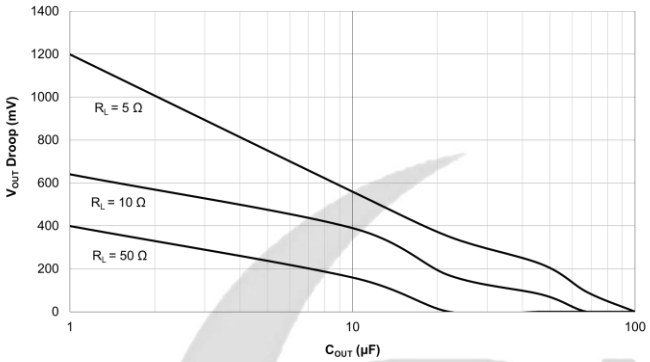


Figure 27. Output Voltage Droop at Switching Over from VIN1 (4.5 V) to VIN2 (3.3 V)

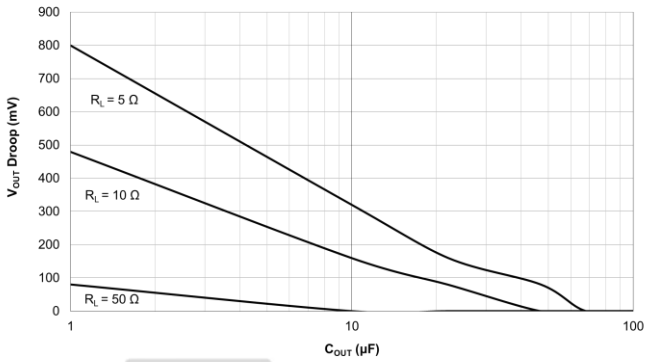


Figure 28. Output Voltage Droop at Switching Over from VIN2 (3.3 V) to VIN1 (4.5 V)

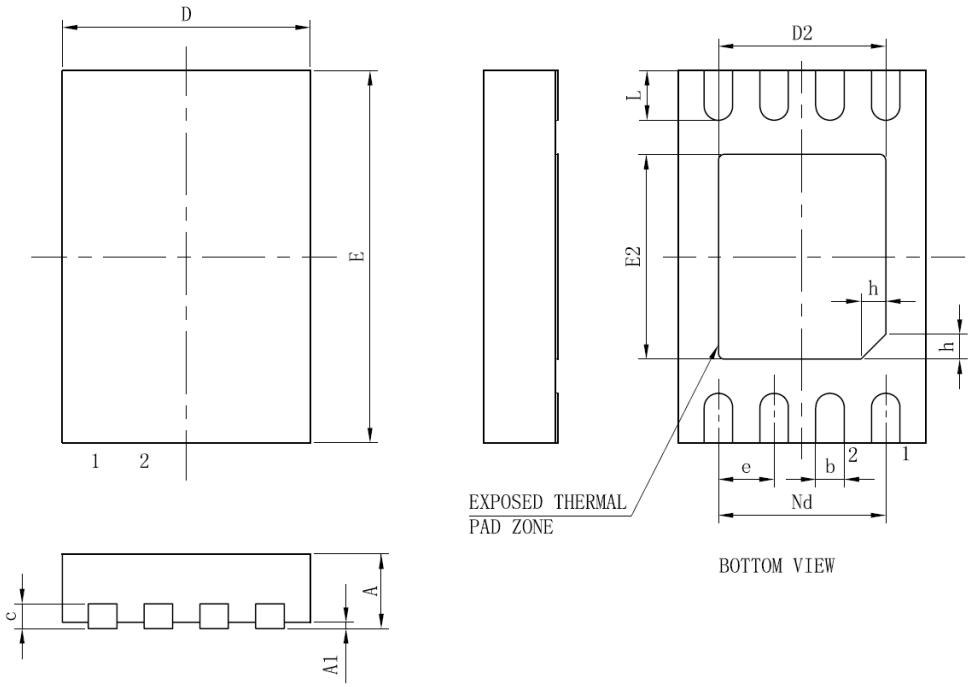
Reverse Current Blocking

The reverse current blocking protection will be enabled when either of the input voltage (VIN1 or VIN2) exceeds its minimum rating. The reverse current blocking protection triggers when the output voltage rises above an input voltage plus the reverse current blocking threshold (V_{RCB_TH}). The main FET immediately shuts off to prevent reverse current flow. It's important to note that some reverse current might exist before V_{RCB_TH} is reached. Normal operation resumes when the output voltage falls below the input minus the reverse current blocking release voltage (V_{RCB_RL}). An additional clamping component and a high output capacitance are recommended to safeguard against potential damage from high output voltage spikes.

Board Layout

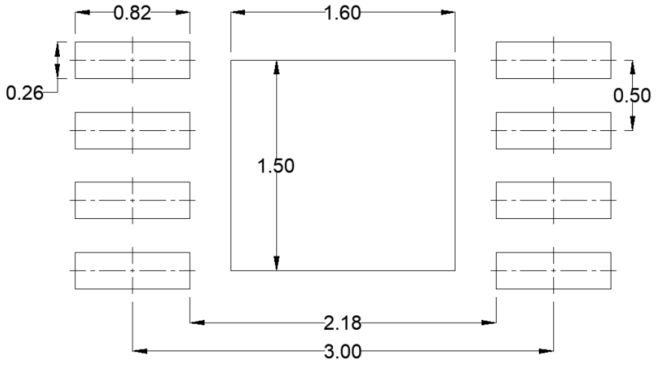
All the external components should be placed to GLF4003 as close as possible. All traces should be as short as possible to minimize parasitic inductance. Wide traces of VIN, VOUT and GND can reduce parasitic effects under dynamic operations to improve thermal performance at high current loading.

PACKAGE OUTLINE



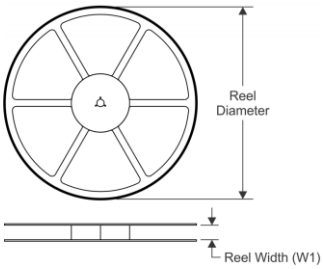
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.30	0.40	0.50
h	0.20	0.25	0.30

Recommended Footprint

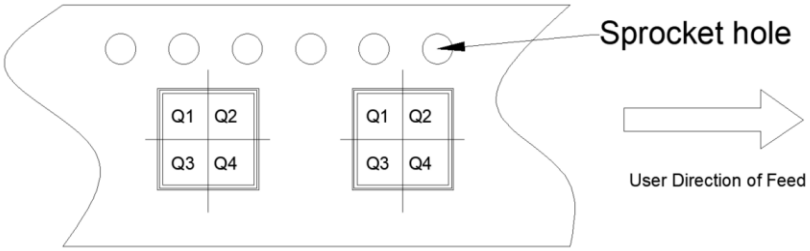


TAPE AND REEL INFORMATION

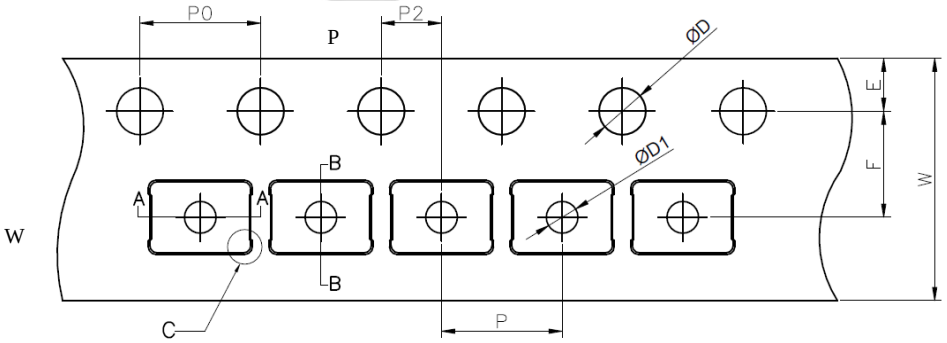
REEL DIMENSIONS

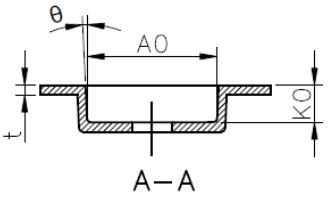


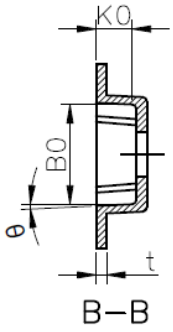
QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS







Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF4003-D3G7	DFN 2x3-8L	8	3000	180	9	3.25	2.25	0.95	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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