GLF74130

Ultra-low Power, 4.5A Power Mux Switch with Auto & Manual Input Selection

Product Specification

DESCRIPTION

The GLF74130 I_QSmart™ is an advanced technology fully integrated power path load switch with the ability to automatically select between two input sources depending on the input voltage level of each source. The power path switch is targeted for the data storage and mobile markets and is therefore available as a chip scale package utilizing 12 bumps in a 1.27 mm x 1.67 mm x 0.55 mm die size to deliver the highest performance lowest cost power path switch solution in the industry.

The GLF74130 has a built-in reverse current blocking protection. When both switches are at the off mode, the GLF74130 prevents the reverse current from a higher output voltage to the input side.

The EN pin can be used along with the SEL pin to control the switches of the GLF74130. By the combination of these two pins, one of input source selection modes is set among the automatic, VIN1, or VIN2 selection.

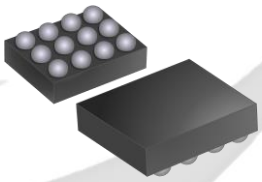
APPLICATIONS

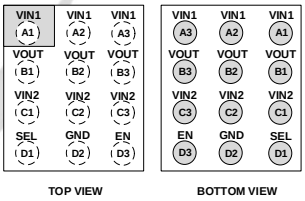
- Smart Devices
- Subsystem with Backup Power
- IoT Tracking System
- Communication / Network System

FEATURES

- Two-Input and Single-Output Power Multiplexer Switch
- Automatic and Manual Input Selection Modes
- Supply Voltage Range: 1.5 V to 5.5 V
- R_{ON} = 20 mΩ Typ at 5.5 V_{IN1} or V_{IN2}
- 4.5 A Continuous Output Current Capability Per Channel
- Ultra-Low Supply Current at Operation
  I_Q: 4 uA Typ at 5.5 V_{IN}
- Ultra-Low Stand-by Current
  I_{SD}: 50 nA Typ at 5.5 V_{IN}
- Reverse Current Blocking when Disabled
- Smart Control Pins
  I_{EN} and I_{SEL} : 10 nA Typ at V_{EN} or V_{SEL} > V_{IH}
  R_{EN} and R_{SEL} : 500 kΩ Typ
- Ambient Operating Temperature Range: -40 °C to 85 °C
- HBM: 6 kV, CDM: 2 kV

PACKAGE



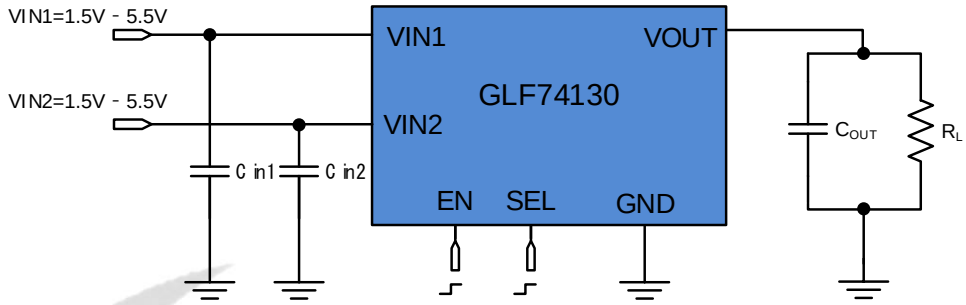


1.27 mm x 1.67 mm x 0.55 mm, 0.4 mm pitch

DEVICE ORDERING INFORMATION

Part Number	Top Mark	R_{ON} at 5.5 V_{IN}	Output Current, I_{OUT}	Ultra-low I_Q at 5.5 V_{IN}
GLF74130	BH	20 mΩ	4.5 A	4 uA

APPLICATION DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

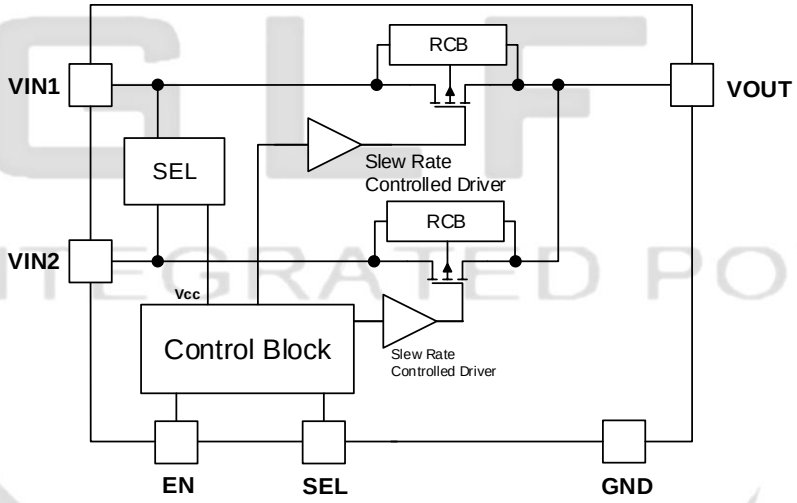
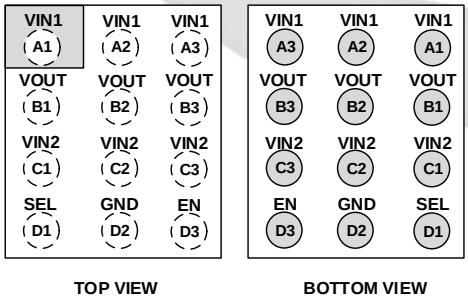


Figure 1. Functional Block Diagram

PIN CONFIGURATION



TOP VIEW BOTTOM VIEW

Figure 2. 1.27mm x 1.67mm x 0.55mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1, A2, A3	VIN1	Switch Input 1 Supply Voltage
B1, B2, B3	VOUT	Switch Output
C1, C2, C3	VIN2	Switch Input 2 Supply Voltage
D1	SEL	Input Source Selection. Do not leave the SEL pin floating.
D2	GND	Ground
D3	EN	Enable to control the switch. Do not leave the EN pin floating.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VIN1, VIN2 VOUT, EN	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Continuous Current			4.5	A
	Pulse, 100 us pulse and 2 % duty cycle			6.5	A
P_D	Power Dissipation at T_A = 25 °C			1.2	W
T_J	Maximum Junction Temperature			150	°C
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Ambient Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIN1, VIN2	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature Range	-40	+85	°C

ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = 1.5 V to 5.5 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Basic Operation							
I_{Q1}, I_{Q2}	Quiescent Current	V_{IN1} = 5.5 V, V_{IN2} < V_{in1}, I_{OUT} = 0 mA, EN = 0 V, SEL = V_{IN1}, V_{OUT} = V_{IN1} or V_{IN2} = 5.5 V, V_{IN1} < V_{IN2}, I_{OUT} = 0 mA, EN = SEL = V_{IN2}, V_{OUT} = V_{IN2}			4	6	µA
		As above, Ta = 85 °C (1)			4.7		
I_{SD1}, I_{SD2}	Shutdown Current	$V_{IN1,2}$ = 5.5 V, V_{OUT} = GND, EN = SEL = 0 V			50	200	nA
		$V_{IN1,2}$ = 5.5 V, V_{OUT} = GND, EN = SEL = 0 V, Ta=85 °C (1)			500		
R_{ON}	On-Resistance	V_{IN1} or V_{IN2} = 5.5 V I_{OUT} = 500 mA	Ta = 25 °C		20	25	mΩ
			Ta = 85 °C (1)		24		
		V_{IN1} or V_{IN2} = 4.5 V, I_{OUT} = 500 mA	Ta = 25 °C		23		
			Ta = 85 °C (1)		26		
		V_{IN1} or V_{IN2} = 3.3 V, I_{OUT} = 500 mA	Ta = 25 °C		27	32	
			Ta = 85 °C (1)		32		
		V_{IN1} or V_{IN2} = 2.5 V, I_{OUT} = 300 mA	Ta = 25 °C		34		
		V_{IN1} or V_{IN2} = 1.5 V, I_{OUT} = 300 mA	Ta = 25 °C		60		
V_{IH}	EN and SEL Input Logic High Voltage	V_{IN1} or V_{IN2} = 1.5 V - 5.5 V		1.2			V
V_{IL}	EN and SEL Input Logic Low Voltage	V_{IN1} or V_{IN2} = 1.5 V - 5.5 V				0.4	V
I_{EN}, I_{SEL}	EN, SEL Current	EN or SEL Voltage > V_{IH}, Enabled			10		nA
R_{EN}, R_{SEL}	EN and SEL pull down resistance	EN or SEL Voltage < V_{IH}, Disabled			500		kΩ
I_{RVS}	Reverse Current (1)	V_{IN1} = V_{IN2} = 0 V, V_{OUT} = 5.5 V, EN = SEL = 0 V			70		nA
Switching Characteristics (2)							
t_{dON}	Turn-On Delay	V_{IN1} = 5.0 V, V_{IN2} = 3.3 V, R_L = 150 Ω, C_{OUT} = 10 µF			580		µs
t_R	VOUT Rise Time				790		µs
TdHL	High-low Delay (1)				9		µs
TfHL	High-low Fall Time (1)				12		µs
Vdroop	Voltage Droop (1)				40		mV
TdLH	Low-high Delay (1)				10		µs
TrLH	Low-high Rise Time (1)				9		µs
td_{OFF}	Turn-Off Delay (1)				90		µs
t_F	VOUT Fall Time (1)				3.5		ms

Notes:
1. By design; characterized, not production tested.
2. t_{ON} = t_{dON} + t_R , t_{OFF} = t_{dOFF} + t_F

TIMING DIAGRAM AND TRUTH TABLE

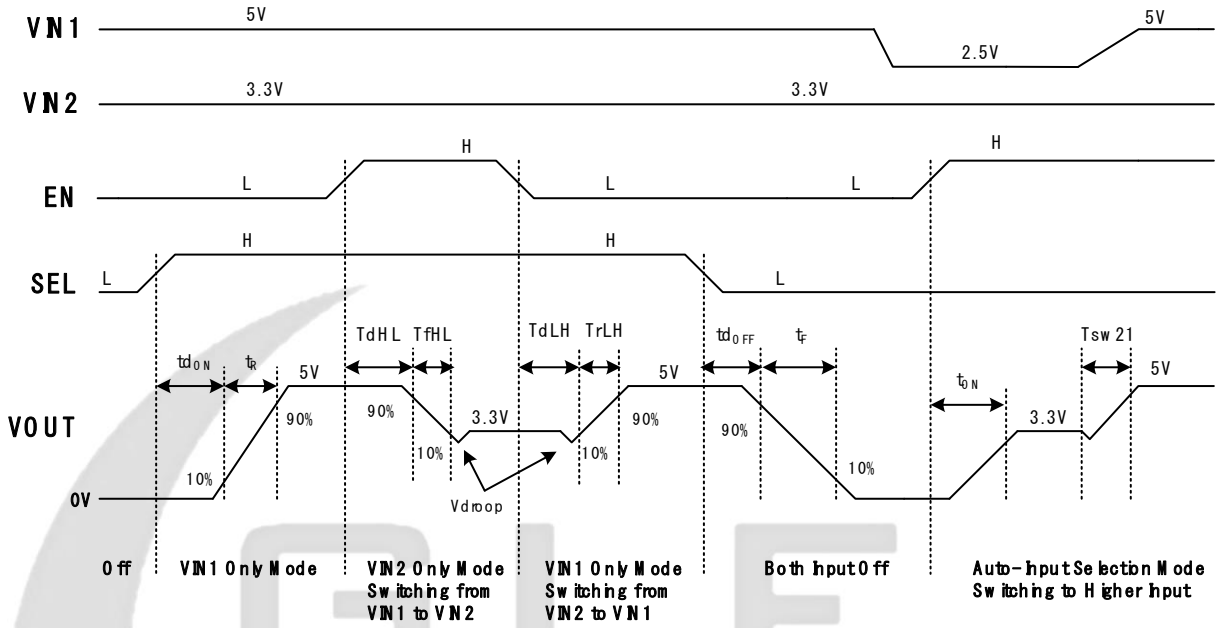


Figure 3. Timing Diagram

SEL	EN	Function	VOUT
0	0	Both switches are off.	High-Z
0	1	Auto-Input selection. Vout is connected to a higher input source automatically.	Higher Input between VIN1 and VIN2
1	0	Only VIN1 is selected.	VIN1
1	1	Only VIN2 is selected.	VIN2

Table 1. Truth Table of Input Source Selection

TYPICAL PERFORMANCE CHARACTERISTICS

Both VIN1 and VIN2 switches are identical.

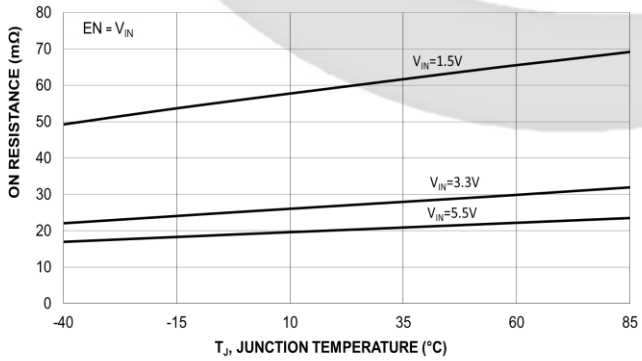


Figure 4. On-Resistance vs. Temperature

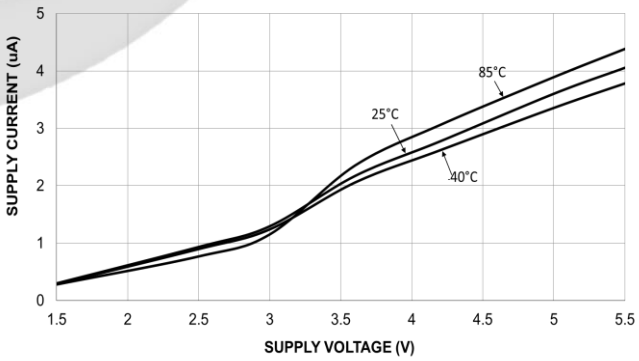


Figure 5. Quiescent Current vs. Supply Voltage

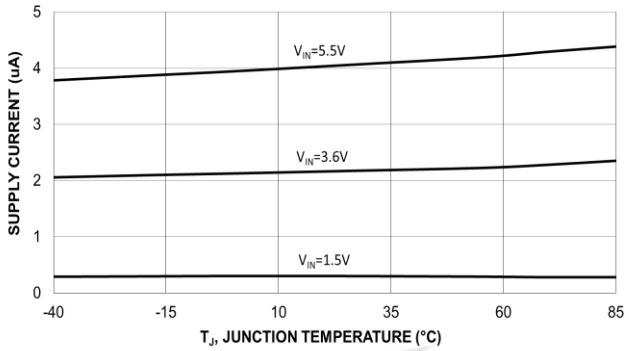


Figure 6. Quiescent Current vs. Temperature

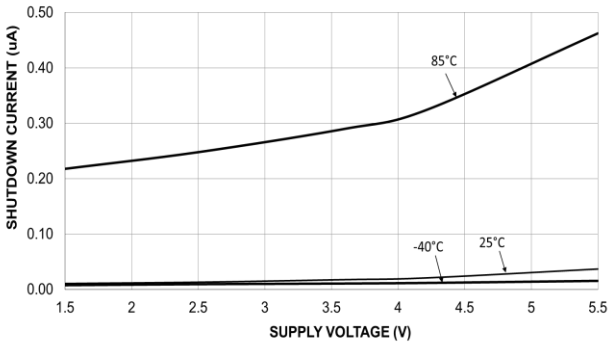


Figure 7. Shutdown Current vs. Supply Voltage

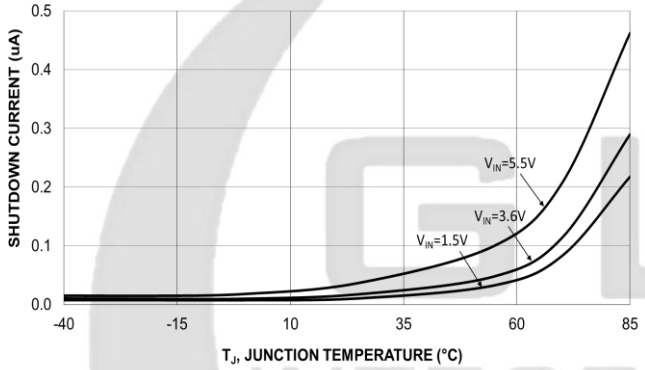


Figure 8. Shutdown Current vs. Temperature

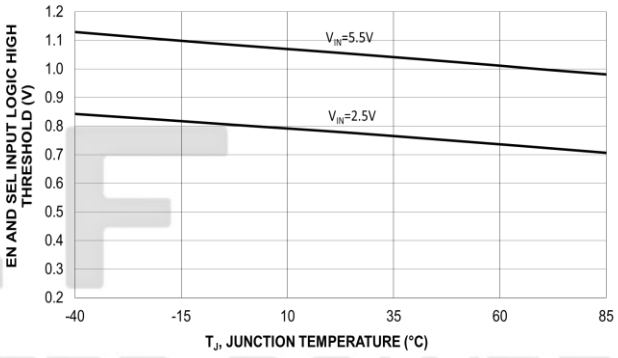


Figure 9. EN and SEL Input Logic High Threshold Vs. Temperature

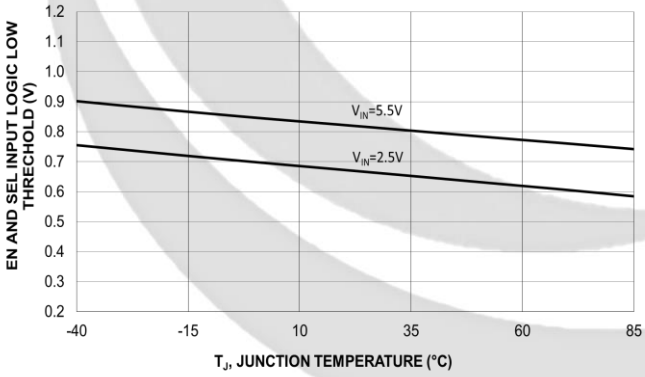


Figure 10. EN and SEL Input Logic Low Threshold Vs. Temperature

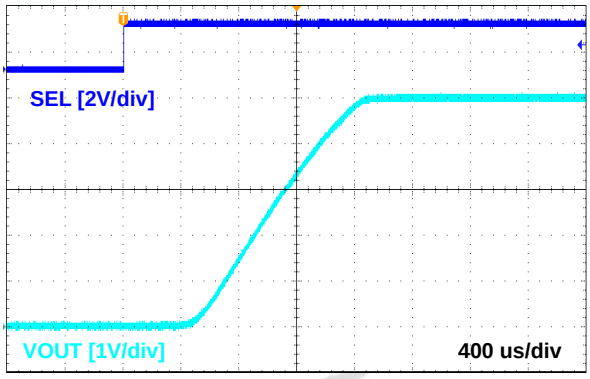


Figure 11. Turn-On Response
V_{IN1}=5.0 V, C_{IN}=10 uF, C_{OUT}=10 uF, R_L=150 Ω

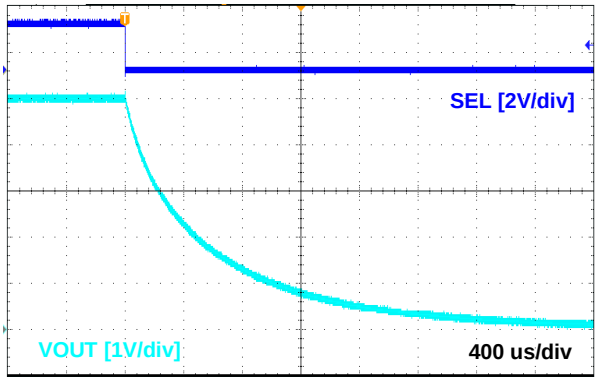


Figure 12. Turn-Off Response
V_{IN1}=5.0 V, C_{IN}=10 uF, C_{OUT}=10 uF, R_L=150 Ω

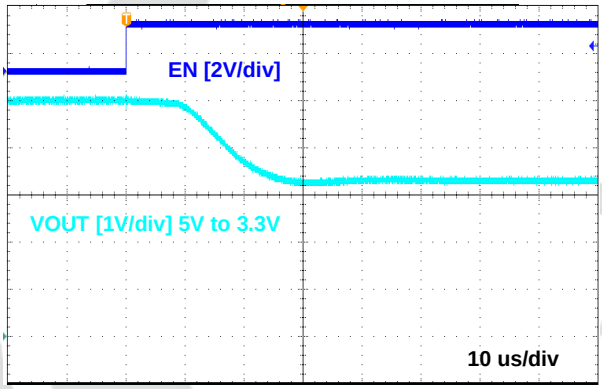


Figure 13. V_{OUT} Switchover from 5 V to 3.3 V
V_{IN1}=5.0 V, V_{IN2}=3.3 V C_{IN}=10 uF, C_{OUT}=10 uF, R_L=150 Ω

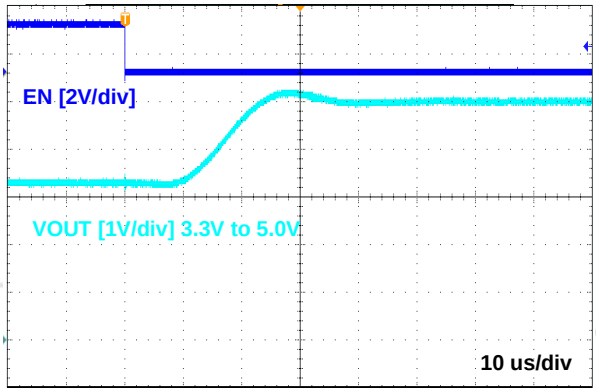


Figure 14. V_{OUT} Switchover 3.3 V to 5 V
V_{IN1}=5.0 V, V_{IN2}=3.3 V C_{IN}=10 uF, C_{OUT}=10 uF, R_L=150 Ω

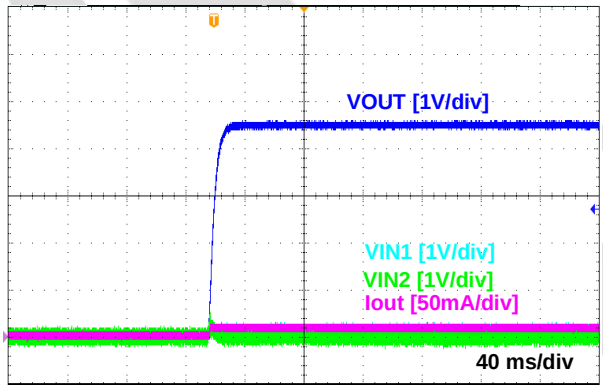


Figure 15. Reverse Current Blocking When Disabled
V_{IN1}=V_{IN2}=0 V, V_{OUT}=0 V to 4.5 V C_{IN}=10 uF, C_{OUT}=10 uF, EN=SEL=0 V

APPLICATION INFORMATION

The GLF74130 is a fully integrated 4.5 A power mux with a fixed slew rate control to limit the inrush current during turn on in the input voltage range from 1.5 V to 5.5 V. Each device has very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power supply. The package is 1.27 mm x 1.67 mm x 0.55 mm wafer level chip scale package saving space in compact applications and it has 12 bumps, 0.4 mm pitch for manufacturing availability.

Smart EN and SEL Control Pin

With a control voltage less than the V_{IH} for EN or SEL pin, the internal pull-down resistance (R_{EN} or R_{SEL} = 500 kΩ Typ.) is used to keep control pins from floating and ensure a reliable off state. When a voltage higher than the V_{IH} is applied to EN and SEL pin, the 500 kΩ pull-down resistor will be completely disconnected save unnecessary power consumption and enable the pin function.

Input Source Selection

According to the state of SEL and EN pins, the GLF74130 offers the automatic as well as the manual selection mode. In each mode, the VOUT connects to one input source. Do not leave both SEL and EN pins floating.

SEL	EN	Function	VOUT
0	0	Both switches are off.	High-Z
0	1	Auto-Input selection. Vout is connected to a higher input source automatically.	Higher Input between VIN1 and VIN2
1	0	Only VIN1 is selected.	VIN1
1	1	Only VIN2 is selected.	VIN2

Notes: The internal Vcc should be connected to the higher between VIN1 and VIN2.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin the moment when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

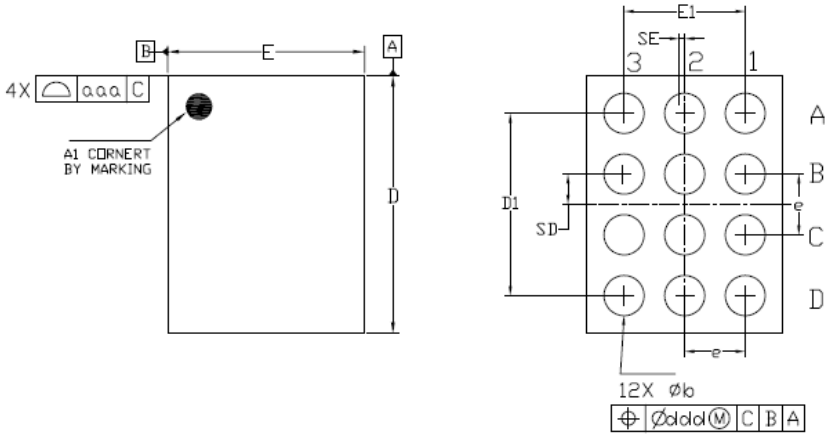
Reverse Current Blocking

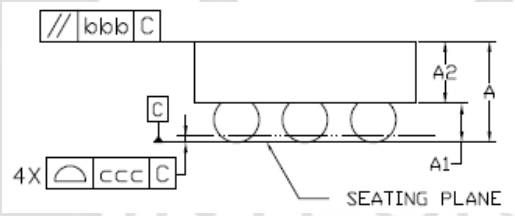
The GLF74130 also prevents the reverse current from the output voltage when both switches are turned off at EN = SEL = 0 V.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.

PACKAGE OUTLINE





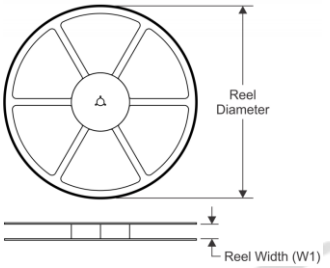
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.175	0.200	0.225
A2	0.325	0.350	0.375
D	1.655	1.670	1.685
E	1.255	1.270	1.285
D1	1.150	1.200	1.250
E1	0.750	0.800	0.850
b	0.215	0.265	0.315
e	0.400 BSC		
SD	0.200 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

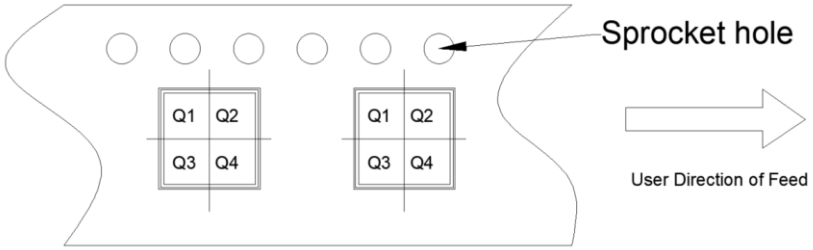
1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

TAPE AND REEL INFORMATION

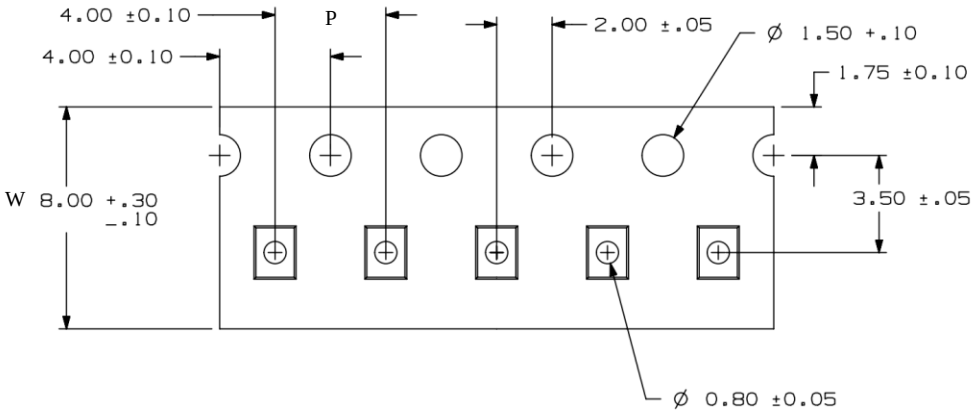
REEL DIMENSIONS

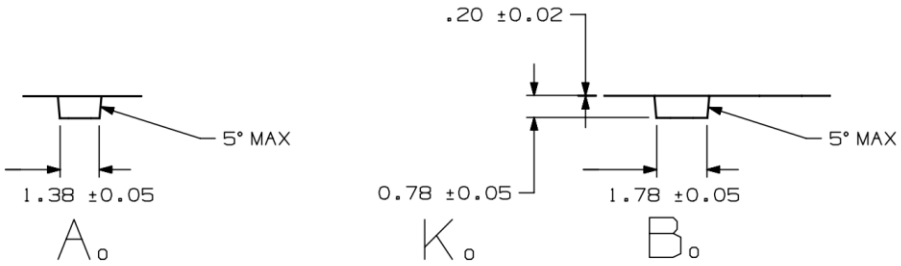


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF74130	WLCSP	12	3000	180	9	1.38	1.78	0.78	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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