GLF78231, GLF78231T

3-Channel I_QSmart™ Load Switch with Sequence Control

Product Brief

DESCRIPTION

The GLF78231 / GLF78231T is a 3-channel integrated switch with a programmable sequence control function. Each switch is an 1A rated rating per a channel, which has an integrated slew rate control. Its best in class efficiency makes it an ideal choice for use in IOT, mobile, and wearable electronics.

The GLF78231 / GLF78231T has an integrated sequence timing function with adjustable ON and OFF delay times for 3 different power input sources with one enable pin control.

The GLF78231 / GLF78231T features ultra-efficient I_QSmart™ technology that supports some of the lowest quiescent currents (I_Q) and shutdown currents (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage currents, improve system efficiency, and increase battery lifetimes.

The GLF78231 / GLF78231T integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the slew rate control specifically limits inrush currents during turn-on, helping to minimize voltage droop.

The GLF78231 / GLF78231T supports an industry leading wide input voltage range, helping to improve operating life and system robustness. Furthermore, one device can be used in 3 different voltage rails applications, helping simplify inventory management and reduce purchasing, and operating costs.

The GLF78231 / GLF78231T is in the 1.27mm x 1.67mm x 0.55mm WLCSP (Wafer Level Chip Scale Package) with 12 bumps and 0.4mm pitch.

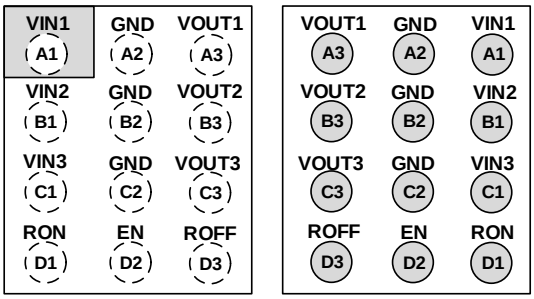
FEATURES

- 3 Switches with Integrated Sequence Control
- Programmable ON and OFF Delay Times
- Ultra-Low I_Q:
  1nA Typ @ 3.3V Input Per Channel
- Ultra-Low I_{SD}:
  5nA Typ @ 3.3V Input Per Channel
- Low R_{ON} = 65 mΩ Typ. @ 3.3V_{IN1}
  90 mΩ Typ. @ 1.8V_{IN2}
  120 mΩ Typ. @ 1.2V_{IN3}
- I_{OUT} Max = 1.0A Per Channel
- Controlled Rise Time: 400us at 3.3V_{IN}
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch On Each Channel
- Ultra-Small WL-CSP Package

APPLICATIONS

- Wearables
- Mobile Devices
- Low Power Subsystems

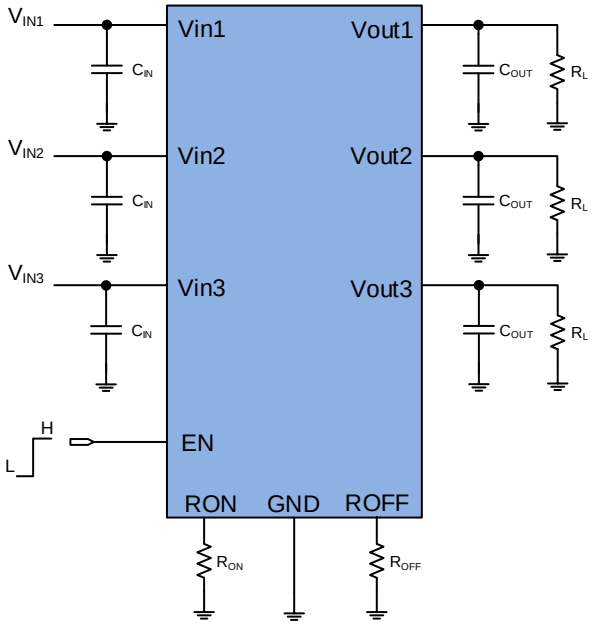
PACKAGE



TOP VIEW BOTTOM VIEW

GLF78231 : 1.27mm x 1.67mm x 0.55mm
GLF78231T : 1.27mm x 1.67mm x 0.35mm

APPLICATION DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

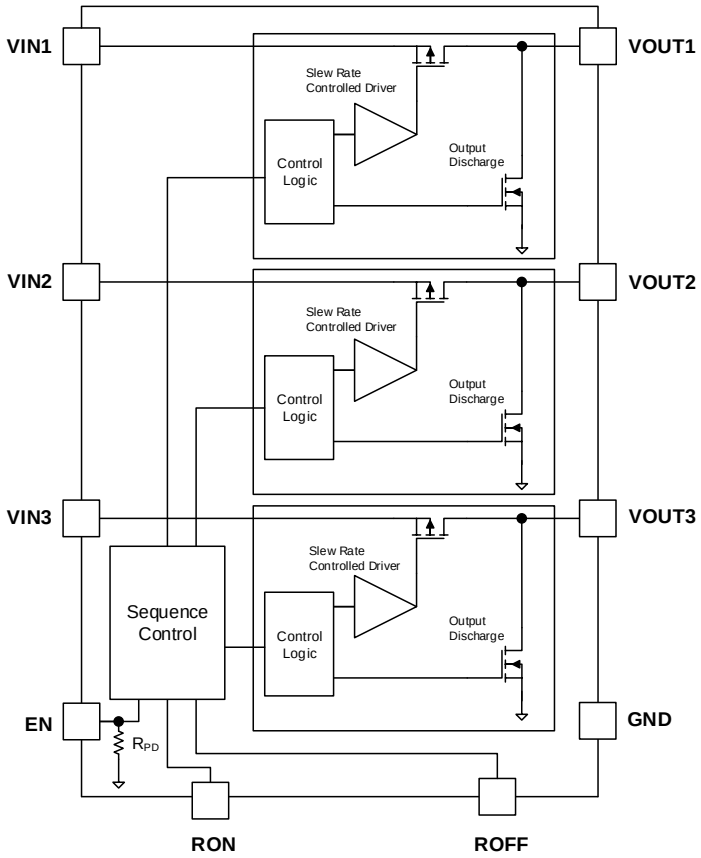


Figure 1. Functional Block Diagram

PIN CONFIGURATION

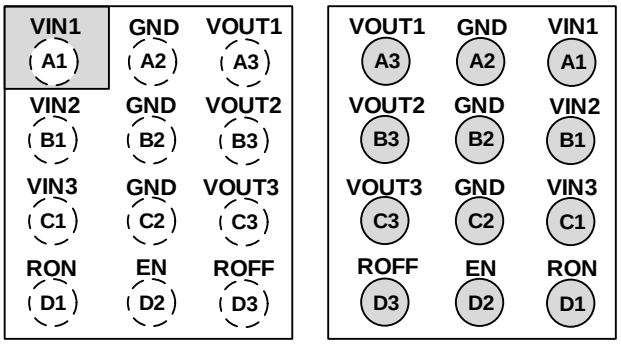


Figure 2. 1.27mm x 1.67mm x 0.5mm WLCSP
1.27mm x 1.67mm x 0.35mm Ultra-Thin WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	VOUT1	Switch Input
A2	GND	Ground
A3	VIN1	Switch Output
B1	VOUT2	Switch Input
B2	GND	Ground
B3	VIN2	Switch Output
C1	VOUT3	Switch Input
C2	GND	Ground
C3	VIN3	Switch Output
D1	RON	An external resistor is connected to set the on time of VOUT2 and VOUT3 after VOUT1 rises. See the Ts1 in the timing diagram.
D2	EN	Enable to control the switch. There is an internal pull-down resistor.
D3	ROFF	An external resistor is connected to set the off time of VOUT1 and VOUT2 after VOUT3 falls. See the Ts2 in the timing diagram.

TIMING DIAGRAM

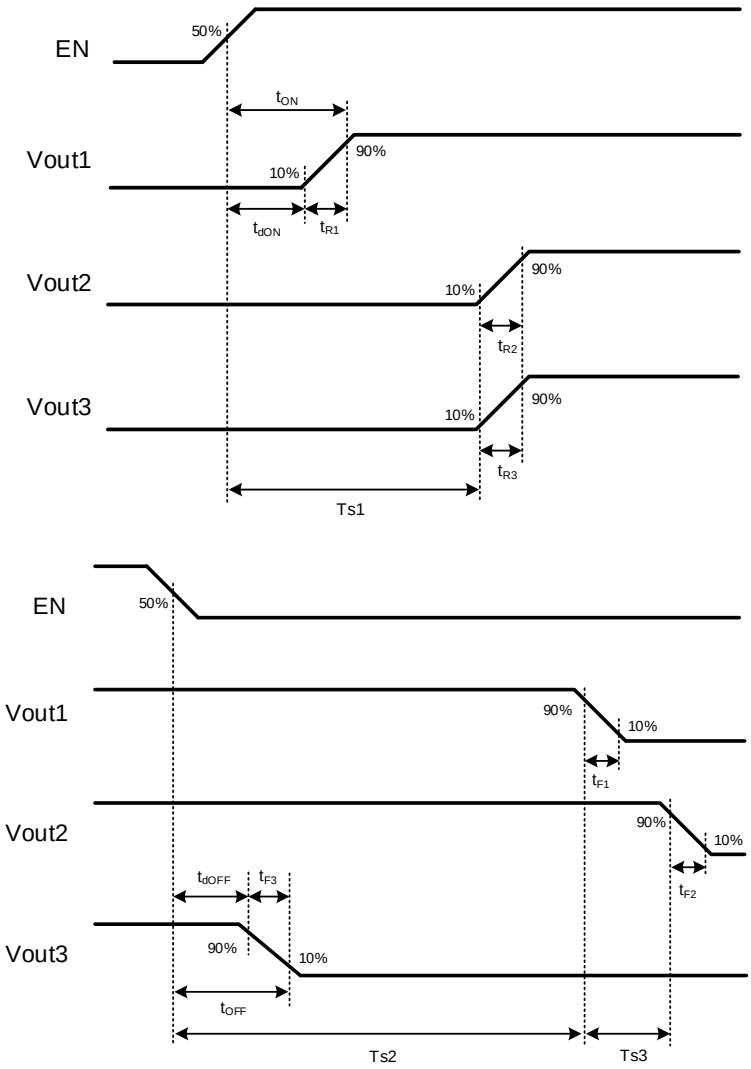


Figure 2. Timing Diagram

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Switching Characteristics						
T_{S1}	On Timing	On timing sequence for V_{OUT1} and V_{OUT3}, R_{ON} = 45kΩ		1		ms
T_{S2}	Off Timing	Off timing sequence for V_{OUT1}, R_{OFF} = 60kΩ,		10		
T_{S3}	Off Timing	Off timing sequence between V_{OUT1} and V_{OUT2}		0.5		
t_{dON}	Turn-On Delay(1)	V_{OUT1}, RL=150Ω, C_{OUT}=0.1µF		275		us
t_{R1}	Rise Time(1)			400		
t_{R2}	Rise Time(1)	V_{OUT2}, RL=150Ω, C_{OUT}=0.1µF		400		
t_{R3}	Rise Time(1)	V_{OUT3}, RL=150Ω, C_{OUT}=0.1µF		700		
t_{dOFF3}	Turn-Off Delay(2,3,4)			TBD		
t_{F3}	V_{OUT} Fall Time(2,3,4)			TBD		

Notes: 1. Output discharge path is enabled during off.
2. By design; characterized; not production tested.
3. T_{S3} is proportional to T_{S2}.