GLF76311
Nano Current Consumption Power On/Off Switch

DESCRIPTION

The EV011-GLF76311 evaluation board features the GLF76311 that is an ultra-thin, ultra-efficient I_QSmart™ load switch with an integrated ON/OFF delay timer for Smart bracelet and Mobile handheld device.

When the VBAT pin is connected to the battery, the main switch of GLF76311 is turned on, that is the default state. When the internal integrated P-MOSFET is turned on, by pulling the SW pin to a low level for 6 s, the internal integrated P-MOSFET will be turned off, and the entire system enters the ultra-deep sleep energy-saving mode. The typical I_{SD} of GLF76311 is 7 nA. When the internal integrated P-MOSFET is turned off, by pulling the SW pin to a low level for 3 s, the internal integrated P-MOSFET will be turned on, and the entire system enters the normal working mode. The I_Q of GLF76311 is 6 nA.

The GLF76311 integrated 1ms slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events.

FEATURES

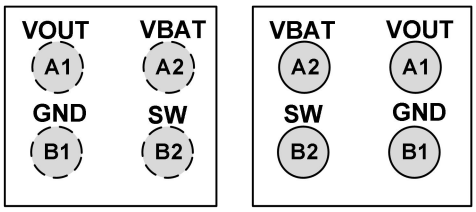
- Ultra-Low I_{SD}: 7 nA Typ at 3.6 V_{BAT}
- Ultra-Low I_Q: 6 nA Typ at 3.6 V_{BAT}
- Low R_{ON} : 34 mΩ Typ at 3.6 V_{BAT}
- I_{OUT} Max : 2 A
- Wide Input Range: 2.5 V to 5.5 V
- Turn-On Delay Time, 3 s Typ
- Turn-Off Delay Time, 6 s Typ
- Controlled Output Rise Time: 1 ms at 3.6 V_{BAT}
- Integrated Output Discharge Switch When Disabled
- Operating Temperature Range: -40 to 85 °C
- HBM: 6 kV, CDM: 2 kV
- Ultra-Small: 0.97 mm x 0.97 mm x 0.55 mm WLCSP

PRODUCT TABLE

Eval Board Ordering Info	Part Number	Top Mark	Turn On Delay Time	Turn Off Delay Time	Output Discharge	Package
EV011-GLF76311	GLF76311	CT	3 s	6 s	Yes	0.97 mm x 0.97 mm x 0.55 mm WLCSP

EVALUATION BOARD, DEVICE PACKAGE, AND PINOUT

PIN CONFIGURATION AND DEFINITION



TOP VIEW **BOTTOM VIEW**

0.97 mm x 0.97 mm x 0.55 mm WLCSP

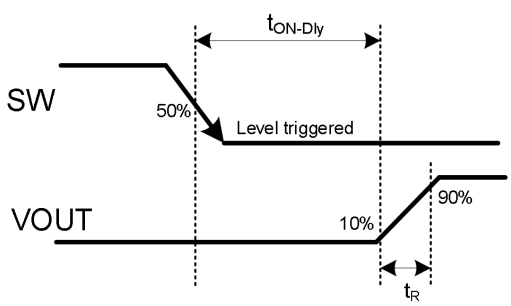
Pin #	Name	Description
A1	VOUT	Switch Output.
A2	VBAT	Switch Input. VBAT pin is connected to the positive input of an external battery.
B1	GND	Ground
B2	SW	Load switch SW control pin. Pulling the SW pin to a low level for 6 second, the internal integrated P-MOSFET will be turned off. Pulling the SW pin to a low level for 3 s, the internal integrated P-MOSFET will be turned on.

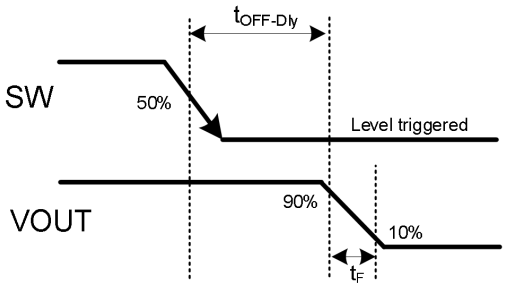
QUICK START GUIDE

The evaluation board EV011-GLF76311 is easy to set up to evaluate the performance of GLF76311.

1. Connect the positive and negative terminals of the input power supply or a Li-battery pack to VBAT pin and GND respectively. The VBAT_Sense and Vout_Sense can be used for measurement points. Make sure there is no high peak voltage generated when a VBAT input source is hot-plugged in.
2. When the VBAT pin is connected to the battery, the main switch of GLF76311 is turned on, that is the default state. The load resistor, RL=499 Ω, has been populated on the PCB board. Short the J3 to use the RL. To increase the output current, connect an electronic load to VOUT pin and GND.
3. Pulling the SW pin (J2) to a low level for 6 s, GLF76311 will be turned off, and the entire system enters the ultra-deep sleep energy-saving mode, the I_{SD} is about 7 nA.
4. Then pulling the SW pin (J2) to a low level for 3 s, GLF76311 will be turned on, and the entire system enters the normal working mode. The IQ of GLF76311 is about 6 nA.

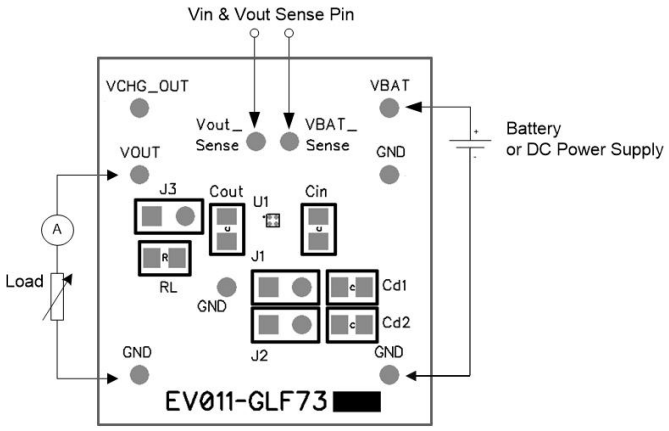
TIMING DIAGRAMS AND INPUT CONDITION



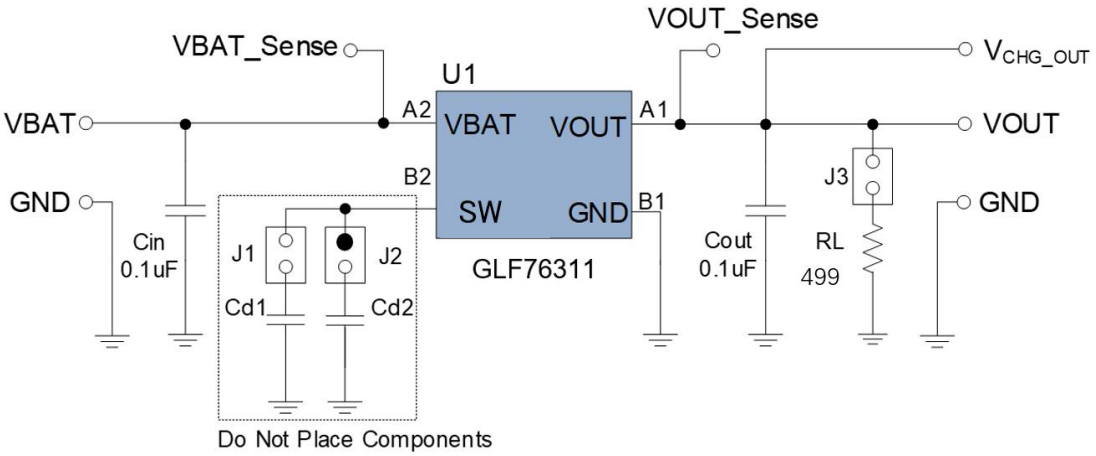


Function	VBAT	SW	Delay Time	VOUT Action
Power-On	First Connect battery	Doesn't matter	NA	VOUT=VBAT
	Connect battery	High to Low & Hold for 3 s	t_{ON-Dly} = 3 s	VOUT=VBAT
Power-Off into Deep Sleep	Connect battery	High to Low & Hold for 6 s	$t_{OFF-Dly}$= 6 s	VOUT to GND

TEST SETUP



SCHEMATIC



BILL OF MATERIALS

Qty	Reference	Value	Part Description	Manufacturer/Part Number
1	U1	GLF76311	GLF76311	GLF Integrated Power
1	Cin	0.1 μF	Cap., X7R, 16 V, 5 % 0805	Kemet # C0805C104J4RACTU
1	Cout	0.1 μF	Cap., X7R, 16 V, 5 % 0805	Kemet # C0805C104J4RACTU
1	RL	499 Ω	Load Resistor	YAGEO RC0805FR-07499RL
1	J3	Jumper	Jumper	-
1	J2	Test point	Test point	-
1	J1	Jumper	Jumper	DNP (Do Not Place)
2	Cd1, Cd2	-	-	DNP (Do Not Place)

PRINTED CIRCUIT BOARD LAYOUT

Fig 1. Top Layer

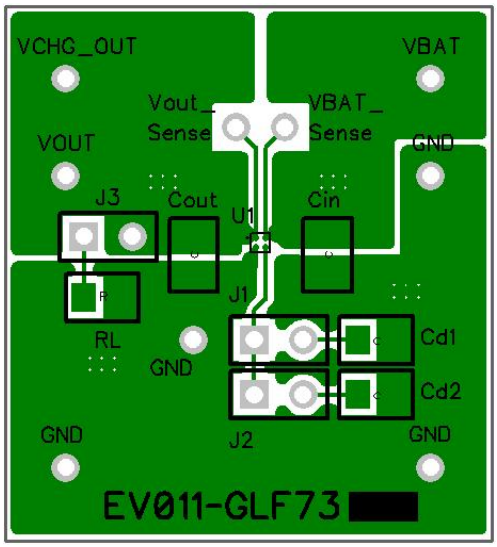
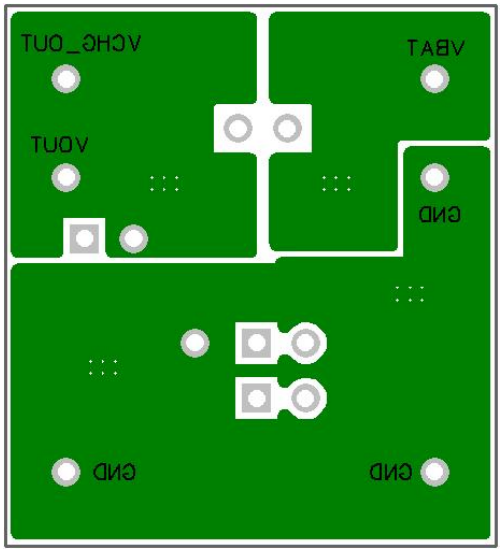


Fig 2. Bottom Layer



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