GLF76431

6A Integrated Power Load Switch with Configurable Power Reset Timer

Product Specification

DESCRIPTION

The GLF76431 is a 6 A load switch with a configurable reset timer for portable devices. The /SRO pin offers a true reset function enabling the load switch to completely disconnect the load from the input battery after a reasonable long delay time. After the reset period, the main switch of the GLF76431 reconnects the output load to the input battery for normal operation. The programmable delay time to the power reset mode by an external resistor on the REXT pin provides designers with system design flexibility.

The OFF input pin allows the GLF76431 to achieve complete shutdown with total downstream standby current of 360 nA typical. With the switch placed between a battery and system, this switch can help to significantly extend system battery life in mobile devices during shipping or periods of extended off time.

The GLF76431 helps to reduce power consumption with the best in class R_{ON} and a breakthrough on state I_Q of only 420 nA typical when the switch is on.

The GLF76431 integrated 1 ms slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switching can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF76431 slew rate control specifically limits inrush currents during turn-on to minimize voltage droop. The output discharge function makes output voltage off quickly during the reset period.

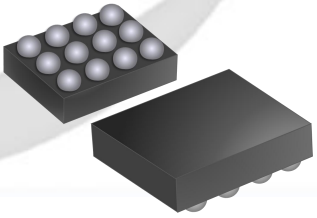
FEATURES

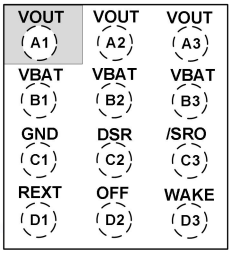
- Ultra-Low I_{SD}: 360 nA Typ at 3.6 V_{BAT}
- Ultra-Low I_Q: 420 nA Typ at 3.6 V_{BAT}
- Low R_{ON}: 19 mΩ Typ at 3.6 V_{BAT}
- I_{OUT} Max: 6 A
- Wide Input Range: 1.8 V to 5.5 V
  6 V_{abs} max
- Power Reset Mode by /SRO Pin Disconnect the downstream system from Battery Source
- Programmable delay and reset duration by one external resistor, R_{EXT}
  - Reset delay time by /SRO pin
  - Turn-off delay time by OFF pin
  - Power reset duration time
- Integrated Output Discharge During Reset Period
- Controlled Output Rise Time: 1 ms at 3.6 V_{BAT}
- Operating Temperature Range: - 40 °C to 85 °C
- HBM: 8 kV, CDM: 2 kV

APPLICATIONS

- Smart Wearables
- IoT Devices
- Medical Devices

PACKAGE





TOP VIEW

1.27 mm x 1.67 mm x 0.55 mm, 0.4 mm Pitch, WLCSP

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DEVICE OPTIONS / PACKAGING INFORMATION

Part Number	Top Mark	Programmable Timing by R_{EXT}	Output Discharge	Tape and Reel Packaging
GLF76431	AG	Reset Delay time, $t_{Reset-Dly}$ Power Off Delay Time, t_{SD} Power Reset Duration. t_{Reset}	90 Ω	3000 Pieces on 7 inch reel

APPLICATION DIAGRAM

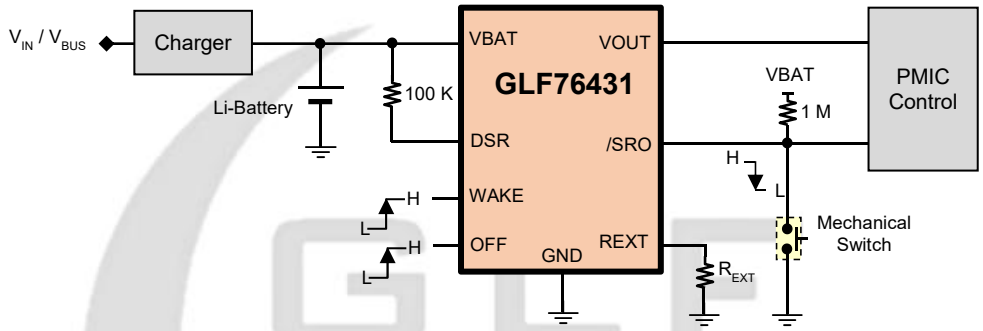

Figure 1. Typical Application with Charger IC

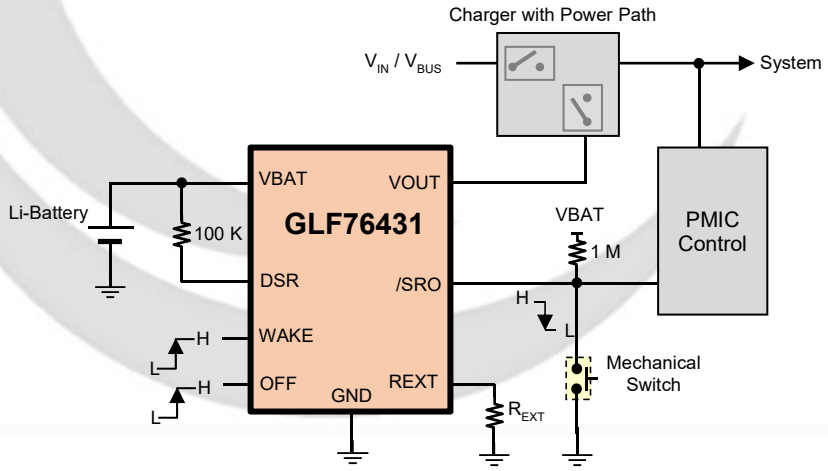

Figure 2. Typical Applications with Charger IC with Power Path and PMIC

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FUNCTIONAL BLOCK DIAGRAM

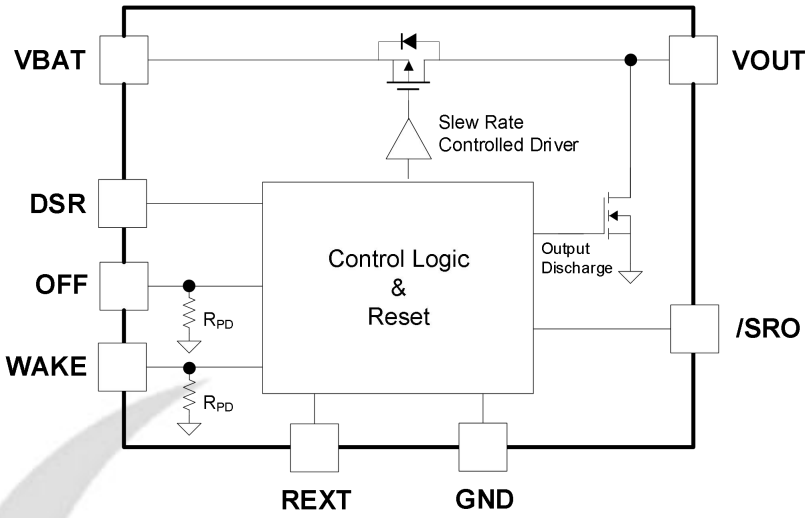

Figure 3. Functional Block Diagram

PIN CONFIGURATION

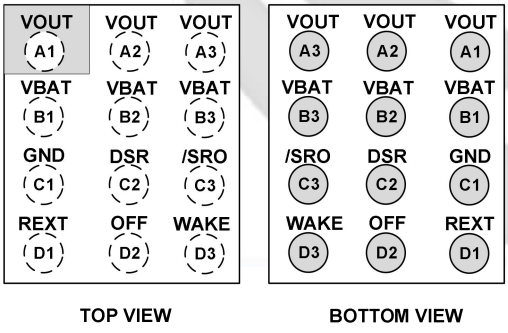

Figure 4. Top and Bottom View

PIN DEFINITION

Pin #	Name	Description
A1, A2, A3	VOUT	Switch Output
B1, B2, B3	VBAT	Switch Input. VBAT pin is connected to the positive input of an external battery
C1	GND	Ground
C2	DSR	Delay Selection Input. When this pin is pulled low, the device enters 0-second factory test mode and there is no delay for power-on, reset and power-off in this mode. To program delay and reset duration time, tie it to VBAT
C3	/SRO	Reset Input or Power-On. Active Low. It needs an external pull-up resistor. It is typically connected to the center between an external pull-up resistor which is directly tied with the battery and a mechanical key button on a device.
D1	REXT	An external resistor, R_{EXT} between REXT pin and GND sets a power reset delay, power off delay, and the reset duration time.
D2	OFF	Main Switch Off Input. It is triggered by the rising edge signal to change the main switch from on to off-state. It has an internal pull-down resistance, 10 MΩ Typ. to keep the OFF pin grounded.
D3	WAKE	System Wake Input. It is triggered by the rising edge signal to change the main switch from off to on-state. It has an internal pull-down resistance, 10 MΩ Typ. to keep the WAKE pin grounded.

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ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VBAT, VOUT	Each Pin Voltage Range to GND		-0.3	6	V
/SRO, WAKE, OFF	Each Pin Voltage Range		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			6	A
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VBAT, VOUT	Supply Input and Output Voltage	1.8	5.5	V
/SRO, WAKE OFF, REXT	Each Pin Voltage Range	0	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

Values are at VBAT = 3.6V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
I_Q	Quiescent Current	VBAT = /SRO, WAKE = OFF = GND I_{OUT} = 0 mA, Load Switch = On			0.42	0.55	µA
I_{SD}	Shut Down Current	VOUT=GND, Load Switch = Off			0.36		
$I_{Q_Dynamic}$	Supply Current	/SRO = GND, I_{OUT} = 0 mA WAKE = OFF = GND, Load Switch = On R_{EXT} =150 KΩ			2.4	3.5	µA
R_{ON}	On-Resistance	V_{BAT} = 5.5 V, I_{OUT}= 500 mA	Ta = 25 °C		16	22	mΩ
			Ta = 85 °C (1)		23		
		V_{BAT} = 4.2 V, I_{OUT}= 500 mA	Ta = 25 °C		17	23	
			Ta = 85 °C (1)		24		
		V_{BAT} = 3.6 V, I_{OUT}= 500 mA	Ta = 25 °C		19	25	
			Ta = 85 °C (1)		26		
		V_{BAT} = 3.0 V, I_{OUT}= 300 mA	Ta = 25 °C		20	27	
		V_{BAT} = 1.8 V, I_{OUT}= 300 mA	Ta = 25 °C		31		
R_{DSC}	Output Discharge Resistance	V_{OUT} = Off, I_{FORCE}= 10 mA			90		Ω
V_{IH}	Input Logic High Voltage (2)	V_{BAT} = 1.8 V to 5.5 V		1.2			V
V_{IL}	Input Logic Low Voltage (2)	V_{BAT} = 1.8 V to 5.5 V				0.4	

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R_{PD}	Pull-down Resistance on OFF and WAKE	V_{BAT} = 5.5 V		10		MΩ
Power On (Load Switch Turn-On) and Power Reset Timing by /SRO (1)						
t_{VON}	Turn-On Delay Time (Hold Time)	VBAT= DSR, R_{EXT} = 150 kΩ R_L = 150 Ω, C_L = 10 µF		0.8		ms
$t_{Reset-Dly}$	Delay Time (Hold Time) before Power Reset			7.5		s
t_{Reset}	GLF76431 Vout Reset Duration			470		ms
Power On (Load Switch Turn-On) Timing by WAKE						
t_{dON}	Turn-On Delay	R_L = 150 Ω, C_L = 10 µF		0.8		ms
t_R	VOUT Rise Time			1.0		
t_{ON}	Turn-On Time (3)			1.8		
Power Off (Load Switch Turn-Off) by OFF (1)						
t_{SD}	Delay to Turn Off Load Switch	VBAT= DSR, R_{EXT} = 150 kΩ R_L = 150 Ω, C_L = 10 µF		7.5		s
t_F	VOUT Fall Time			1.0		ms
t_{OFF}	Turn Off Time (3)			7.5		s

Notes:
1. By design; characterized, not production tested.
2. Input pins are /SRO, OFF, and WAKE.
3. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{SD} + t_F$

TIMING DIAGRAMS AND INPUT CONDITION

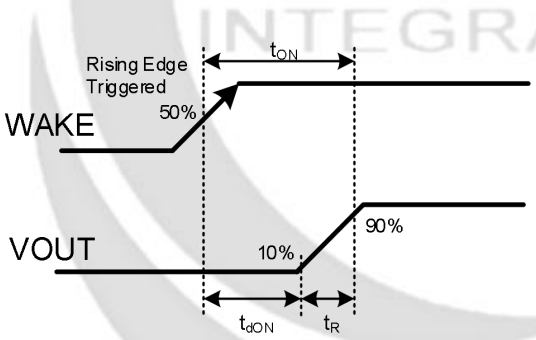

Figure 5. Power On by WAKE Pin

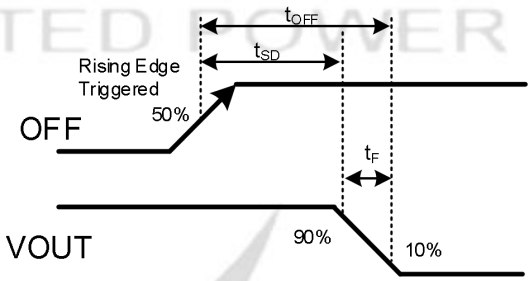

Figure 6. Power Off by OFF Pin

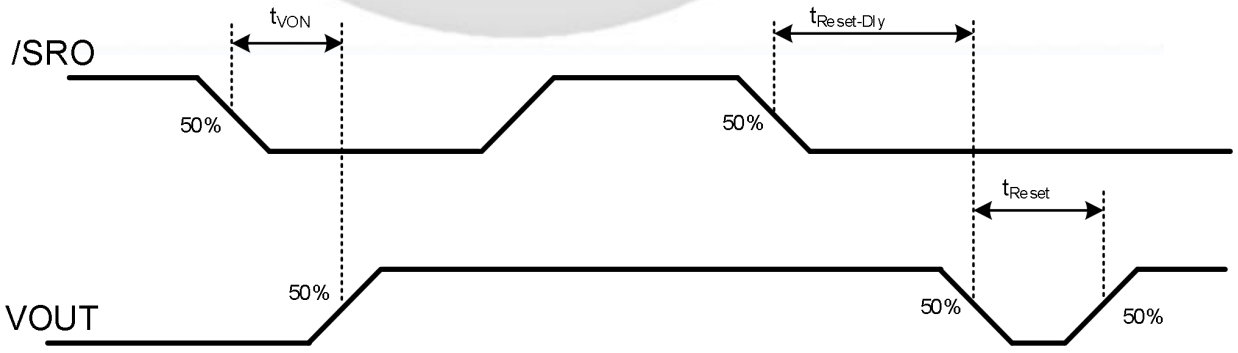

Figure 7. Power On and Power Reset by /SRO Pin

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Pin Name	/SRO	WAKE	OFF	VOUT
Default State	1	0	0	GND

Notes: 1=Logic High, 0=Logic Low, The VOUT=GND means the internal load switch is off.

Table 1. Pin Default State with Input Power Source

Function	/SRO	WAKE	OFF	DSR	Delay Time (Hold time) at R_{EXT}=150 kΩ	VOUT Action
Power-On	High to Low & Hold to Ground	X	X	Low	t_{VON} < 4 ms	VOUT = VBAT
	High to Low & Hold to Ground	X	X	High	t_{VON} = 0.8 ms	VOUT = VBAT
	High	Low to High Rising Edge Triggered	X	High	t_{dON} = 0.8 ms (2)	VOUT = VBAT
Power Reset	High to Low & Hold to Ground	X	X	Low	$t_{Reset-Dly}$ < 1 ms t_{Reset} = 470 ms	VOUT to GND to VOUT
	High to Low & Hold to Ground	X	X	High	Programmable (3) $t_{Reset-Dly}$ = 7.5 s t_{Reset} = 470 ms	VOUT to GND to VOUT
Power Off	High	Low	Low to High Rising Edge Triggered	Low	t_{SD} < 1 ms	VOUT to GND
	High	Low	Low to High Rising Edge Triggered	High	Programmable (3) t_{SD} = 7.5 s	VOUT to GND

Notes: 1. X = Don't Care
2. The t_{dON} can be longer with an external capacitor on the WAKE pin due to a RC time-constant to the trigger level of rising edge.
3. The programmable delay time by an external resistor, R_{EXT} presets both delay times of $t_{Reset-Dly}$ and t_{SD} at the same time.

Table 2. Input Conditions and VOUT Action

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TYPICAL PERFORMANCE CHARACTERISTICS

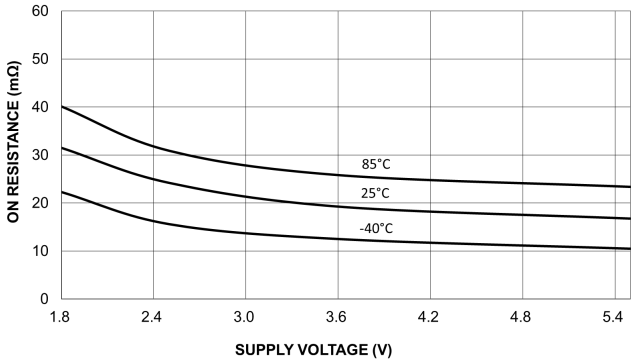

Figure 8. On-Resistance vs. Input Voltage

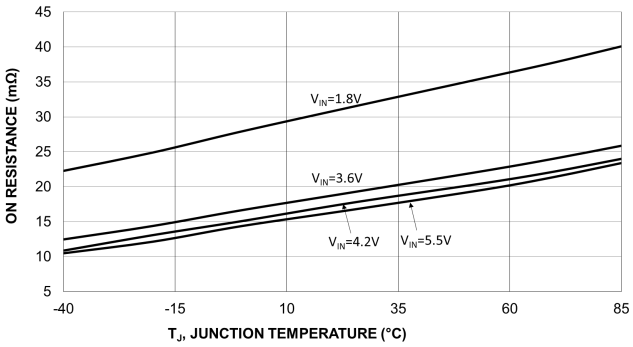

Figure 9. On-Resistance vs. Temperature

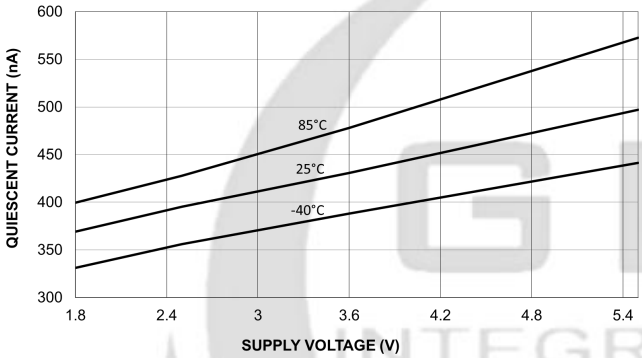

Figure 10. Quiescent Current vs. Input Voltage

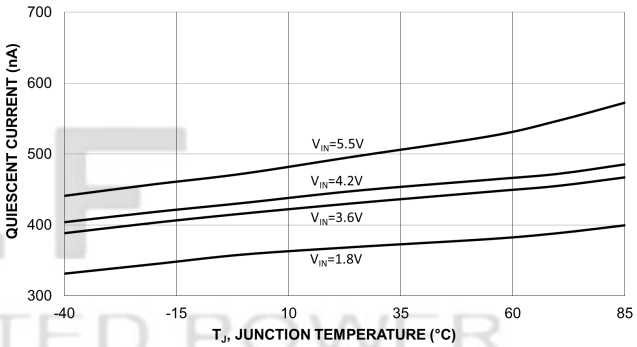

Figure 11. Quiescent Current vs. Temperature

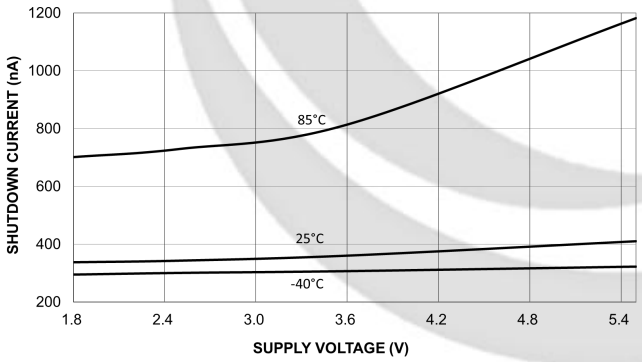

Figure 12. Shutdown Current vs. Input Voltage

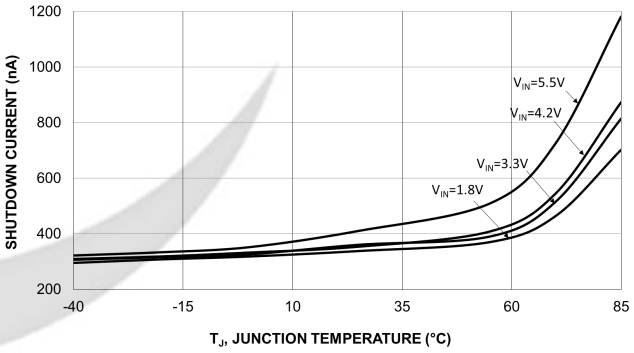

Figure 13. Shutdown current vs. Temperature

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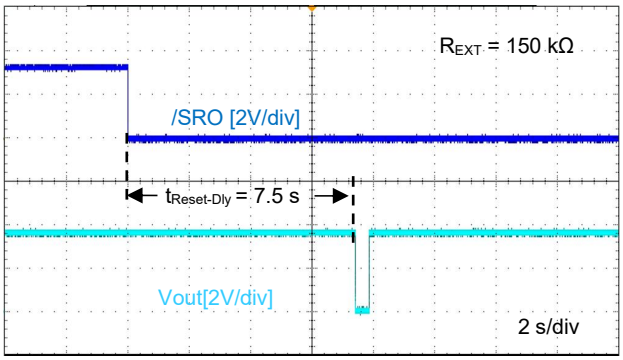

Figure 14. Delay time before Reset, $t_{Reset-Dly}$

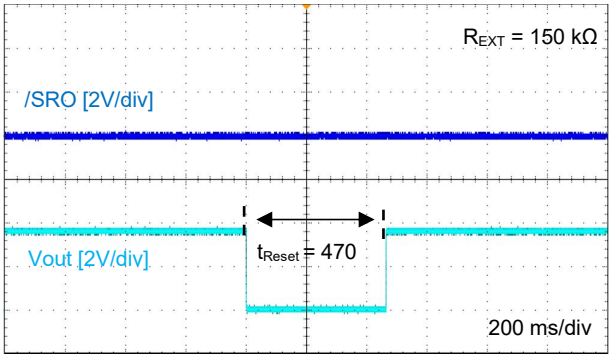

Figure 15. Vout Reset Duration, t_{Reset}

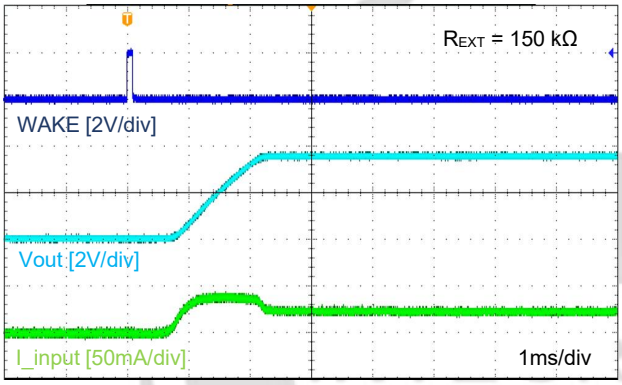

Figure 16. Turn-On Response
VBAT = 3.6 V, C_{IN} = 10 µF, C_L=10 µF, R_L=150 Ω

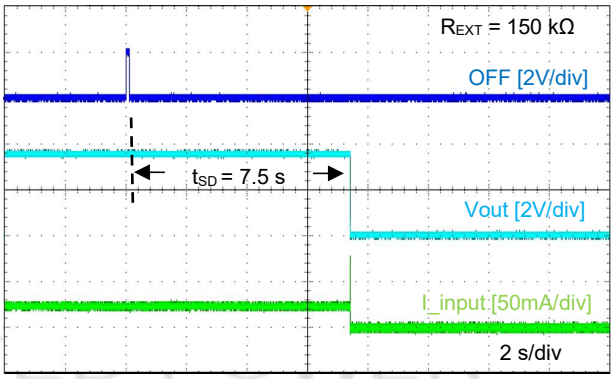

Figure 17. Turn-Off Response
VBAT = 3.6 V, C_{IN} = 10 µF, C_L=10 µF, R_L = 150 Ω

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APPLICATION INFORMATION

The GLF76431 is an integrated load switch with the configurable reset timer. Typical applications are shown in Fig.1 and Fig. 2.

Power On

There are two methods to enable the main switch of GLF76431 to wake up the system. The Fig.20 shows the power-on mode by /SRO and WAKE pins.

1) /SRO pin

When the main switch of GLF76431 is turned off and a system is disabled, holding the /SRO pin low for the preset delay time or hold time turns on the main switch to wake up the downstream system. The preset delay or hold time, t_{VON} is 0.75 s with R_{EXT}=150 kΩ when DSR is pulled high, and when DSR is pulled low, the GLF76431 bypasses the delay time t_{VON} and turns on Vout immediately.

2) WAKE pin

When a high signal is applied to the WAKE pin, the GLF76431 turns on the main switch to connect the battery ower to the downstream system. The Wake pin is initiated on a rising edge of a high signal. The t_{dON} of timing can be longer due to a RC time-constant to the trigger level of rising edge of WAKE pin. The WAKE pin has an internal pull-down resistance which is typically 10 MΩ to remain off state when no signal is asserted.

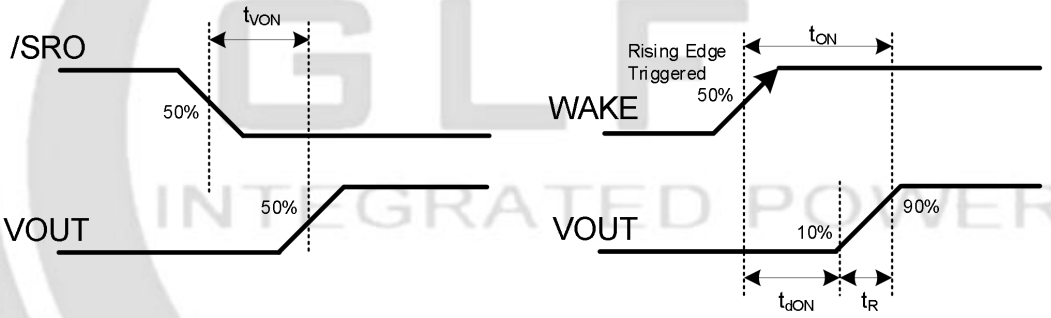

Figure 18. Power-On Mode by /SRO and WAKE

Reset Function

If a system reset is required to address malfunction of a mobile device or even during its normal operation, holding the /SRO pin low to GND by a key button for the preset delay time or hold time turns off the main switch to disconnect the batter power source from the downstream system. The output discharge switch is turned on to quickly bring VOUT down to GND when the main switch is turned off. In the pre-defined reset period, the GLF76431 reconnects the battery power source to the system by turning on the main switch and disabling the output discharge switch. With R_{EXT}=150 kΩ, the preset delay or hold time, $t_{Reset-Dly}$ is 7.5 s and the reset duration time, t_{Reset} is 470 ms when DSR is pulled high, and when DSR is pulled low, $t_{Reset-Dly}$ is less than1ms.

Note that if the /SRO is returned to high within the preset delay time or hold time [$t_{Reset-Dly}$], the VOUT remains in the on state without initiating the reset function.

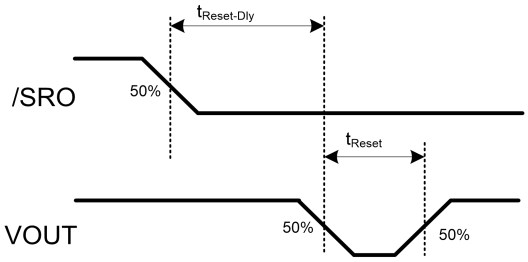

Figure 19. Reset Function by /SRO

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Power Off

When the OFF pin is triggered by a rising edge of the signal from low to high, the main switch of the GLF76431 is turned off in the preset delay time (t_{SD}) and enters the sleep mode. Note that if the /SRO pin action of going low and high is detected within the preset delay time (t_{SD}), the turn-off process is terminated and the VOUT remains in on state. To initiate the OFF pin again, the OFF pin needs to return to low and then a rising edge signal is asserted. The OFF pin has an internal pull-down resistor which is typically 10M Ohm to remain low state when no signal is asserted. The output discharge switch of the GLF76431 is turned on to quickly bring VOUT down to GND when the main switch is turned off. The preset delay time, t_{SD} is 7.5 s for the GLF76431 with R_{EXT}=150 kΩ when DSR is pulled high, and when DSR is pulled low, the GLF76431 bypasses the delay time t_{SD} and turns off Vout immediately.
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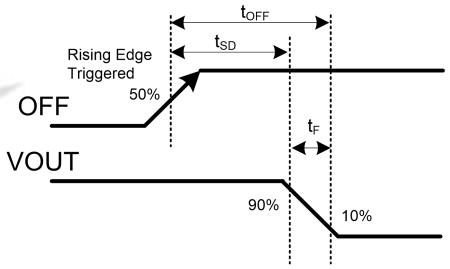

Figure 20. Power-Off Mode by OFF

Input Priority

The GLF76431 supports two different methods for turning on and off the main switch with /SRO, OFF, and WAKE pins. When two input pins are asserted at the same time or in any sequence, a higher priority input pin is chosen to be asserted and a lower priority input is ignored to avoid unnecessary conflicts.

Input	Priority (1 : Highest)
/SRO	1
WAKE	2
OFF	3

Table 3. Pin Priority

Output Discharge Function

The GLF76431 has an internal discharge switch on VOUT. It is activated to discharge an output capacitor quickly during the power reset period as well as when the main switch is turned off. During the sleep mode, the discharge switch remains in the on state holding the VOUT to GND. When the main switch is enabled, the output discharge switch is turned off.

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Program Delay Time and Reset Duration by an External Resistor

A resistor (R_{EXT}) between REXT pin and ground can program the reset delay ($t_{Reset-Dly}$), the reset duration time (t_{Reset}), and the power off delay (t_{SD}). The relationship between this resistor value and the timing is shown in table 4.

R_{EXT} (kΩ)	Power Reset Delay time $t_{Reset-Dly}$ (s)	Power Reset Duration t_{Reset} (s)	Power Off Delay Time t_{SD} (s)
1	1.86	0.12	1.87
10	2.34	0.15	2.34
20	2.83	0.18	2.83
36	3.51	0.22	3.53
50	4.08	0.26	4.08
100	5.86	0.37	5.89
150	7.50	0.47	7.50
200	9.00	0.57	9.04
250	10.49	0.66	10.48
300	11.89	0.75	11.89
400	14.63	0.91	14.59
450	15.89	0.99	15.92
500	17.20	1.08	17.20
600	19.71	1.24	19.68
700	22.20	1.39	22.16
800	24.61	1.54	24.56
900	26.97	1.69	26.91
1000	29.32	1.83	29.38
2000	51.20	3.20	51.11

Table 4. Programmable Timing vs. R_{EXT}

Output Discharge Function

The GLF76431 has an internal discharge switch on VOUT. It is activated to discharge an output capacitor quickly during the power reset period as well as when the main switch is turned off. During the sleep mode, the discharge switch remains in the on state holding the VOUT to GND. When the main switch is enabled, the output discharge switch is turned off.

Input Capacitor

A 0.1 μF capacitor is recommended to be placed close to the VBAT pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

A 0.1 μF output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

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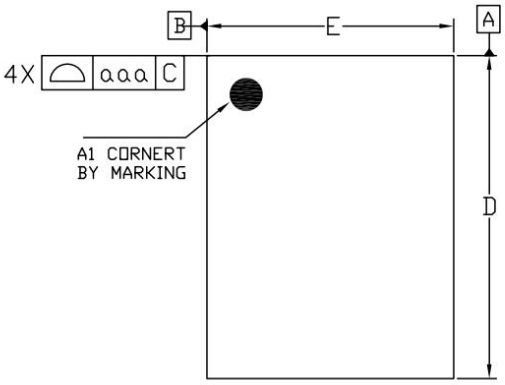
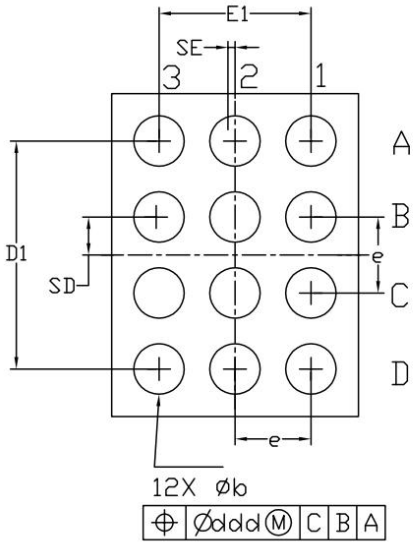
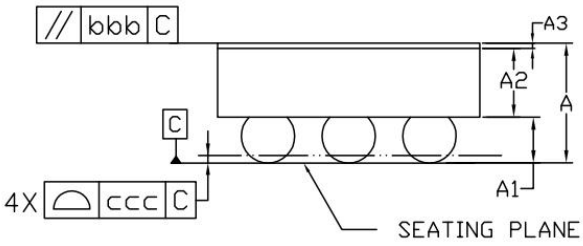
PACKAGE OUTLINE

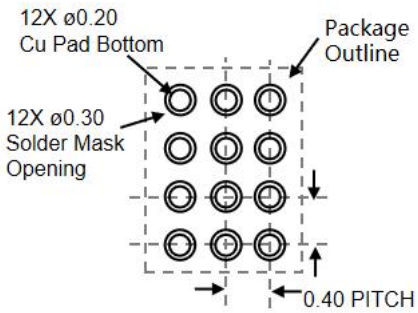






Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.175	0.200	0.225
A2	0.300	0.325	0.350
A3	0.020	0.025	0.030
D	1.655	1.670	1.685
E	1.255	1.270	1.285
D1	1.150	1.200	1.250
E1	0.750	0.800	0.850
b	0.215	0.265	0.315
e	0.400 BSC		
SD	0.200 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint



Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

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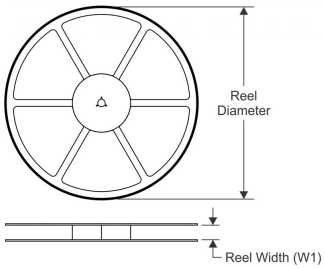
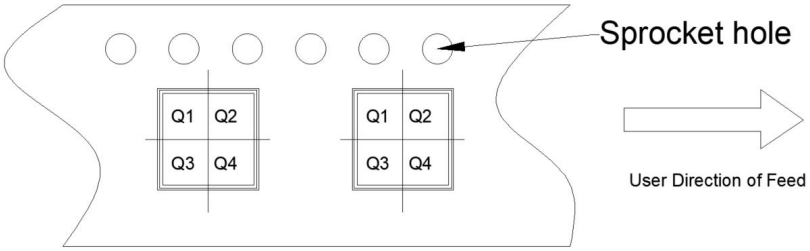
TAPE AND REEL INFORMATION

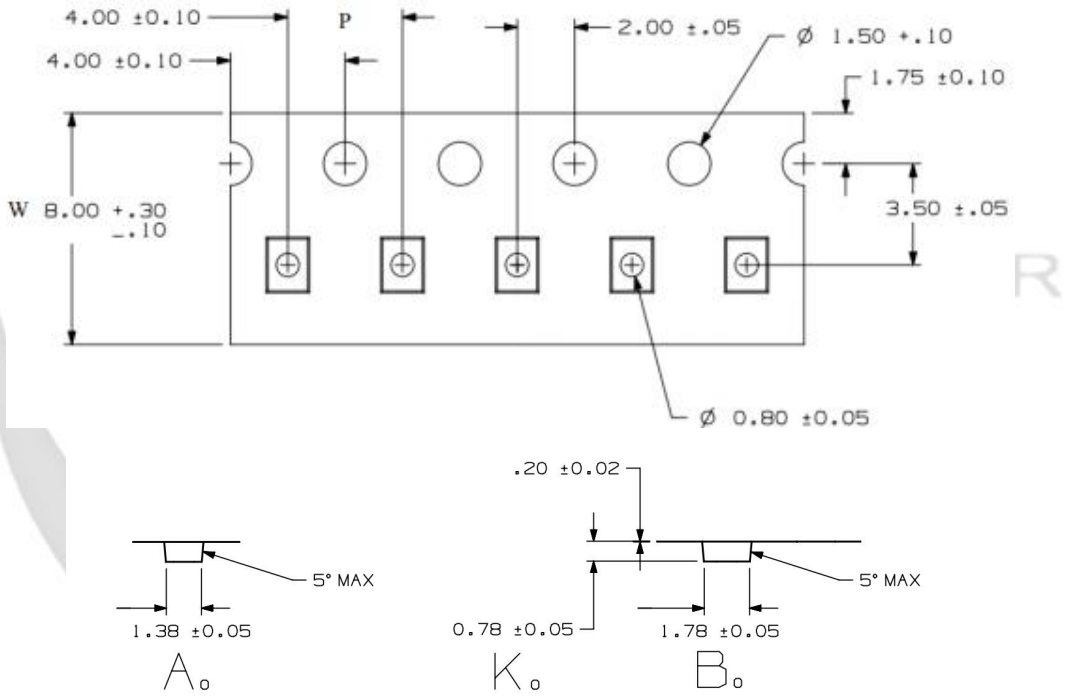
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF76431	WLCSP	12	3000	180	9	1.38	1.78	0.78	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

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SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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