GLF8114

4 A, 1.3 MHz Synchronous Step-Down DC/DC Converter With Low Quiescent Current

DESCRIPTION

The GLF8114 is a low quiescent current, peak current mode PWM synchronous step-down DC/DC converter. The device integrates switches capable of delivering an output current up to 4 A.

The GLF8114 operates over a wide input voltage range from 2.5 V to 5.5 V and runs in 1.3 MHz switching frequency to minimize the PCB and external components' size. The GLF8114 can automatically switches between PWM in heavy load operation and PFM for light-load operation to minimize the switch loss.

FEATURES

- Supply Voltage Range: 2.5 V to 5.5 V
- 4 A Output Current
- 1.3 MHz switching frequency
- Low I_Q: 21 µA Typ at 5 V_{IN}
- Low I_{SD}: 6 nA at 5 V_{IN}
- Efficiency up to 94 %
- Peak current mode control
  - Power Save Mode for Light Load
  - Internal Compensation
- Cycle-by-Cycle Over Current Protection
- Thermal Shutdown Protection
- Adjustable Soft Start Time
- Power Good Window Comparator

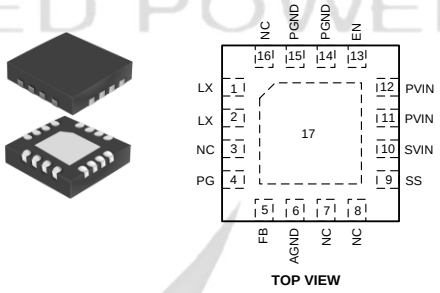
APPLICATIONS

- Solid State Drives
- Core Chipset Power Supplier
- Embedded / Portable Computing

DEVICE INFORMATION

Part Number	Top Mark	Package Type
GLF8114-Q3G13	FK	3 mm x 3 mm QFN-16L

PACKAGE



3 mm x 3 mm QFN-16L

APPLICATION DIAGRAM

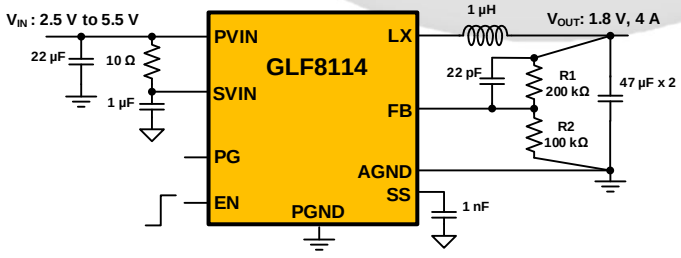


Figure 1. Typical Schematic

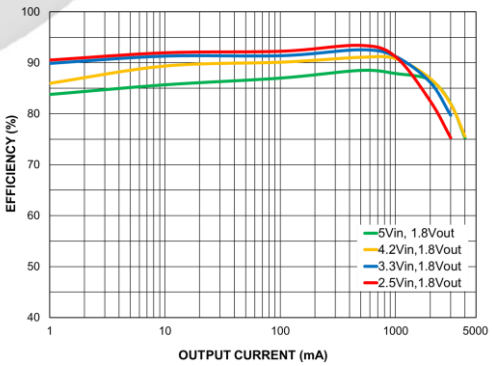


Figure 2. Efficiency

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FUNCTIONAL BLOCK DIAGRAM

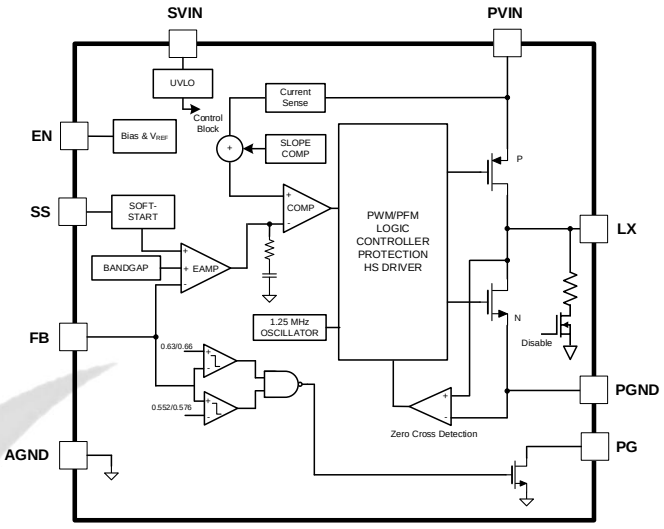
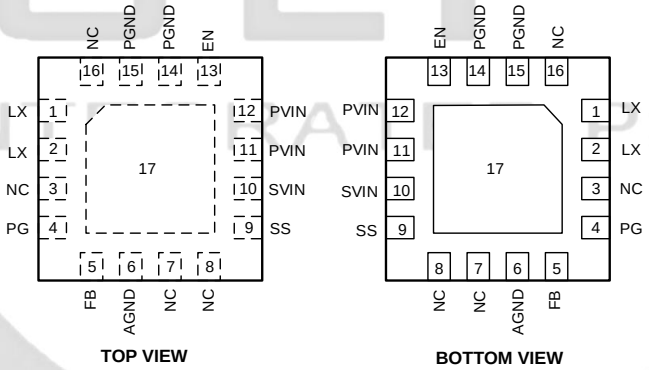


Figure 3. Functional Block Diagram

PIN CONFIGURATION



PIN DEFINITION

Pin No.	Name	Description
1,2	LX	Switch node of the power stage
3,7,8,16	NC	No Connection.
4	PG	Power Good open-drain output pin, connect a pull-up resistor to the input.
5	FB	Voltage feedback pin.
6	AGND	Analog ground
9	SS	Soft-start pin. Connect a capacitor from this pin to ground to program the soft-start time. Don't leave it floating.
10	SVIN	Signal Input Supply
11,12	PVIN	Power Input Supply
13	EN	Enable pin. A 10 MΩ pull-down resistor is integrated
14,15	PGND	Power ground
	Thermal Pad	Connect this pad to signal ground.

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ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
FB, EN	Voltage Range to GND	-0.3	V_{IN}+0.3	V
All other pins	Each Pin Voltage Range to GND	-0.3	6	V
P_D	Power Dissipation at T_A = 25 °C		2.6	W
T_{STG}	Storage Junction Temperature	-65	150	°C
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (Measured using 2S2P JEDEC std. PCB.)		67	°C/W
θ_{JC}	Thermal Resistance, Junction to Case		8	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage (VIN=PVIN=SVIN)	2.5	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

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ELECTRICAL CHARACTERISTICS

Typical values are at PV_{IN} = SV_{IN} = 5.0 V, V_{OUT} = 1.8 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
V_{UVLO}	Under Voltage Lockout	SV_{IN} Ramping Up	2.25	2.3	2.35	V
		Hysteresis		170		mV
I_Q	Supply Current	SV_{IN} = PV_{IN} = V_{EN} = 5.0 V, I_{OUT} = 0 mA		21		µA
		SV_{IN} = PV_{IN} = V_{EN} = 5.0 V, I_{OUT}=0 mA T_A = 85 °C (1)		22		
		SV_{IN} = PV_{IN} = V_{EN} = 3.3 V, I_{OUT}=0 mA		20		
I_{SD}	Shut Down Current	SV_{IN} = PV_{IN} = 5.0 V, V_{EN} = 0 V I_{OUT} = 0 mA		6		nA
		SV_{IN} = PV_{IN} = 5.0 V, V_{EN} = 0 V I_{OUT} = 0 mA, T_A=85 °C (1)		22		
		SV_{IN} = PV_{IN} = 3.3 V, V_{EN} = 0 V I_{OUT} = 0 mA		3		
R_{ON}	High Side Switch On Resistance	PV_{IN} = 5 V		75	85	mΩ
		PV_{IN} = 3.3 V		90	100	
	Low Side Switch On Resistance	PV_{IN} = 5 V		57	66	
		PV_{IN} = 3.3 V		65	75	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation (1)	1 mA to 4 A, C_{OUT}=47 µF x 2		0.5		%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation (1)	I_{OUT} = 1 A, PV_{IN} = 2.5 V to 5.5 V		0.5		%
R_{EN}	EN Pull Down Resistance	Internal Resistance		10		MΩ
V_{REF}	Feedback Reference Voltage		0.594	0.6	0.606	V
V_{IH}	EN Input Logic High Voltage	PV_{IN} = 2.5 V to 5.5 V	1.0			V
V_{IL}	EN Input Logic Low Voltage				0.5	V
f_{OSC}	Oscillator Frequency		1.1	1.3	1.5	MHz
V_{PG}	Power Good Rising Threshold	As a Percentage of the Regulated V_{OUT}	85	90	95	%
	Over Voltage Rising Threshold		105	110	115	%
V_{PG_Hyst}	Power Good Hysteresis			5		%
$V_{PG(LO)}$	PG Output Low Voltage	I_{PG} = 1 mA		40		mV
I_{PG}	PG Output High Leakage	V_{PG} = 5.5 V		3	10	nA
I_{LIM}	High-side Switch Current Limit	V_{IN} = 5 V	5	6	7	A
R_{DSC}	Output Discharge Resistance	EN = Low		60		Ω
TSD	Thermal Shutdown			150		°C
	Thermal Hysteresis			15		°C

Notes: 1. By design; characterized, not production tested

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TYPICAL PERFORMANCE CHARACTERISTICS

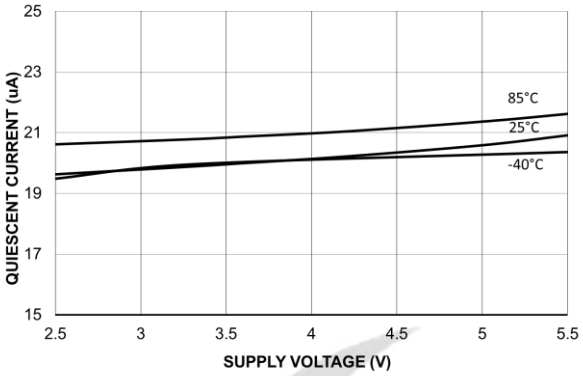

Figure 4. Quiescent Current vs. Supply Voltage

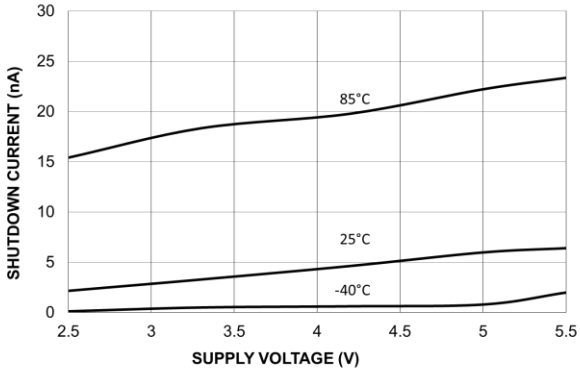

Figure 5. Shutdown Current vs. Supply Voltage

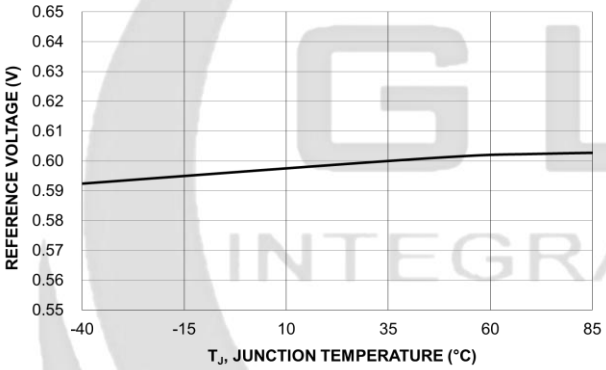

Figure 6. Reference Voltage vs. Temperature

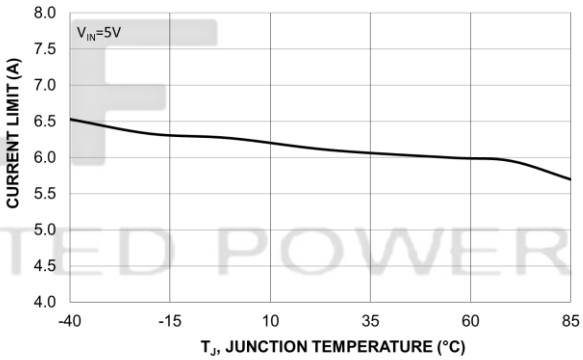

Figure 7. Current Limit vs. Temperature

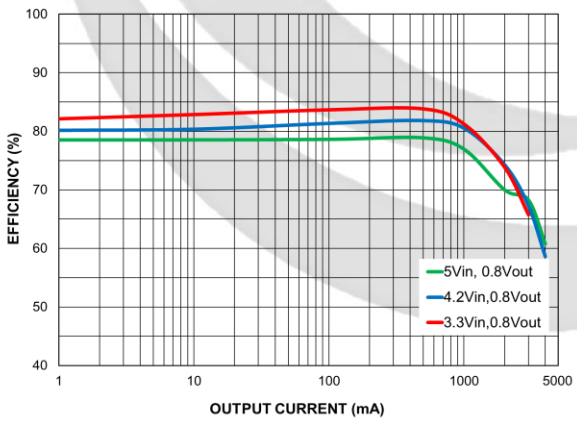

Figure 8. Efficiency vs. Load Current, V_{OUT} = 0.8 V

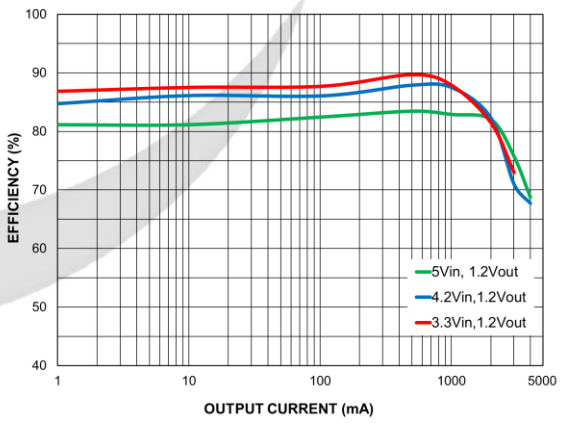

Figure 9. Efficiency vs. Load Current, V_{OUT} = 1.2 V

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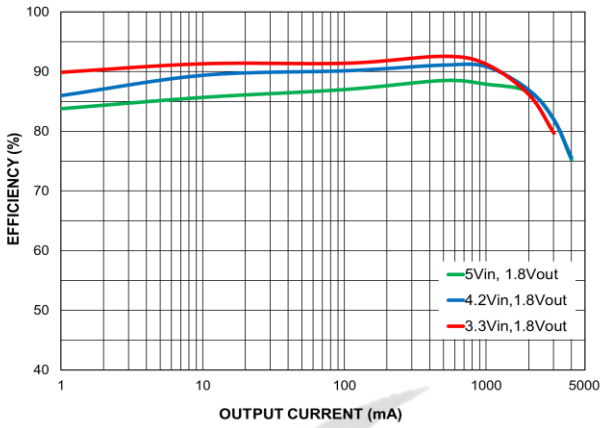

Figure 10. Efficiency vs. Load Current, V_{OUT} = 1.8 V

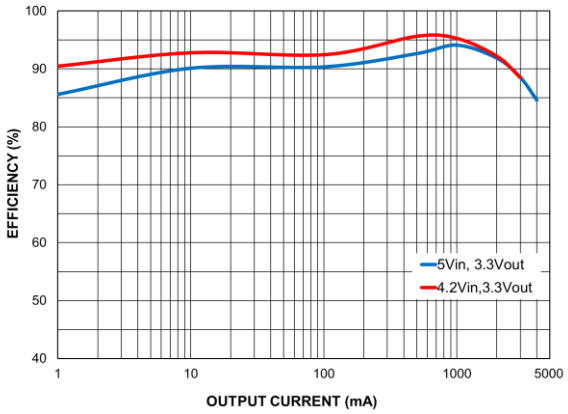

Figure 11. Efficiency vs. Load Current, V_{OUT} = 3.3 V

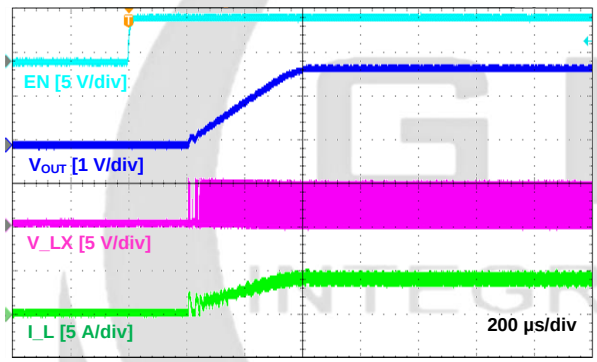

Figure 12. Startup from Enable
V_{IN} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 4 A

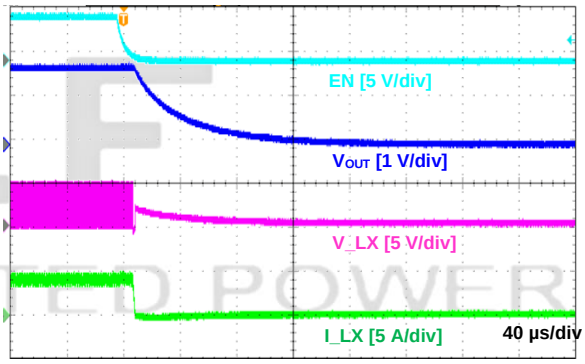

Figure 13. Shutdown from Enable
V_{IN} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 4 A

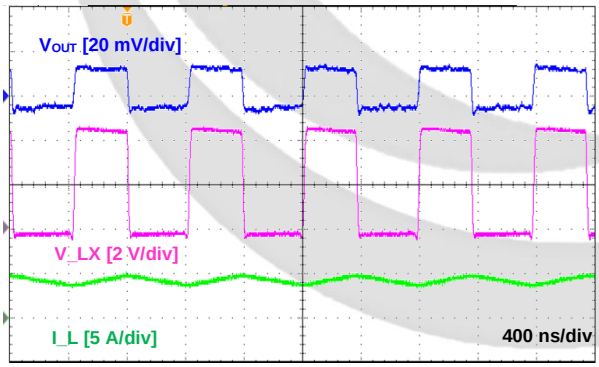

Figure 14. Output Ripple
V_{IN} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 4 A

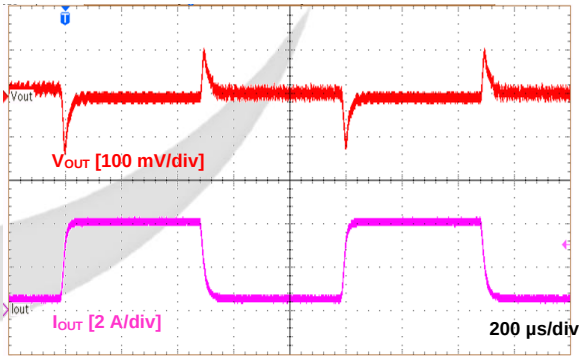

Figure 15. Load Transient
V_{IN} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 0.4 A to 4 A

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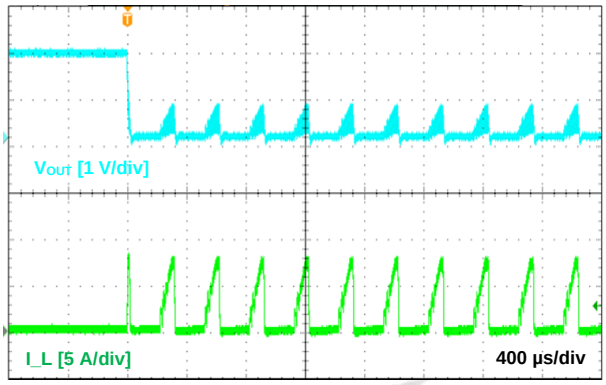

Figure 16. V_{OUT} Short Circuit Protection
V_{IN} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A

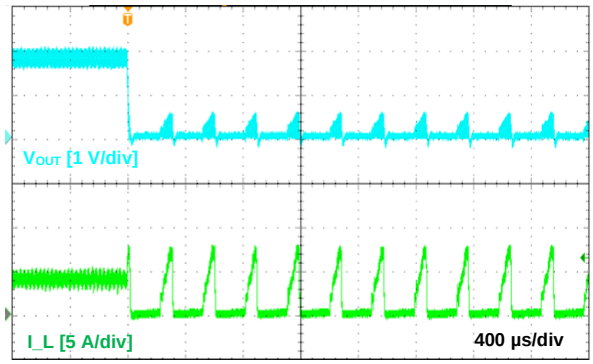

Figure 17. V_{OUT} Short Circuit Protection
V_{IN} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 4 A

APPLICATION INFORMATION

The GLF8114 is a low quiescent current, 4 A integrated synchronous step-down DC/DC converter operating from 2.5 V to 5.5 V input supply. Using 1.3 MHz constant frequency and peak current mode control, the GLF8114 features fast transient response with small external components. The internally compensated regulator requires only external feedback resistors to set the output voltage.

Setting the output voltage

The output voltage is set by an external resistor divider as shown in Figure 1 according to the following equation.

$$V_{OUT} = (R1 + R2) \times V_{REF} / R2$$

A 200 kΩ value resistor is recommended for R1 to achieve high efficiency at light load and good noise immunity. A 10 pF~100 pF ceramic capacitor in parallel with R1 can help to speed up the load transient response.

Enable Operation and Undervoltage Lockout

The GLF8114 can be activated by EN pin high. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller. When the device is disabled, the internal discharge MOSFET will turn on to discharge the output capacitor quickly. VIN must remain present for this function. The undervoltage lockout (UVLO) function turns off both high-side and low-side switches to prevents mis-operation if the input voltage falls below the input falling threshold. The device fully operates to regulate the output voltage as the input voltage increase above the rising UVLO threshold.

Soft Start

When EN goes high, the soft-start circuitry controls the output voltage gradually to rise to a nominal value. The soft-start time can be programmed by an external capacitor between the SS and AGND pin. The soft-start time is calculated according to the following equation.

$$t_{SS} = C_{SS} \times 0.6\ V / 1.6\ \mu A$$

Power Good Indication

The GLF8114 has a built-in Power Good (PG) function. PG is an open-drain output pin, and is specified to sink up to 1mA current. PG is connected to VIN through a pull up resistor. Only when output voltage reaches in the windows between low-side and high-side thresholds, the PG pin goes high impedance, otherwise it will stay low.

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Over Load Condition

The device senses the current in the high side switch when it is turned on after the blanking time and then compared with its current limit threshold in every switching cycle. If the peak current reaches the current limit threshold after the minimum on time, the high-side switch is turned off immediately. If this over current condition exists for 25 switching cycles (~20 µs), the device turns off both high side and low side switches for about 100 µs. It allows the inductor current to decrease through the body diode of the low side switch and restarts again with a soft start cycle. The device maintains this operation limiting the output power until an over load condition presents.

Thermal Shutdown

The junction temperature of the device is monitored by an internal temperature sensor. If the junction temperature exceeds 150 °C (Typ.), the device goes in thermal shutdown with a hysteresis of typically 20°C. Once the junction temperature cools down below the hysteresis level, the device resumes normal operation.

Output inductor Selection

The maximum peak-to-peak output inductor current ripple is given by

$$\max\left(\Delta i_{pp}\right)=\frac{V_o}{L_o\cdot f_{sw}}\cdot\left(1-D_{\min}\right)$$

It is suggested to choose the maximum ripple current to be 30 % to 60 % of the maximum output current. The saturation current of inductor must be larger than:

$$\mathrm{I}_{SAT}=\mathrm{I}_{OUT_MAX}+\frac{V_{OUT}\cdot\left(1-D_{\min}\right)}{2\cdot f_{sw}\cdot L}$$

It is recommended to choose a saturation current for the inductor that is approximately 20 % to 30 % higher than I_{SAT}. In addition, the low DCR of the inductor is desirable to keep the power dissipation low in the inductor.

Input Capacitor Selection

The AC RMS current of input capacitor is given by

$$I_{acrms}\left(C_{in}\right)=\sqrt{D\cdot\left(1-D\right)}\cdot I_o$$

The maximum RMS current occurs at D = 0.5

$$\max\left[I_{acrms}\left(C_{in}\right)\right]=\sqrt{0.5\cdot\left(1-0.5\right)}\cdot 4A=2A$$

A 22 µF to 100 µF X5R or X7R ceramic capacitor of above 6.3 V voltage rating is recommended for input capacitor, and it should be able to handle the maximum ripple current. It must be placed as close as possible between PVIN and PGND pin. Another 1 µF ceramic capacitor is recommended to added across SVIN and SGND pin.

Output Capacitor Selection

The output capacitor is used to filter out the ripples and keep the output voltage stable during the transient duration. It is recommended to use X5R or X7R ceramic capacitors with above 6.3V voltage rating and more than 47 µF capacitance.

Board Layout

The following checklist is recommended to ensure proper operation of the GLF8114 when laying out the printed circuit board. It minimizes parasitic circuit elements and optimize the operation performance.

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1. The placement of C_{IN}, inductor L and C_{OUT} should be as close as possible. Especially the copper area of LX node should be minimized to reduce the switching noise. The adequate trace width is needed for power paths where the high currents flow.
2. Pay attention to the grounding. Power ground and signal ground must be separated. They should be connected in one node.
3. Keep the control circuitry like feedback network from power path. If the PCB board is a multi-layer printed circuit board, dedicate one solid layer in the middle layers for a power ground plane and another solid layer underneath this layer for a signal ground plane. Place control circuitry at the bottom layer to be immune to the noises from the top layer.
4. The thermal pad of the device should be connected to an adequate ground plane through at least 4 vias to dissipate heat.

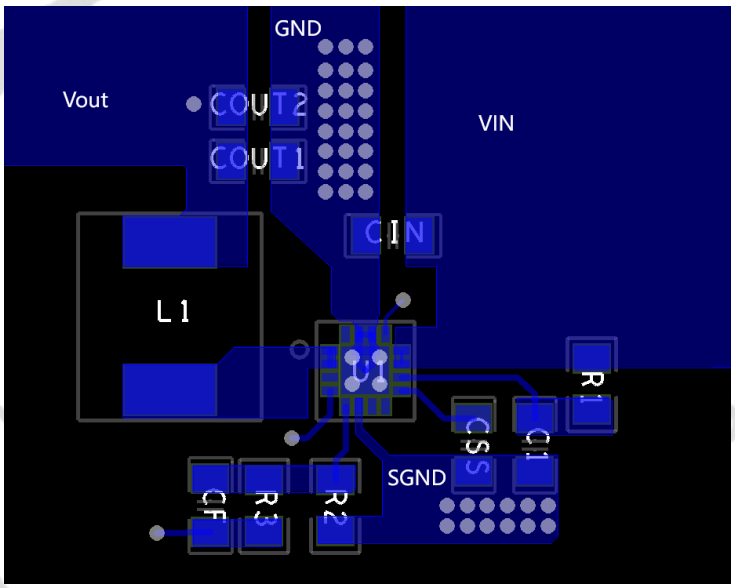

Figure 18. PCB Layout Reference

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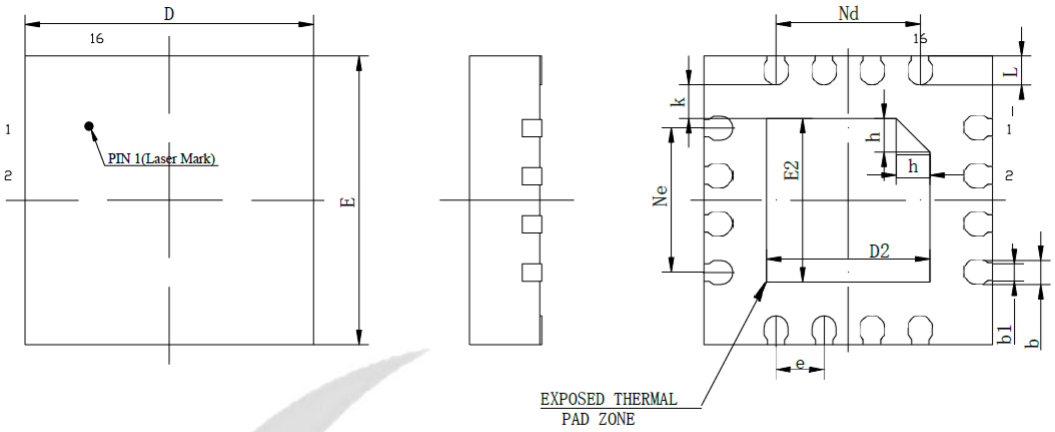
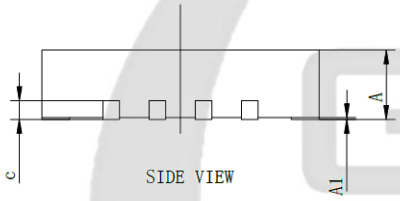
PACKAGE OUTLINE



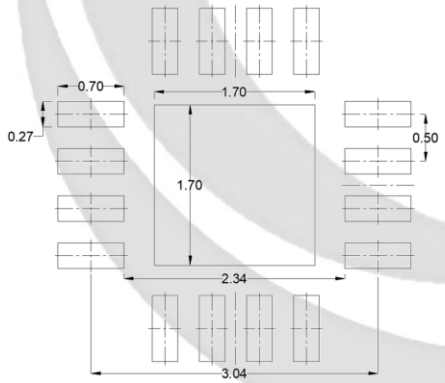
TOP VIEW

BOTTOM VIEW



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	2.90	3.00	3.10
D2	1.60	1.70	1.80
e	0.50BSC		
Ne	1.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
L	0.25	0.30	0.35
h	0.30	0.35	0.40
k	0.30	0.35	0.40

Recommended Footprint



Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

PACKAGING INFORMATION

Part Number	Package	Pins	Pitch	Top Mark	Moisture Sensitivity Level	Environmental Information
GLF8114-Q3G13	QFN 3x3	16	0.40mm	FK	MSL3	ROHS+HF

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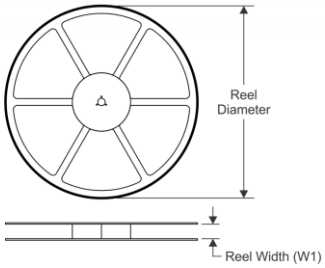
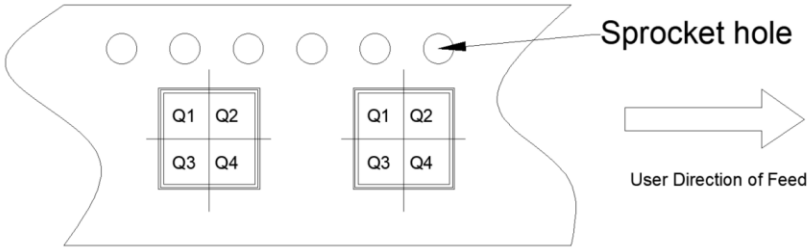
TAPE AND REEL INFORMATION

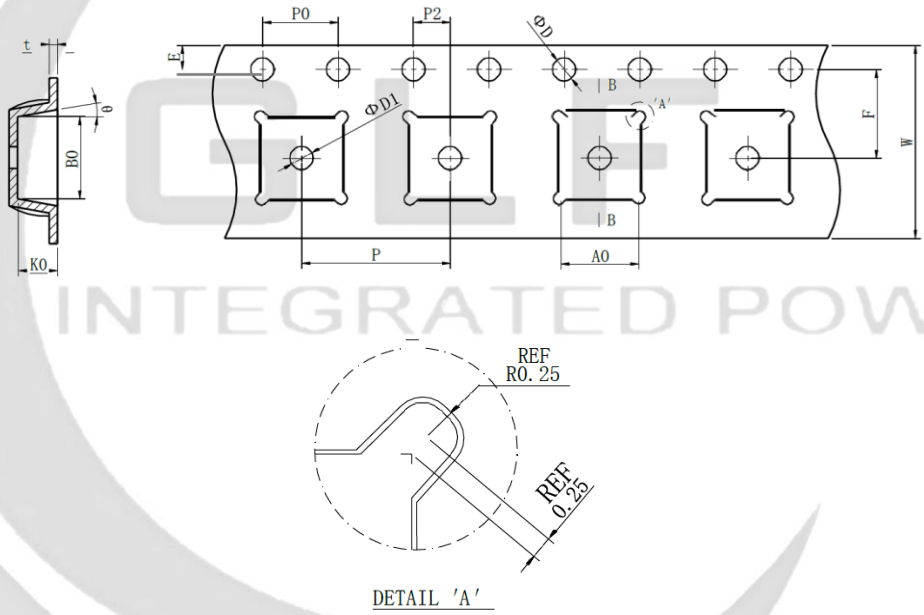
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF8114-Q3G13	QFN 3x3	16	5000	329	12.4	3.3	3.3	1.1	8	12	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

K0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

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SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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