1 Description

GLF70602 is a chip specially designed for wearables application, which provides a perfect solution for charging and power line communication. GLF70602 is integrated with NVDC structure, a linear/switch charger management, a single signal line for data bidirectional transmission, battery gauge meter, 12-bit SAR-ADC and I^2C interface. The I^2C interface is used for charging management and data communication.

GLF70602 integrates the VINCMD module for sending and receiving VINCMD.

For TWS, GLF70602 also supports the auto-detection of earbuds casein/caseout status.

2 Applications

TWS, wearables, IoT

3 Features

- VBAT standby current: 3uA
- Ship-mode standby current: 400nA
- VIN BV = 16V
- VIN OVP = 6.0V/6.8V
- 2mA~500mA register configurable constant charging current
- VFLOAT 4.00V~4.10V register configurable, step=25mV, accuracy of ±0.5%
- VFLOAT 4.10V~4.55V register configurable, step=12.5mV, accuracy of ±0.5%
- ITC and ITERM: 1mA~40mA register configurable
- Watchdog function, 40s/80s/160s configurable
- Support DCDC charging with 93% efficiency
- Bidirectional communication with communication direction auto-switching / manual switching mode, up to 3Mbps
- Powerline bidirectional communication:
  - support voltage mode bidirectional communication
  - support voltage mode receive and current mode send
- Auto detection of earbuds in-case /out-case status integrated
- Support I^2C, up to 400kbps
- 12bit SAR-ADC，with VIN, VBAT, NTC voltage, ICC current and IVIN current data readable
- Battery gauge meter integrated with accuracy of 5%
- Package: CSP - 2.0 mm x 2.0 mm

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

4 Typical Application Circuit

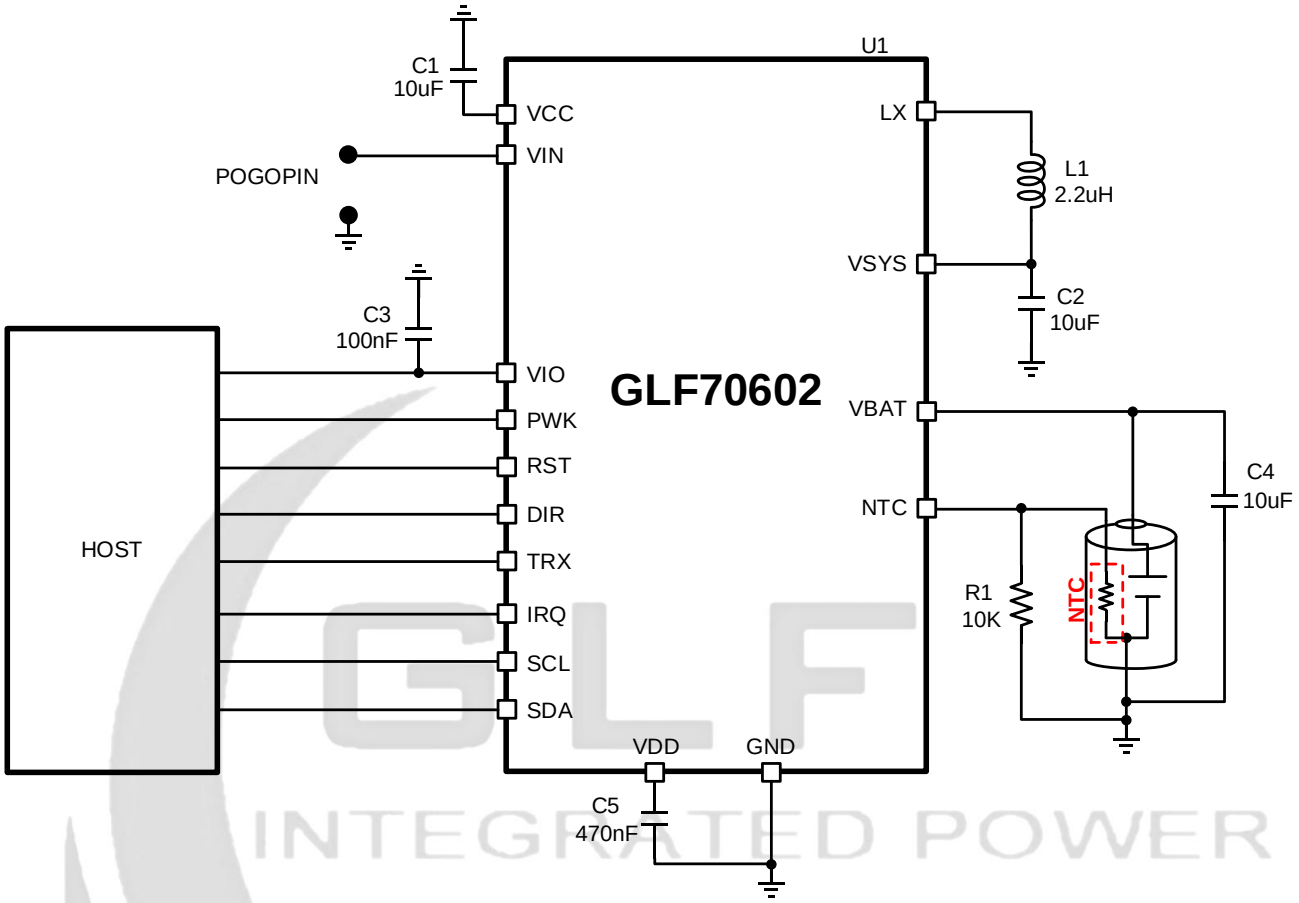


Figure 4-1 BUCK Mode Typical Application Circuit

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

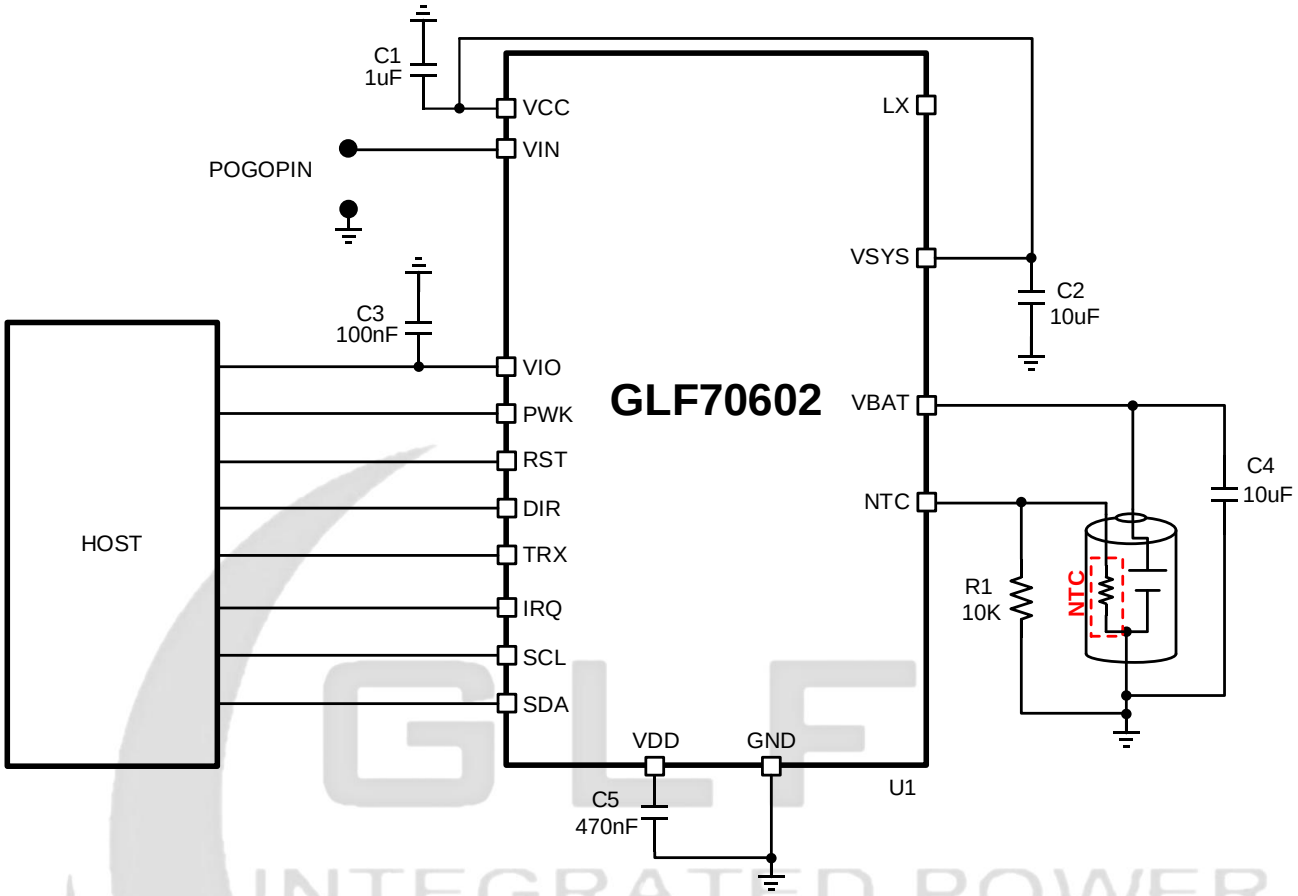


Figure 4-2 Linear-Bypass-Mode Typical Application Circuit

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

Table of Contents

1 Description 1
2 Applications 1
3 Features 1
4 Typical Application Circuit 2
5 Pin Configuration and Functions 6
6 Specifications 7
6.1 Absolute Maximum Ratings 7
6.2 Recommended Operating Conditions 7
6.3 ESD Ratings 7
6.4 Thermal Information (CSP) 7
6.5 Electrical Characteristics 8
6.6 Typical Characteristics 12
7 Functional Description 14
7.1 Block Diagram 14
7.2 Input Protection 15
7.3 Charger Mode 15
7.4 Charging Process 16
7.5 ChargeEnd Mode 17
7.6 Charging Protection 18
7.7 Recharge 18
7.8 BFET Charging/Discharging 18
7.9 NTC Monitoring 18
7.10 Communication 19
7.11 VIO power supply 21
7.12 CaseIn/CaseOut Status Detection 21
7.13 RST and PWK Output 22
7.14 VINCMD 22
7.15 Gas Fuel 25
7.16 ADC 25
7.17 Watchdog 26
7.18 IRQ 26
7.19 I2C Interface 28
8 Register Summary 29
8.1 Register List 29
9 Application and Implementation 60
9.1 System Example 60
9.2 Bill of Materials 60
10 Package Outline and Layout 61
10.1 Package Outline(CSP) 61
10.2 Recommended Land Pattern(CSP) 62
10.3 Layout Guidelines 63
10.4 Layout Example 63

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

11 Packaging and Ordering Information 64
11.1 Ordering Information 64
11.2 Tape and Reel Information 64
11.3 Package Quantity Information 64

GLF INTEGRATED POWER

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

5 Pin Configuration and Functions

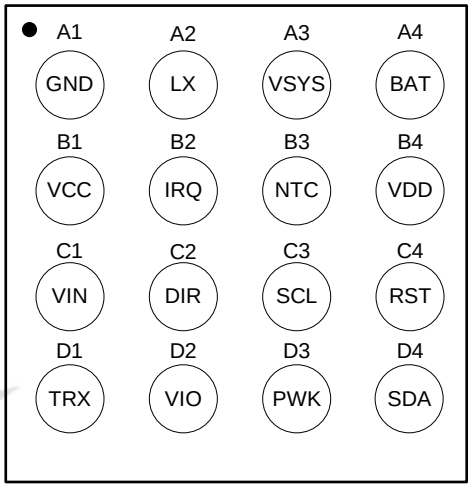


Figure 5-1. GLF70602 Pin Configuration

Name	NO.	I/O	Function
GND	A1	GND	GND
LX	A2	O	Switching node, connected with inductor
VSYS	A3	O	Power supply for Bluetooth IC
BAT	A4	O	Battery anode
VCC	B1	O	Bluetooth charging power supply detection
IRQ	B2	O	Interrupt output interface with open-drain output, 100K Ohm resistor pull up to VIO
NTC	B3	I	Battery temperature sensor input
VDD	B4	O	Internal power source VDD, 470nF needed
VIN	C1	I/O	POGOPIN power supply input; input/output port for communication with the case
DIR	C2	I	Communication direction controlling pin, neither internal pull-up nor pull-down. For IODIR，if DIR=0，data sending from VIN to TRX；if IDR=1，data sending from TRX to VIN。
SCL	C3	I	I2C clock input port with 10K Ohm internal pull-up resistor to VIO
RST	C4	O	Connection to the reset interface of the Bluetooth earbuds MCU with open-drain output, no internal pull-up resistor internal
TRX	D1	I/O	Push-pull output, bidirectional communication port; push-pull output, hi-z input
VIO	D2	I	SCL、SDA、TRX、DIR、STA port external power supply input
PWK	D3	O	Power Key port with open-drain output, no internal pull-up resistor
SDA	D4	I/O	I2C data port with internal 10K Ohm resistor pull up to VIO

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

6 Specifications

6.1 Absolute Maximum Ratings (1)

	Min	Max	Unit
VIN voltage	- 0.3	16	V
Other pin voltage	- 0.3	6	V
Storage temperature	- 55	150	℃
Junction temperature	- 40	150	℃

6.2 Recommended Operating Conditions (2)

		Min	Nom	Max	Unit
T_A	Ambient temperature	- 20	27	85	℃
T_J	Junction temperature	- 40	27	125	℃
V_{IN}	input voltage	- 0.3	5.0	5.5	V

6.3 ESD Ratings

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per Mil-Std-883H Method 3015.8 1, all pins	± 2000	V
		Charged device model (CDM), per JS-002-2018, all pins	± 1000	V

6.4 Thermal Information (CSP)

Thermal Metric		Package Type	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.8	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	83	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	℃/W

Note:
(1) Stress beyond absolute maximum rating may cause permanent damage to device.
(2) The device is not guaranteed to function outside of its operating conditions.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

6.5 Electrical Characteristics

V_{IN}=5V, V_{BAT}=3.85V, T_a=25℃ for typical values (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VIN	input voltage		4.4	5.0	5.8	V
VIN_{OVP}	VIN OVP threshold		5.8	6.0	6.2	V
VIN_{UVLO}	VIN UVLO threshold	VIN_UVLO [1:0] = 2'b11	3.7	3.8	3.9	V
VINUV_hys	Hysteresis of UVLO			200		mV
I_{STDB_VIN}	standby mode VIN power consumption	V_{IN}=5.0V，VCC on，VBAT fully charged		300	350	uA
	standby mode VIN power consumption	V_{IN}=5.0V，VCC off，VBAT fully charged		12	15	uA
I_{STDB_VBAT}	standby mode VBAT power consumption	V_{IN}=5.0V，VCC on，VBAT fully charged		20	35	uA
	standby mode VBAT power consumption	V_{IN}=5.0V，VCC off，VBAT fully charged		5	7	uA
	standby mode VBAT power consumption	V_{IN}=0V，VBAT=4.35V		5	7	uA
I_{SD_SM}	Shipmode VBAT power consumption	V_{IN} = 0V Vsys off		0.4	0.9	uA
I_{VCCOCP}	VCC OCP		850	1000	1150	mA
T_{VCC_OC}	VCC OCP deglitching time			250		μS
Ron_{VCC}	VIN to VCC turn on resistance			120		mΩ
PMOS	BUCK high-side turn on resistance			100		mΩ
NMOS	BUCK low-side turn on resistance			300		mΩ
Ron_{BFET}	VBAT to VSYS turn on resistance			100		mΩ
OTP	Over temperature protection threshold			145		℃
OTP_{HYS}	OTP hysteresis			20		℃
Charge Mode						
V_{FLOAT}	ChargeEnd voltage	Register configurable，Step=12.5mV	4.179	4.200	4.221	V
			4.328	4.350	4.372	V
			4.378	4.400	4.422	V
			4.428	4.450	4.472	V
V_{RECHG}	VBAT recharge voltage	<0x21>.b[2:0]=3'b000		3.9		V
VSYS_MIN	VSYS Voltage Regulation	<0x20>.b[5:4]=2'b10	3.45	3.50	3.55	V
Freq_Buck	Buck switching frequency				1.8	MHz
Duty					93.8%	

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

Electrical Characteristics(continued)

V_{IN}=5V, V_{BAT}=3.85V, T_a=25℃ for typical values (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Constant current (CC) mode charging current	<0x1E>.b[6:0]=0x0E		30		mA
	Accuracy I_{CC}	I_{CC} ≤ 20mA	-1.5		+1.5	mA
		I_{CC} ≤ 200mA	-7%		+7%	
		I_{CC} > 200mA	-10%		+10%	
I_{TRIKL}	Trickle charge (TC) current	Register configurable		3		mA
	Accuracy I_{TRIKL}	I_{TRIKL}=1mA	-0.5		+0.5	mA
		I_{TRIKL} ≤ 20mA	-1.5		+1.5	mA
		I_{TRIKL} > 20mA	-7%		+7%	%
V_{TRIKL}	TC mode to CC mode threshold voltage	V_{BAT} rise，V_{TRIKL}=3.0V	2.9	3.0	3.1	V
V_{TRHYS}	CC mode to TC mode hysteresis voltage			150		mV
V_{PRE}	pre-change voltage			2.2		V
I_{PRE}	pre-charge current	VBAT < VPRE	1.5	3.0	5.0	mA
I_{TERM}	Terminated current	Register configurable	-	3	-	mA
	Accuracy I_{TERM}	I_{TERM} =1mA	-0.5		+0.5	mA
		I_{TERM} ≤ 20mA	-1.5		+1.5	mA
		I_{TERM} > 20mA	-7%		+7%	%
T_{LIM}	Threshold temperature in the limited temperature mode			110		℃
T_{TRIKL}	Trickle charge overtime	Register configurable		1		h
T_{CC}	Trickle charge overtime	Register configurable		3		h
Discharge Mode						
$VBAT_{UV}$	VBAT UVLO threshold voltage	Register configurable	2.575	2.600	2.625	V
$VBAT_{UVHYS}$	VBAT UVLO hysteresis voltage			400		mV
T_{BATUV}	VBAT UVLO debounce time			64		mS
I_{BAT_OC}	VBAT over current threshold			200		mA
	Accuracy I_{BAT_OC}		-20%		+20%	%
T_{BAT_OC}	VBAT over current debounce time			64		μS
V_{SYS_SHORT}	VSYS short voltage threshold			V_{BAT}-0.7		V

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

Electrical Characteristics(continued)

V_{IN}=5V, V_{BAT}=3.85V, T_a=25℃ for typical values (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Discharge Mode						
T_{SYS_SHORT}	VSYS short debounce time			8		mS
VIO						
VIO	Voltage range of the external VIO power supply	BaudRate = 3Mbps	1.0	1.8	VBAT	V
TRX，DIR，SCL，SDA，IRQ Pins Logic Level						
V_{IL}	TRX、SCL、SD Input low threshold voltage				0.3* V_{IO}	V
V_{IH}	TRX、SCL、SDA Input high threshold voltage		0.7* V_{IO}			V
V_{OL}	SDA、IRQ pull down driving	SINK current = 10mA			0.4	V
Rpulldown	PWK、RST pull-down internal resistance			1		kΩ
I_{OHTRX}	TRX logic high level driving	IO DIR mode		5		mA
I_{OLTRX}	TRX logic low level driving	IO DIR mode		5		mA
VIN Pin Logic Level						
V_{ILCOMM}	VIN Input low threshold voltage	Communication mode			0.5	V
V_{IHCOMM}	VIN Input high threshold voltage	Communication mode	1.7			V
V_{ILCMD}	VIN Input low threshold voltage	VIN receiving private controlling instructions			0.5	V
V_{IHCMD}	VIN Input high threshold voltage	VIN receiving private controlling instructions	1.7			V
Rpulldown	VIN、TRX internal pull down resistance	AutoDIR mode		4		kΩ
Rpushup	VIN、TRX internal pull up resistance	AutoDIR mode		4		kΩ
I_{OHVIN}	VIN logic high level driving	IODIR and RegDIR mode		3		mA
I_{OLVIN}	VIN logic low level driving	IODIR and RegDIR mode		10		mA
Timing Parameter						
T_{VINOK}	VINOK debouncing time			32		mS
I2C speed					400	kHz
ADC Parameter						
VDD	ADC power supply range			3.16		V
N	ADC accuracy			12		bit

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

Electrical Characteristics(continued)

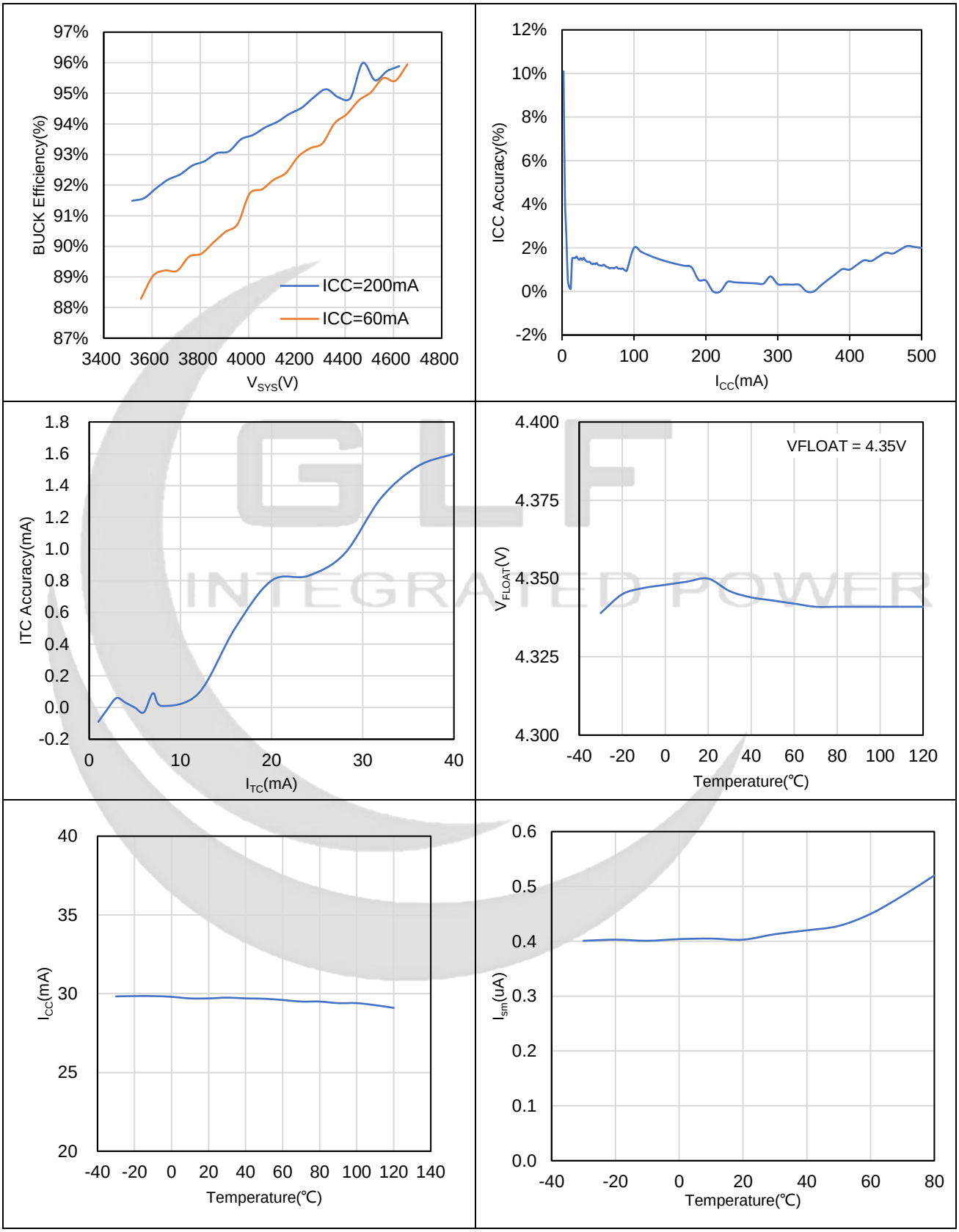
V_{IN}=5V, V_{BAT}=3.85V, T_a=25℃ for typical values (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Channel	ADC channel			5		
V_{MEAS}	Range of VIN for measurement		3		6	V
	Range of VBAT for measurement		0		4.55	V
	Range of IBAT charging current for measurement		2		600	mA
	Range of IVIN for measurement		2		1000	mA
	Range of NTC voltage for measurement	V_{BAT}=2.6V	0		1.5	V

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

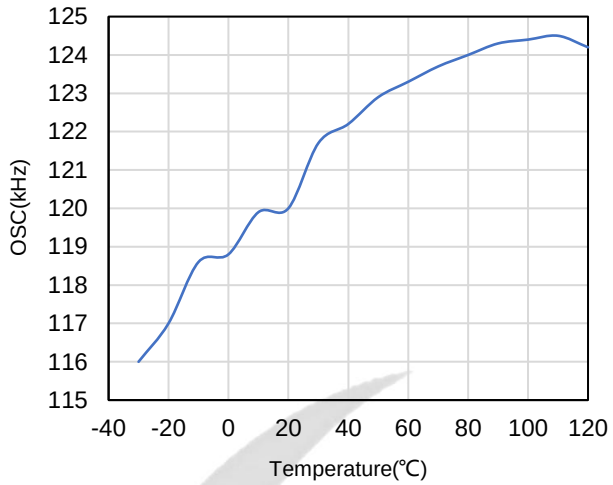
6.6 Typical Characteristics

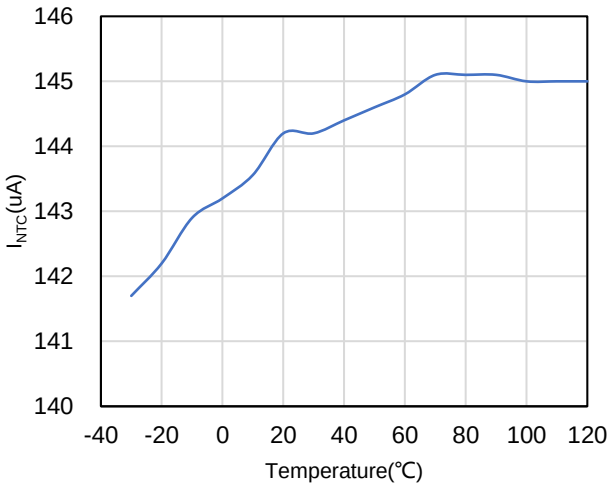
V_{IN}=5V，V_{BAT}=3.7V，T_a=25℃

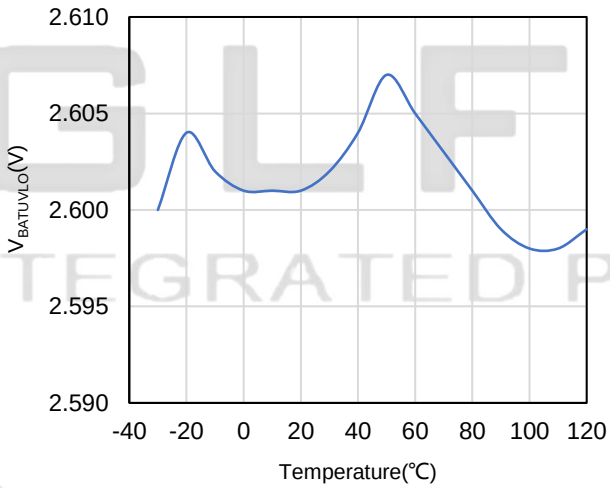


Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

Typical Characteristics(continued)







Copyright © 2023 GLF Integrated Power. All Rights Reserved.

7 Functional Description

7.1 Block Diagram

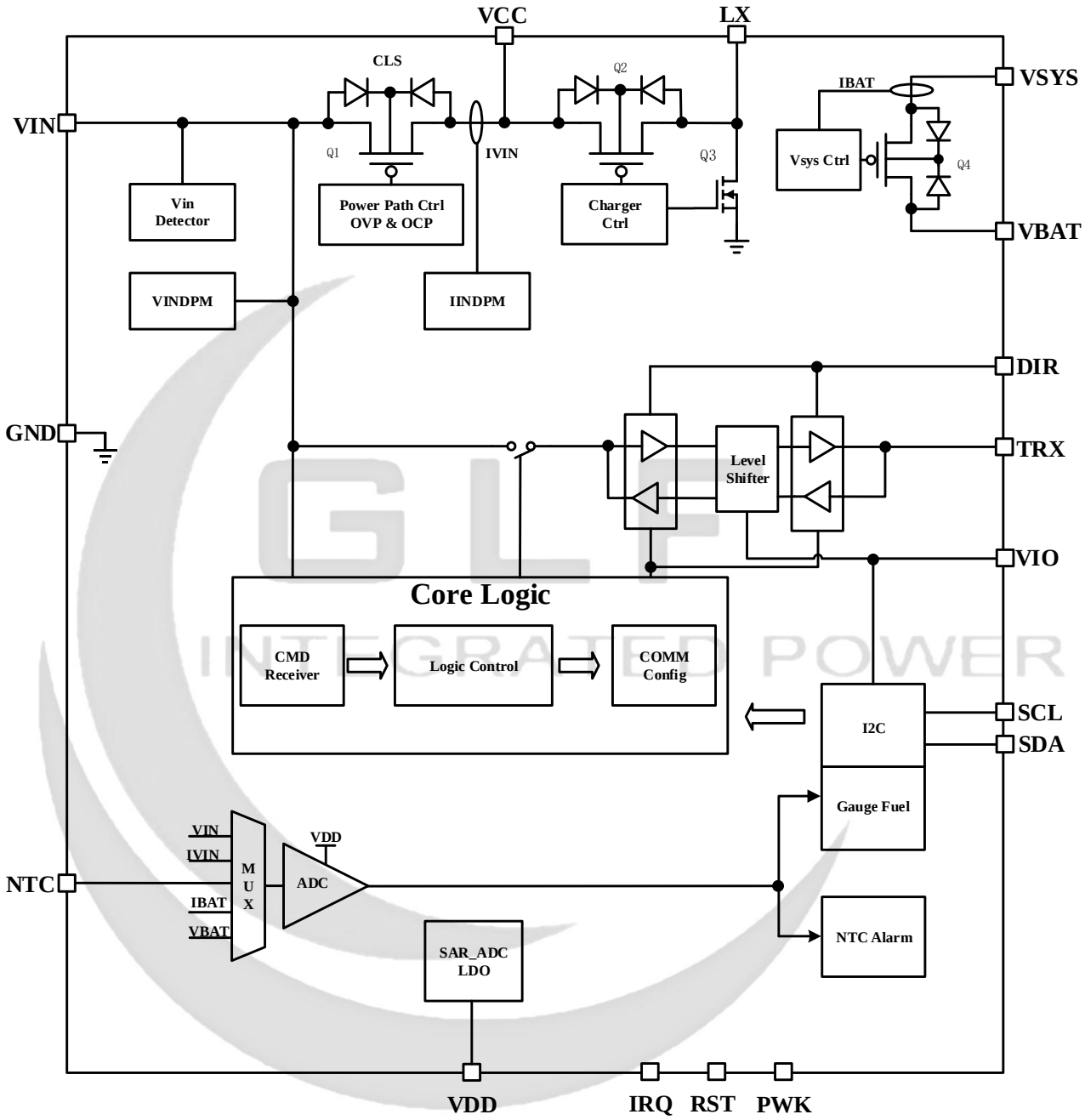


Figure 7-1. Block Diagram

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

7.2 Input Protection

VIN is for charging and communication, and VIN capacitor is not needed. VCC is generated after VIN passes through Q1, which is used as the charging input of GLF70602 and an external capacitor is required. The VIN terminal has OVP, OCP and under voltage protection (UVP). Q1 will shut down instantly to protect the system whenever it triggers OVP, OCP or UVP.

GLF70602 will automatically turn off Q1 when entering the communication mode to prevent the capacitance on VCC from affecting the communication rate.

7.3 Charger Mode

GLF70602 combines two charge mode: (1) DCDC charge i.e. BUCK+NVDC; (2) Linear-Bypass-Mode charge (LBMC) i.e. BUCK bypass + NVDC.

7.3.1 Switch Charge Mode

GLF70602 adopts the BUCK+NVDC mode by default, as shown in Figure7-2. Q1 is high-voltage mosfet., used for communication isolation. Q2, Q3 and Charger Ctrl forms a complete BUCK Converter. LX is connected to VSYS through an inductor. Q4 is the BFET, constructs the NVDC structure with the combination of Vsys Ctrl block. The efficiency of this system could be higher than 93% when setting IBAT charging current=500mA, VIN as input and VBAT as output, which meets most of small capacity battery efficiency requirements.

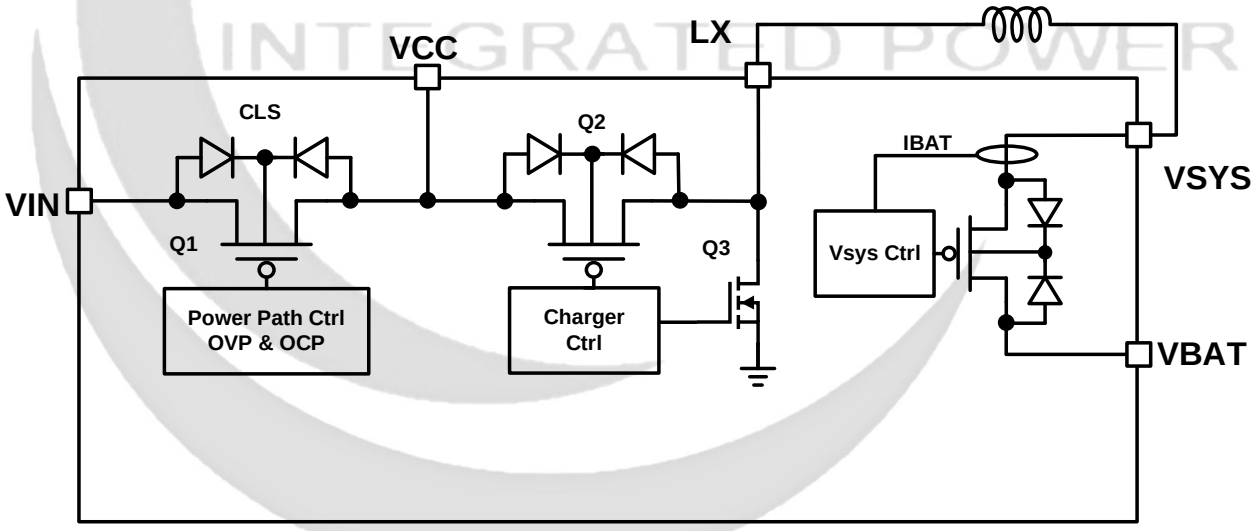


Figure 7-2. BUCK + NVDC Internal Diagram

Specially, the BUCK of GLF70602 is implemented with ACOT controlling structure. This structure benefits the dynamic output response, which satisfies greatly the current spike and fast changing property of earbud system. Even when VIN is close to VBAT, GLF70602 can still be charging. Ideally, the duty ratio of BUCK can reach near 100%, so in other word, GLF70602 can charge with a low VIN input in order to optimize the charging efficiency of the whole system.

7.3.2 Linear-Bypass-Mode

GLF70602 can be configured as a linear charger (LBMC), as shown in Figure7-3. Q1 is the high-voltage mosfet, used for communication isolation. VCC is connected with VSYS directly via PCB layout (which

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

means the DCDC BUCK is disable). Q4 is the BFET, constructs the NVDC structure with the combination of Vsys Ctrl block.

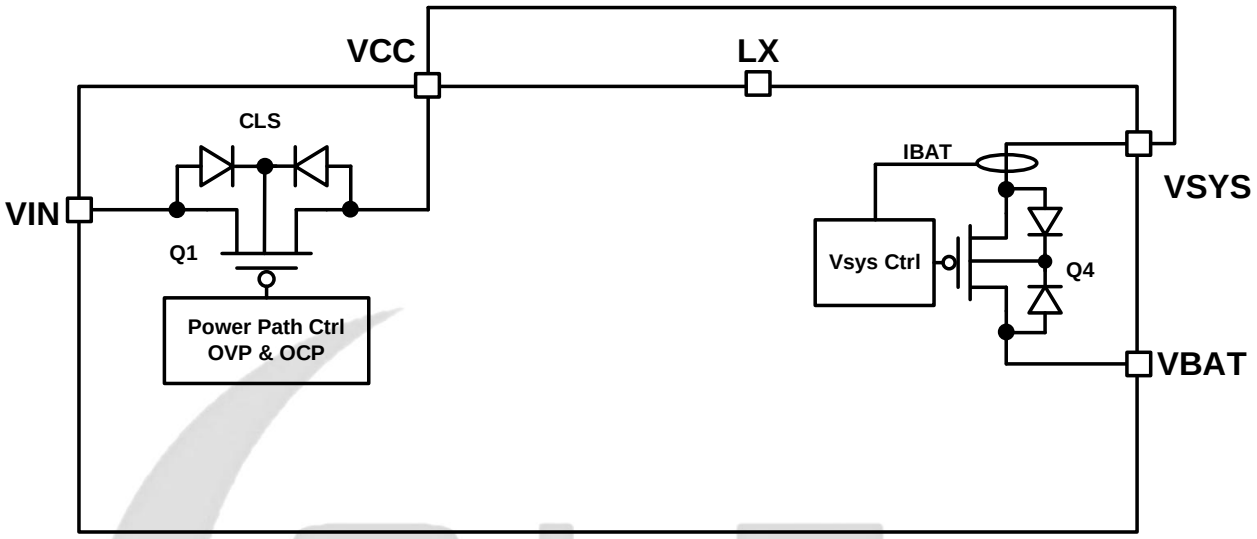


Figure 7-3. BUCK bypass + NVDC Diagram

The LBMC mode of GLF70602 can meet some special applications' requirement. Ideally, the efficiency of charging can be as high as 97% when the voltage difference of VIN and VBAT is lower 50mV.

7.4 Charging Process

GLF70602 integrates the full process of charging management, 3 stage totally: trickle current charge (TC), constant current charge (CC), constant voltage charge (CV), as shown in Figure7-4.

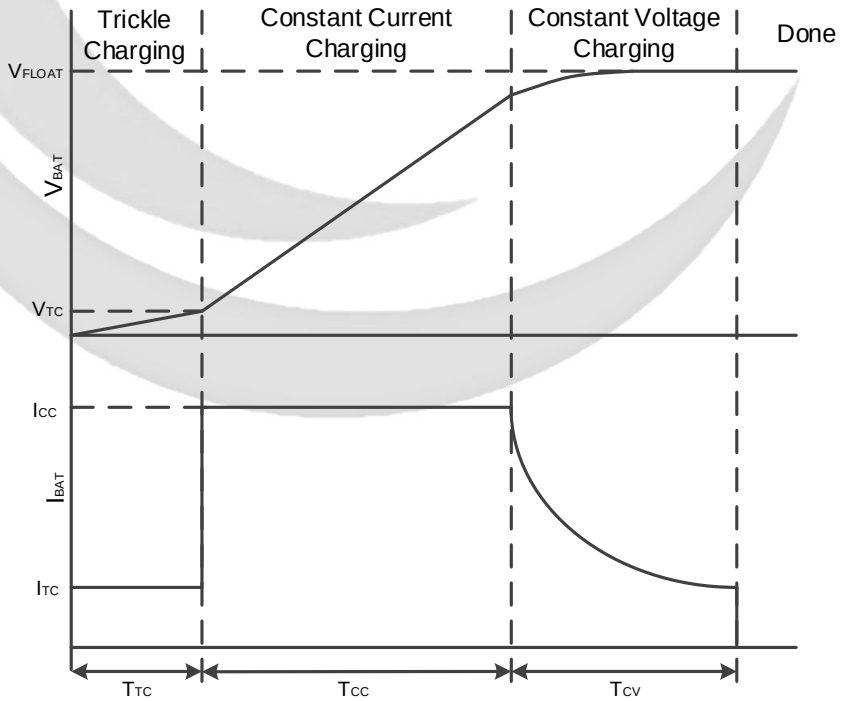


Figure 7-4. Charging Process Diagram

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

7.4.1 Switch Charge Process

For DCDC charge mode i.e. BUCK+NVDC, GLF70602 is in charging state and the output voltage of VSYS is:

(1) If VBAT<VSYS_MIN-100mV, BFET works as LDO, VSYS=VSYS_MIN.

(2) If VBAT≥VSYS_MIN-100mV, BFET works as LDO, VSYS=VBAT+100mV.

(3) If VBAT is fully charged, remain VSYS=VBAT+100mV.

In order to utilize the charging power of VIN and protect the VIN power supply, meanwhile, GLF70602 integrates the VCCDPM and IINDPM function:

(1) If VIN power supply can provide sufficient driving ability (for example lower output impedance), once VIN input current reaches the IINDPM threshold, GLF70602 will limit the BFET charging current. Meanwhile, if current consumption of VSYS keeps going high, BFET will further reduce the charging current to 0 mA in order to deliver full power to VSYS loading. Ultimately, if VSYS loading keeps going higher, GLF70602 will trigger DCDC BUCK peak current protection or VINOCP.

(2) If VIN power supply cannot provide driving ability (for example large output impedance), the voltage of VIN pin (or VCC) will fall down, when the current consumption of VSYS loading increases. Once the voltage of VCC reaches VCCDPM, BFET will limit the charging current to maintain VCC=VCCDPM and ensure VSYS functioning.

(3) VCCDPM = MAX (VINUV, VBAT) + DeltaVCCDPM, in other word, when VBAT is charged to a higher voltage, VCCDPM also increase.

The ACOT BUCK structure in GLF70602 also provides a new function called ‘Pass Through Mode’, which can enhance the charging efficiency, stabilize the output and lower the switching loss. When VCC-VBAT<400mV, GLF70602 enters the ‘Pass Through Mode’, which means the BUCK high side PMOS keeps always ON and low side NMOS keeps always OFF. VCC will be directly connected with VSYS to ensure the driving ability of output. When VCC-VBAT>550mV, BUCK will restart.

The charging current can be configured by setting register during trickle charge state; while in constant charging state, GLF70602 uses DCDC switching charging mode and the charging current is also configurable, ranges from 2mA~500mA; finally, during constant voltage stage, the charging current decreases gradually. When the charging current decreases to the charging cut-off current ITERM, GLF70602 stops charging, ChargeEnd=1.

7.4.2 Linear Charge Process

For NVDC only linear charger, when GLF70602 is working in charging stage, we have:

(1) If VBAT< VTRIKL (3.0V), GLF70602 conducts trickle charging, BFET works in LDO mode.

(2) If VBAT≥VTRIKL (3.0V), GLF70602 works in constant current (ICC) charging mode and BFET works in LDO mode.

7.5 ChargeEnd Mode

After VBAT is fully charged, the state of VCC, BUCK would be configured.

If VccOnAsChgEnd=0, when StChip[2:0] = ChargeEnd mode, VCC is shut down automatically.

If VccOnAsChgEnd=1, when StChip[2:0] = ChargeEnd mode, VCC and BUCK keep on.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

7.6 Charging Protection

Multiple protection is also included during charging state: Charging overtime protection, Over temperature protection (OTP).

The charging timeout protection is divided into two stages: (1) If the duration time of TC stage exceeds 1 hour, GLF70602 will stop charging automatically; (2) if the duration time of CC/CV stage exceeds 3 hours, GLF70602 will also stop charging automatically. This charging overtime protection function is default off and could be turn on.

If the junction temperature of power management path is over 110 degrees, the charging current will decrease automatically. This function can utilize GLF70602 power delivering ability while preventing not only internal but also external devices from overheat damaging.

7.7 Recharge

GLF70602 integrates the auto recharge function and active recharge request function.

Automatic recharging: When VIN is 5V constantly existing and VBAT is full of charge, GLF70602 enters ChargeEnd mode, and the charging current drops to 0. Due to the internal resistance of the battery and its own chemical characteristics, VBAT will slowly decrease. When VBAT drops to VRECHG voltage. GLF70602 will restart the charging module and recharge the battery.

Active Recharge Request (ARR): Active Deposit Request (ARR): This feature needs to be used with other GLF products. It is not described in detail here.

7.8 BFET Charging/Discharging

BFET is equipped with battery discharging path management function. The VBAT of GLF70602 generates VSYS through BFET to supply power to the earbud system. Also, the earbud system can shut down BFET by I2C controlling thus achieving earbud system power down, lowering power consumption and enter ship-mode.

BFET has over discharging current protection (OCP). When current of BFET exceeds IBAT_OC, BFET enters current limitation protection mode and regulate the discharging current to IBAT_OC. However, if VSYS<VBAT-0.7V, BFET enters VSYS short circuit protection mode: hiccup for every 2 seconds until VSYS exits short circuit state, BFET will turn on again.

BFET also has over discharged protection function, whenever in charging or discharging status, if VBAT<VBATOD, BFET exit discharging status.

The charging function can be turn on or off flexibly by configuring EN_CHG register:
(1) If VIN is ready and stable, BFET charging function is turn on automatically.
(2) If VIN < VINUV, BFET charging function is turn off automatically.

When GLF70602 is under standby status, once VINCMD(0x22) has been received, or register <0x5A> = 0x3 is written, GLF70602 will shut down BFET and enter shipmode. To exit the ship-mode state, VIN=5V is needed to plug in and last for at least 32mS, or GLF70602 receives the VINCMD(0x23).

7.9 NTC Monitoring

GLF70602 provide an integrated 12-bit SAR ADC to monitor the temperature by sampling the voltage of

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

NTC pin. The voltage of NTC pin will be sent to the Gas Fuel and NTC temperature comparison module.

The schematic of the NTC temperature comparison module is shown in Figure 7-5.

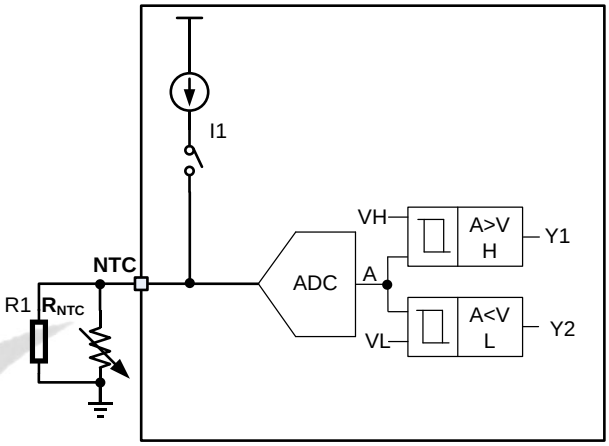


Figure 7-5. Diagram of The NTC Temperature Comparator

The ADC samples the voltage of NTC pin and then compares the result A of sampling with the register values VH and VL. If A>VH or A<VL, GLF70602 will sent IRQ pulse and change the status in register NTC_STAT [1:0].

Suppose that -10℃ corresponds to 1600mV, 0℃ to 1400mV, 15℃ to 800mV, and set VH=1400mV, VL=800mV, then when A>VH, it means NTC temperature is less 0℃. At this point, if it is necessary to detect whether NTC temperature is lower than -10℃, the VH should be reset to 1600mV. VL is set up and so on. The hysteresis of the VH and VL of the NTC temperature can be configured.

If current temperature exceeds threshold, the NTC temperature protection will only alert the user via sent IRQ pulse and will not trigger any protection mechanism. User need to perform corresponding protection based on the NTC status.

The NTC resistor needs to be placed away from the GLF70602 to avoid the heating of GLF70602 itself affecting the detection of NTC resistor. The recommend NTC resistance parameters are 10KΩ and β = 3380K.

7.10 Communication

GLF70602 has a bi-directional communication channel (referred to as the COMM channel), which provides a one-wire communication interface between master MCU and local MCU.

The COMM channel can be enabled in two ways:

(1) VIN receives the private command “COMM ON” to turn on the COMM channel.

(2) Enable the COMM channel through the I2C communication to set “COMM ON”.

The COMM channel can be diable the COMM channel:

(1) Turn off the COMM channel after VIN receives the private command “COMM OFF”.

(2) Disable the COMM channel through the I2C communication to set “COMM OFF”.

(3) circuit short in VSYS.

(4) Comm Time-out.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

(5) Enter shipmode.
(6) Both VIN and VBAT are undervoltage.

When the CommTimeOut is enable, it can be clear to extend the duration of COMMON. Ways to clear CommTimeOut: (1) Write <CommTimeOutClrIdle>=0xAA.(2) VIN or TRX pin toggle (or VIN=1, register optional).(3) ACK_Busy=1.

There are three mode for bidirectional communication, which need to be configured by registers: (1) AutoDIR.(2) IODIR.(3) RegDIR.

AutoDIR mode is only applicable to the non-charging state. When VIN=5V, AutoDIR will be automatically disable. IODIR and RegDIR are applicable to charging and non-charging states.

7.10.1 AutoDIR Mode

When the communication mode is set to AutoDIR for VIN and TRX pins, the pull-up and pull-down resistance of both VIN and TRX pins is 4K. The pull-up and pull-down resistance of MCU input IO pin must be greater than 20K.The pull-up and pull-down resistance of MCU output IO pin must be less than 1K.

For earbud system, the charging case can enable and disable COMM channel by sending a VINCMD command through VIN pin. When the COMM channel is enable, Casein/Caseout function is disable. Therefore it needs to set the register by I2C to enable the timeout mechanism when charging case communicates with the earbud MCU. If the VIN and TRX pin do not detect the flip-flop within a certain time (e.g. 16ms, 50ms) and no data is written to the ACK_DATA register, the CommTimeOut_OV timeout flag will be set to 1, and the device will disable the COMM channel. If the GLF70602 has enabled the Case-in detection function, the Case-in detection function will be enable again after the COMM channel is disable.

7.10.2 IODIR Mode

When the communication mode is configured as IODIR, earbud MCU needs to pull-up/pull-down DIR pin to control data transmission direction. When DIR=0, communication data is transferred from VIN to TRX; When DIR=1, communication data is transferred from TRX to VIN.

When the communication mode is set to RegDIR, earbud MCU needs to set register CommDirCtrlMode =0/1 to control the transmission direction of data. When CommDirCtrlMode =0, communication data is transmitted from VIN to TRX. When CommDirCtrlMode =1, communication data is transmitted from TRX to VIN.

With the COMM channel enabled and the device in IODIR mode, if VINOK=1, VCC can be enabled or disabled to adapt to different applications.

When VINOK=1 and the COMM channel is enabled, CommTimeOut will be forcibly enabled. When CommTimeOut occurs, the COMM channel is disabled.

7.10.3 ACK_DATA Mode

GLF70602 can also send data from the ACK_DATA register to VIN. When the sending data source is selected as ACK_DATA, i.e. Comm_DataSrc=0, the DIR pin no longer controls the direction of data transmission, and the TRX pin switches to the high resistance state. In this case, VIN pin defaults to input and continuously detects the data sent from the master MCU. When the VIN pin detects VINCMD, GLF70602 saves the data in the VINCMD_RX register. When the user needs to send the VINCMD to VIN,

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

it needs to detect ACK_BUSY=0 before writing to ACK_DATA register via I2C to start sending ACK_DATA data.

7.11 VIO power supply

For bi-directional communication, the power supply of TRX, DIR, SDA, SCL and IRQ pins is provided by VIO, which is connected to the IO power pin of the Bluetooth master, in order to achieve power supply matching of communication.

When the VIO undervoltage lasts for 100ms, GLF70602 will automatically turn off the TRX module, then the TRX pin and DIR pin switch to high resistance state. At this time, the VIN receive function remains normal, and the ACK_DATA transmit function also remains normal. Local MCU can still communicate with the master MCU through ACK_DATA and VINCMD_RX registers. This function is applicable to "send data in the form of current" communication when "VIN is normal but VBATOD=1".

7.12 CaseIn/CaseOut Status Detection

The casein/caseout status detection is shown in Figure 7-6..

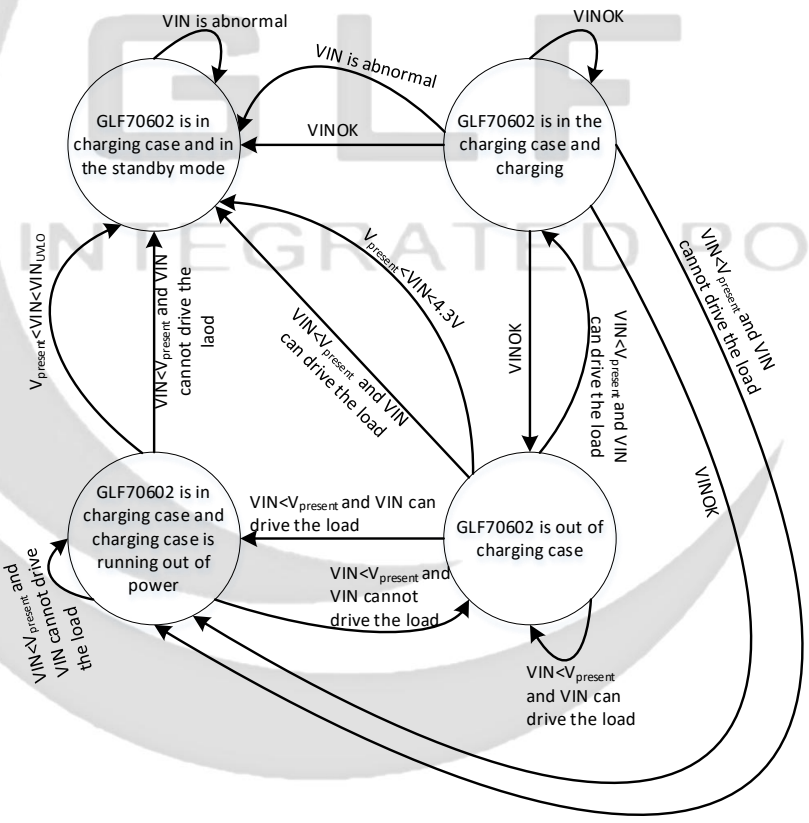


Figure 7-6. CaseIn/CaseOut Status Detection

GLF70602 integrates a built-in function of casein/caseout detection, it can detect whether the local system is in case or not in real time, and whether the case is lowpower or not, and the detection results will be saved in the register.

When GLF70602 is in shipmode , the casein/caseout detection function will be turned off and register <0x30>.CaseStat will reset. After the device is out of shipmode, the Casein/Caseout detection will be restored.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

7.13 RST and PWK Output

The RST pin of the GLF70602 is connected to the reset pin of the earbud MCU to reset MCU. The PWK pin of the GLF70602 is connected to the POWERKEY (multi-function key) of the earbud MCU to wake up and notify the MCU.

RST and PWK pins are both open-drain output. The I2C can be configured as active low or active, which should be connected with pull-up/pull-down resistance when using. The active time of RST and PWK can be set through the I2C register. For RST, GLF70602 can be configured to send RST signal to the earbud MCU after a certain delay time after detecting casein. For PWK, the GLF70602 can be configured to send a PWK signal to the earbud MCU after detecting caseout.

The master MCU can control the GLF70602 to send RST and PWK signals through private commands, where RST can be configured through registers for effective voltage and duration, and PWK can be configured through registers for click, double click, triple click, long press, super long press, etc. Refer to the Private Commands section for specific commands.

7.14 VINCMD

The GLF70602 has a built-in private instruction receiving module (VINCMD) at the VIN pin, which is used to receive control instructions from the master MCU, and the received private instructions will be saved in the register VINCMD_RX for users to read.When the GLF70602 receives any VINCMD that meets the private instruction format, it can generate an IRQ to notify the local MCU and return ACK_DATA to the master MCU. The VINCMD module decodes it in real time and immediately performs the function of the corresponding module.

The VINCMD set retains 11 system instructions for its own state control, as shown in Table 1. These 11 instructions, including reset VSYS instruction, enter/exit shipmode instruction, enable/disable COMM channel instruction, RST control instruction, and PWK control instruction. When the GLF70602 is in the standby state, the COMM channel can be enabled by local MCU to actively communicate with the master MCU.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

Table 1. VINCMD

Instruction	Command	Function
0x20	Reserve	-
0x21	Restart	Turn off VCC, BUCK, and BFEF, and then restore VCC, BUCK, and BFET after 200ms.
0x22	Ship Mode ON	When GLF70602 is in Standby mode, it responds to this command, turns off BFET and enters ship mode. (1) The GLF70602 can receive “COMM ON” command and turn on COMM channel after receiving the Ship Mode ON command until it enters the shipmode state, but after the 100ms/4s delay, it will still enter the shipmode state. (2) When GLF70602 is in shipmode state, it can only respond to Ship Mode OFF command, and other commands will not be responded. (3) After entering shipmode, it will force to pull down VSYS for 200ms, and it cannot be interrupted. If a “shipmode off” command is received during the VSYS pull-down period, the VSYS pull-down will end immediately and the shipmode will be exited.
0x23	Ship Mode OFF	Exit ship mode .When the device is in shipmode, it only responds to “shipmode off” command.
0x24	COMM ON	When the COMM channel is turned on, GLF70602 can only respond to “COMM OFF” command and “Ship Mode ON” command. It must wait until the VSYS pull-down of “shipmode on” command is finished before it can turn on COMM, i.e., after receiving the “shipmode on” command via I2C/VINCMD, it needs to wait for the 200ms of pull-down VSYS, and then receive the “shipmode off” command before it can turn on VSYS.
0x25	COMM OFF	Disable the COMM channel.
0x26	RST	Trigger RST signal output, the parameters of the time and valid level are set by registers.
0x27	PWK SHORT	Trigger PWK to output single short waveform, the parameters of the time and valid level are set by registers.
0x28	PWK DOUBLE	Trigger PWK to output double clicks waveform, the parameters of the time and valid level are set by registers.
0x29	PWK TRIPLE	Trigger PWK to output triple clicks waveform, the parameters of the time and valid level are set by registers.
0x2A	PWK LONG	Trigger PWK to output long-press waveform, the parameters of the time and valid level are set by registers.
0x2B	PWK LONGLONG	Trigger PWK to output long long-press waveform, the parameters of the time and valid level are set by registers.
0x2C~0x2F	Reserve	-

Remarks:

(1) During the execution of the PWK SHORT/DOUBLE/TRIPLE/LONG/LONGLONG instruction, it will not respond to other PWK instructions, but:

a. If a COMM command is received, the PWK command will be stopped, the PWK module will be reset, GLF70602 will

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

respond to this COMM command and enable the COMM channel.

b. If the “ShipMode On” command is received, it will enter shipmode state and stop the PWK instruction and reset the PWK module after a delay (100ms/4s).

c. If the “Restart” instruction is received, it will reset VSYS and stop the PWK instruction and reset the PWK module.

(2) If the “COMM”, “ShipMode On”, or “Restart” instruction is received during the execution of RST instruction, it will be handled in the same way as the PWK instruction. When GLF70602 detects casein, but after a moment later GLF70602 is caseout again before RST module response, GLF70602 will terminate the RST waveform and reset the RST module.

7.14.1 Physical Layer of VINCMD

The signals of physical layer mainly consist of S, SYNC, BIT1, BIT0, and STOP. Each signal includes a certain of unit time T, as shown in Table 2.

Table 2. Physical Layer Timing Parameters

Signal	High Level Time(T)	Low Level Time(T)
S	1	-
SYNC	1	16
BIT1	3	1
BIT0	1	3
STOP	8	0

The time accuracy of T for private commands sent from the master MCU is required to be ±20%, if it exceeds this range, GLF70602 will receive an error instruction. To make master MCU flexible and convenient, GLF70602 defines four types of unit time T as shown in Table 3, and register <0x50>.

Table 3. Duration Selection of T

<0x1C>.CMD_T[1:0]	Duration of T	Packet duration
0	100uS	6.1mS
1	200uS	12.2mS
2	400uS	24.4mS
3	1mS	61mS

When sending private instructions, firstly sending the code “S”, secondly sending the code of “SYNC”, thirdly sending the data bits, and lastly sending the code of “STOP”, as shown in Figure7-7.

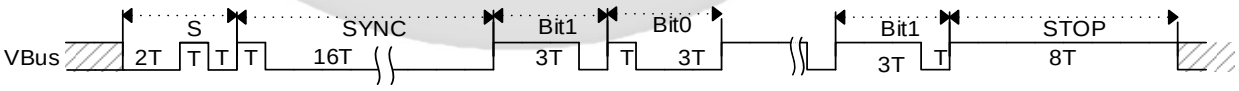


Figure 7-7. Physical layer protocol

The code “S” is used to wake up the sleep GLF70602, composing of at least a high level pulse lasts 1T and a low level pulse lasts 1T.

The code “SYNC” consists of a high level pulse lasts 1T and a low level pulse lasts 16T, which is used to synchronize the clock of cradle and GLF70602.

“BIT 1” consists of a high level pulse lasts 3T and a low level pulse lasts 1T.

“BIT 0” consists of a high level pulse lasts 1T and a low level pulse lasts 3T.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

The code “STOP” consists of at least a high level pulse lasts 8T.

7.14.2 Protocol Layer of VINCMD

After the code “SYNC”, follow the high 4-bits feature code of “0010”, and the low 4-bits are used to transmit instructions, as shown in Figure7-8.

Figure 7-8. Protocol Layer

7.15 Gas Fuel

GLF70602 measures the cell voltage, current, and temperature to determine battery SOC. The accuracy of Gas Fuel is as high as ±5%.

The gauge can work in two mode which require configuration by the master.

(1) Normal mode. The Gas Fuel is running at full speed. When the device is in the charging state, The Gas Fuel is automatically set to Normal mode. When the device is charging, the Gas Fuel is automatically set to Normal mode. When the device is not charged and the earbud MCU works normally, the earbud MCU needs to set the Gas Fuel to Normal mode (for example, when the Bluetooth wakes up from sleep mode).

(2) Sleep mode. The Gas Fuel work in low power mode. When the device is not charging and the earbud master is going to sleep, the Bluetooth master needs to set the Gas Fuel work from to Normal mode to Sleep mode to reduce power consumption. When the device enters shipmode and VSYS is turned off, the Gas Fuel automatically turns off.

The Gas Fuel needs to be calibrated before to be used. The calibration parameters can be written through I2C.

The Gas Fuel can not be reset by Watchdog and abnormal status. The device will always calculate the remaining capacity as long as the Gas Fuel is enabled and the battery voltage is normal and not shipmode. When the Gas Fuel is enable, the ADC should also be enabled at the same time, otherwise the Gas Fuel will work abnormally.

7.16 ADC

GLF70602 provide an integrated 12-bit SAR-ADC to monitor VIN, VBAT, NTC, IVIN, and IBAT. Each channel of the ADC can be configured with auto continuous conversion mode and single conversion mode. The conversion result will update to registers.

Since the ADC conversion result is 12bit, and I2C accesses the ADC conversion result in Byte, it is recommended to read two bytes at one time in a continuous reading mode. For example, the high 8 bits and low 4 bits of VBATADCVal are read in a continuous reading mode, which can ensure that the two bytes of data are the result of the same conversion cycles.

7.16.1 AutoMode

When the ADC is configured as AutoMode, the device will automatically turn on the ADC at intervals for analog-to-digital conversion of the corresponding input signal. The interval conversion time can be configured in the register of Gas Fuel. By default, ADC conversion is performed in 2s interval in the order of VBAT, NTC, IBAT, VIN, IVIN. When a channel conversion is completed, the EOC (end of conversion)

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

flag will be set to 1 and the conversion result will be save in the corresponding channel register.

The method of enable AutoMode as follow:

(1) Set ADCEN = 1 and ADCAutoModeStartup = 1.

(2) Set the corresponding channel in register <0x45> as AutoMode.

7.16.2 SingleMode

When the ADC is configured as SingleMode, the user needs to manually turn on the ADC. Each time it is started, the ADC is immediately converted once. When this conversion is completed, the EOC (end of conversion) flag will be set to 1 and the conversion result will be save in the corresponding channel register.

The method of enable SingleMode as follow:

(1) Set ADCEN=1 and ADCAutoModeStartup=0.

(2) ConFigthe SingleChxSel in register <0x45> as the corresponding ADC channel.

(3) Set register <0x5A>.I2C_CMD=0x2.

7.17 Watchdog

GLF70602 contains a watchdog timer. The Watchdog timer is disabled by default and can be set by register. When the watchdog expires, the register will be reset to the default values.

The Gas Fuel and ADC are not reset when the watchdog timer expires.

7.18 IRQ

IRQ pulse can be set to 7.5ms and 2s. The interrupt is only used to wake up the local MCU, or to alert the local MCU. Upon receiving the interrupt pulse, the local MCU may read the flag registers to determine the event that caused the interrupt, and for each flagged event, read the corresponding status registers to determine the current state.

IRQ interrupt events are shown in Table 4. All other interrupt events except ChargeEnd can be disable and enable.Users can choose wether to mask corresponding interrupt events as required.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

Table 4. Lists of The Interrupt Events

No.	Interrupt Events	IRQ can be masked	IRQ default status	Description
1	VIN_OVP	Y	ON	IRQ events are merged, but the state is differentiated. When VIN status changes, an IRQ pulse (VIN_STAT_IRQ) is sent.
2	VIN_OK			
3	VIN_UVLO			
4	VCC_OCP	Y	ON	VCC_OCP_IRQ.
5	ITC Timeout	Y	ON	IRQ events are merged, but the state is differentiated. When the charge timeout occurs, an IRQ pulse (CHG_TimeOut_IRQ) is sent.
6	FC Timeout			
7	CHIP OTP	Y	ON	When over temperature protection occurs, an IRQ pulse (CHIP_OTP_IRQ) is sent.
8	Case in / Case out	Y	ON	CaseSTAT_IRQ
9	Init_OK	Y	ON	Init_OK_IRQ
10	VBAT Recharge	Y	ON	ReChg_IRQ
11	NTC status changes	Y	ON	NTC_IRQ
12	ChargeEnd	N	ON	Interrupt of charge end. Can not be masked.
13	ADC end of single converter	Y	ON	IRQ events are merged, but the state is differentiated.
14	ADC end of auto converter	Y	ON	
15	ACK_DATA	Y	ON	Interrupt after sending ACK_DATA
16	VINCMD RX	Y	ON	Interrupt after receiving VINCMD.
17	Every 1% change in battery power when charging or discharging	Y	ON	1%SOC
18	100% battery power when charging	Y	ON	100%SOC
19	0% battery power when discharged	Y	ON	0%SOC
20	Battery low voltage alarm	Y	ON	LowSOC
21	CRC32	Y	ON	Cyclic Redundancy Check
22	INT_SHT	Y	ON	Inductor short circuit
23	VCCDPM	Y	ON	VCC voltage regulation
24	IINDPM	Y	ON	Input current regulation
25	SysStat	Y	ON	st_chip status changes
26	CommTimeOut	Y	ON	CommTimeOut

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

7.19 I2C Interface

GLF70602 integrates a standard I2C slave interface, which supports continuous read and write. The communication rate supports standard 100 kHz and fast mode 400 kHz. The Slave address of the chip is 0x68, the write address 0xD0 and read address 0xD1. The power supply of I2C is VIO, the earbud MCU can choose the appropriate VIO power supply, so that the GLF70602 and the earbud MCU can match the communication voltage level.

GLF70602 supports single-byte write operations, as well as multi-byte continuous write operations. The timing diagram of single-byte and multi-byte write operation is shown in Figure7-9 and Figure7-10 .

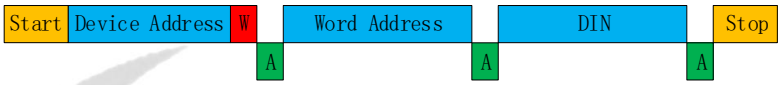


Figure 7-9. I2C Single Byte Write Operation

Figure 7-10. I2C Multi-byte Continuous Write Operation

GLF70602 supports single-byte and multi-byte read operations. The sequence diagram is shown in Figure7-11 and Figure7-12.

Figure 7-11. I2C Single Byte Read Operation

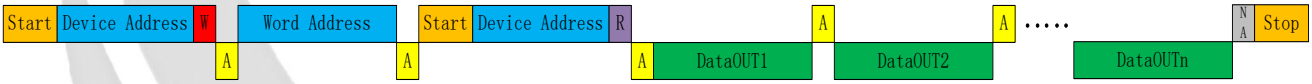


Figure 7-12. I2C Multi-byte Continuous Read Operation

Table 5. I2C Electric Characteristics

Symbol	Parameters	Min	Max	Unit
F_{scl}	Clock Frequency of SCL	-	400	kHz
$T_{HD,STA}$	Hold time of the initial condition	0.6	-	μS
T_{LOW}	Low level time of SCL	1.3	-	μS
T_{HIGH}	High level time of SCL	0.6	-	μS
$T_{SU,STA}$	Setup time of the repeated initial condition	0.6	-	μS
$T_{HD,DATA}$	Data hold time	0.6	-	μS
$T_{SU,DATA}$	Data setup time	100	-	nS
T_R	Rise time of the signals of SDA and SCL	-	300	nS
T_F	Fall time of the signals of SDA and SCL	-	300	nS
$T_{SU,STO}$	Hold time of the stop condition	0.6	-	μS
T_{BUF}	Bus idle time between the stop and initial condition	1.3	-	μS
C_B	Capacitive load of each bus line	-	400	pF

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

8 Register Summary

8.1 Register List

Table 6 shows the codes that are used for access types in this section.

Table 6. I2C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WC	WC	Write 1 then Clear

Register types include status registers and configuration registers. Write <0x72> = 0x97 and <0x73> = 0x39, then registers <0x1A> can be written.Write <0x72> = 0x97, then registers <0x1B>~<0x1F> can be written.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x1A>EnChg_Drop_BuckByp

Addr	Type	Field	Name	Reset	Description
0x1A	R/WP/F	7:4	reserved	-	Prohibit modification
		3	I2C_Watchdog	0	The enable control bit of I2C Watchdog, it is used to reset I2C and release SDA pin when SDA is pulled down to 0 for more than 1s in case of I2C communication error 0: Disable I2C Watchdog 1: Enable I2C Watchdog
		2	SetEnChgAsVINOK	0	EN_CHG=1 is automatically configured after VINOK from 0 to 1 0: Disable 1: Enable
		1	RstEnChgAsVINUV	0	VIN power down will reset EN_CHG. 0: Disable. 1: Enable. When it is detected that the VIN changes from VINOK=1 to VINUV=1 , it will make EN_CHG=0.
		0	Buck_Bypass_Sel	0	0: DCDC BUCK enable 1: Linear Bypass Mode enable

Reset by POR, SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x1B>Wdg_VINCHG

Addr	Type	Field	Name	Reset	Description
0x1B	R/W/F	7	SetWdgAsVINOK	0	Watchdog=1 is automatically configured after VINOK=1 0: Disable 1: Enable
		6:5	Watchdog	00	The configuration of watchdog: 00: 40S 01: 80S 10: 160S 11: 160S
		4	EnWdg	0	enable watchdog: 0: Disable 1: Enable
		3	DIS_IND_SHT	0	Enable register of "inductive short circuit detection function" of BUCK module: 0: Enable 1: Disable
		2	VCCLDOBypass	1	Voltage mode of VIN to VCC: 0: VIN to VCC is LDO output, and LDO=5.3V 1: VIN pass through VCC
		1	VIN_OVP_Sel	0	VIN OVP 0: 6.0V 1: 6.8V
		0	EN_CHG	0	Charging enable of BFET 0: Disable BFET charging 1: Enable BFET charging

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x1C>T_DPM

Addr	Type	Field	Name	Reset	Description
0x1C	R/W/F	7:6	CMD_T[1:0]	00	Unit T of receiving instructions： 00: 100uS 01: 200uS 10: 400uS 11: 1mS
		5:4	DeltaVCCDPM[1:0]	00	VCCDPM = DeltaVCCDPM + MAX(VIN_UVLO,VBAT) 00: 300mV 01: 200mV 10: 100mV 11: 60mV
		3	DIS_VCCDPM	0	VCCDPM enable 0: Enable 1: Disable
		2:0	IINDPM[2:0]	000	IINDPM current setting 000: 150mA 001: 200mA 010: 250mA 011: 300mA 100: 350mA 101: 400mA 110: 500mA 111: 800mA

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x1D>VFLOAT

Addr	Type	Field	Name	Reset	Description
0x1D	R/W/F	7:6	-	-	-
		5:0	VFLOAT[5:0]	0x14	VFLOAT , step=12.5mV 0x00: 4.1000V 0x01: 4.1125V …… 0x08: 4.2000V …… 0x14: 4.3500V …… 0x18: 4.4000V …… 0x1C: 4.4500V …… 0x20: 4.5000V …… 0x24~0x3B: 4.5500V 0x3C: 4.000V 0x3D: 4.025V 0x3E: 4.050V 0x3F: 4.075V

Reset by POR ,SoftRst and Watchdog

<0x1E>ICC_IPRE

Addr	Type	Field	Name	Reset	Description
0x1E	R/W/F	7	IPRE	0	Charging current when VBAT<2.0V 0: 3mA 1: 12mA
		6:0	ICC[6:0]	0x0E	ICC current setting 0x00~0x2C: 2mA~90mA, step=2mA 0x2C~0x55: 90mA~500mA, step=10mA

Reset by POR ,SoftRst and Watchdog

<0x1F>ITERM_ITC

Addr	Type	Field	Name	Reset	Description
0x1F	R/W/F	7:4	ITERM[3:0]	0010	ITERM current setting 0000: 1mA 1000: 12mA 0001: 2mA 1001: 16mA 0010: 3mA 1010: 20mA 0011: 4mA 1011: 24mA 0100: 5mA 1100: 28mA 0101: 6mA 1101: 32mA 0110: 7mA 1110: 36mA 0111: 8mA 1111: 40mA
		3:0	ITC[3:0]	0010	ITC current setting 0000: 1mA 1000: 12mA 0001: 2mA 1001: 16mA 0010: 3mA 1010: 20mA 0011: 4mA 1011: 24mA 0100: 5mA 1100: 28mA 0101: 6mA 1101: 32mA 0110: 7mA 1110: 36mA 0111: 8mA 1111: 40mA

Reset by POR, SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x20>UV_MIN_ChgT

Addr	Type	Field	Name	Reset	Description
0x20	R/W	7:6	VIN_UVLO[1:0]	01	VIN UVLO setting 00: 4.40V 01: 4.20V 10: 4.00V 11: 3.80V (1) For Buck mode, the drop threshold of VIN UVLO is VIN_UVLO-200mV。 (2) For Linear Bypass mode charger, the only value of VIN UVLO drop threshold is 3.0V.
		5:4	VSYS_MIN[1:0]	10	VSYS_MIN setting 00: 3.3V 01: 3.3V 10: 3.5V 11: 3.7V
		3	TCTimer	0	Timeout of trickle charging: 0: 1hour 1: 2hour
		2	TCTimerEn	0	Timeout protection function of trickle charging: 0: Disable 1: Enable
		1	FCTimer	0	Timeout of fast charging (CC and CV): 0: 3hour 1: 6hour
		0	FCTimerEn	0	Timeout protection function of fast charging: 0: Disable 1: Enable

Reset by POR, SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x21>FM _VRECH

Addr	Type	Field	Name	Reset	Description
0x21	R/W	7:4	-	-	-
		3	FaultMode	0	VCCOCP/ VSYSOCP protection mode version: 0：Hiccup every 2s 1：VCCOCP/ VSYSOCP protection locked, and unlocked when VIN is inserted
		2:0	Rechg [2:0]	0x0	VBAT recharge voltage: 000：3.90V 001：3.80V 010：3.70V 011：3.55V 100：4.30V 101：4.20V 110：4.10V 111：4.00V (1) When VIN is normal, and ChargerEnd=1, if VBAT drops to Rechg voltage point, Charger will restart charging. (2) When VIN is under voltage and VBAT voltage drops to rechg voltage, "Recharge Request Pulse" will be triggered, VIN will send 100ms low-level pulse, and IRQ will be sent to notify MCU. This function needs to be used together with ReChgVinPdEn.

Reset by POR, SoftRst and Watchdog

<0x22>BATComp

Addr	Type	Field	Name	Reset	Description
0x22	R/W	7:3	BAT_COMP[4:0]	00	Resistance value of BAT internal resistance compensation: 00000: 20mΩ 00001~01000: 40 mΩ~180 mΩ(20 mΩ/step) 01001~10000: 200 mΩ~900 mΩ(100 mΩ/step) xxxxx: 900 mΩ
		2:1	BAT_COMP_TIMER[1:0]	0	Scan time of BAT compensation function: 00: 32mS 01: 64mS 10: 128mS 11: Follow the register Cal_rate
		0	BAT_COMP_EN	0	BAT internal resistance compensation function enable(only VINOK=1): 0: Disable. 1: Enable. When it is enable, <0x46>.bit[1:0]=0x3 must be set, that is, ADCAutoModeStartup=1 and ADCEN=1.

Reset by POR, SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x30>STATE0

Addr	Type	Field	Name	Reset	Description
0x30	R	7	VINOK	0	Status indication of the VINOK： 0: VIN> VIN_{OVP} or VIN<VIN_{UVLO} 1: VIN normal, UVLO<VIN<VIN_{OVP} VINH, VINOK and StChip jointly indicate the current charging state.
		6	INIT_OK	0	Initialization state of the chip after power on: 0: Initialization not completed 1: Initialization completed
		5:4	CaseStat[1:0]	0	Status indication of in cradle and low/out of power of the cradle： 00: Case out 01: Case in and power of master MCU is normal 10: Case in and power of master MCU is low power 11: Undefined
		3	BFET_CHG_STAT	0	Status indication of the BFET： 0：BFET is in charging state, and the current flows from VSYS to VBAT 1：BFET is in discharge state, and the current flows from VBAT to VSYS
		2:0	StChip[2:0]	000	Status indication of the chip: 000: Standby mode 001: Ship mode 010: unCharge mode: VIN normal, not in charge 011: TC Charge mode: TC charging 100: CC Charge mode: CC charging 101: CV Charge mode: CV charging 110: ChargeEnd mode: Full of charge VINH, VINOK and StChip jointly indicate the current charging state. When VINOK=1 and VINH=1, StChip=011~110 of GLF70602 is meaningful.

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x31>STATE1

Addr	Type	Field	Name	Reset	Description
0x31	R	7	VINH	0	VINH, VINOK and StChip jointly indicate the current charging state. 0: When VINOK=0, then VINH=0; when VINOK=1, if VIN<VBAT, then VINH=0. 1: When VINOK=1, if VIN>VBAT, then VINH=1。
		6	IND_SHT	0	In the BUCK mode, the inductive short-circuit protection status indication in the charging state: 0: Normal 1: The inductive short-circuit
		5:4	NTC_STAT[1:0]	00	00: VL≤NTC ≤VH 01: NTC <VL 10: NTC >VH 11: VH and VL configuration error. The register configuration of VH and VL must be VH>VL.
		3:2	TRX_COMM_STAT	00	After the COMM channel is enabled, the state of the COMM channel: 00: COMM channel is enabled and ACK_ DATA as the data source. 01: COMM channel is enabled, and the TRX pin is used as the data source. The direction control is IODIR. 10: COMM channel is enabled, and the TRX pin is used as the data source. The direction control is AutoDIR. 11: COMM channel is enabled, and the TRX pin is used as the data source. The direction control is RegDIR.
		1	ACK_Busy	0	ACK status: 0: No ACK_DATA is being sent. 1: Sending ACK_DATA. At this time, data cannot be written to the ACK_DATA register.
		0	COMM_ON_STA	0	COMM channel status: 0: COMM channel disable 1: COMM channel enable

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x32>STATE2

Addr	Type	Field	Name	Reset	Description
0x32	R	7	-	-	-
		6	DecBusy	0	Receive decoding status of VINCMD: 0: No VINCMD is receiving at VIN port 1: The VIN port is receiving the Data and Stop bits of the VINCMD. DecBusy=1 will be set only when the correct Sync is received.
		5	ShipmodeReady	0	When VINCMD=ShipModeOn or I2CCMD=shipmode is received, GLF70602 enters the shipmodeready state. After the 100ms/4s delay expires, GLF70602 formally enters the shipmode state. After entering shipmode, this status is also cleared. 0: No delay is triggered to enter shipmode 1: Delaying entry into shipmode
		4	-	-	-
		3	IDPM	0	0: VIN power is normal 1: VIN current in IDPM state
		2	VDPM	0	0: VIN power is normal 1: VIN is in VDPM state
		1	FC_TO	0	0: Fast charging stage normal 1: Fast charging stage timeout
		0	TC_TO	0	0: Trickle charging normal 1: Trickle charging timeout

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x33>STATE3

Addr	Type	Field	Name	Reset	Description
0x33	R/WC	7	CRC32_OK	0	1: CRC32 calculation completed
		6	OTP_WC	0	Chip over temperature(greater than 110℃)status indication: 0: Normal 1: Chip over temperature Set 1 to clear
		5	VIN_OVP_WC	0	VIN OVP status indication： 0: Normal 1: VIN OVP protection Set 1 to clear
		4	VCC_OCP_WC	0	VCC OCP status indication: 0: Normal 1: VCC OCP protection Set 1 to clear
		3	VSYS_SHORT_WC	0	VSYS SHORT status indication: 0: Normal 1: VSYS short circuit Set 1 to clear
		2	VBAT_OC_WC	0	VBAT OCP status indication: 0: Normal 1: VBAT OCP protection Set 1 to clear
		1	VBAT_OD_WC	1	VBAT OD(over discharge) status indication: 0: Normal 1: VBAT over discharge Set 1 to clear
		0	WDT_TO_WC	0	0: Watchdog normal 1: Watchdog timeout

All bits of STATE3 are cleared by writing 1. If the MCU writes 1 to clear this register when the abnormal state persists, the abnormal state will be reset after the system clock arrives.The purpose of this register is to mark the existence of a certain state.

Reset source: POR+Soft

<0x34>COMM_ADCEOC

Addr	Type	Field	Name	Reset	Description
0x34	R/WC	7	CommTimeOut_OV	0	1: CommTimeOut timeout overflow, set 1 to clear
		6	ACK_TX_OK	0	1: Signal transmission of ACK_DATA register is completed, set 1 to clear
		5	VINCMD_RX_OK	0	1: VINCMD received, set 1 to clear
		4	IVINADC_EOC	0	1: IVIN channel ADC conversion completed, set 1 to clear
		3	VINADC_EOC	0	1: VIN channel ADC conversion completed, set 1 to clear
		2	IBATADC_EOC	0	1: IBAT channel ADC conversion completed, set 1 to clear
		1	NTCADC_EOC	0	1: NTC channel ADC conversion completed, set 1 to clear
		0	VBATADC_EOC	0	1: VBAT channel ADC conversion completed, set 1 to clear

Set 1 to clear this register

Reset by POR, SoftRst

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x36~0x37>VBATADCVal

Addr	Type	Field	Name	Reset	Description
0x36	R	7:0	VBATADCValH [11:4]	0x0	High 8 bits of the ADC sample value of VBAT. VBAT= VBATADCVal [11:0] / 4095 * 4600 mV, VBAT= 0V~4.5V
0x37	R	7:4	-	-	-
		3:0	VBATADCValL [3:0]	0x0	Low 4 bits of the ADC sample value of VBAT.

Reset by POR

<0x38~0x39>NTCADCVal

Addr	Type	Field	Name	Reset	Description
0x38	R	7:0	NTCADCValH [11:4]	0x0	High 8 bits of the ADC sample value of NTC. NTC= NTCADCVal [11:0] / 4095 * 4600 mV
0x39	R	7:4	-	-	-
		3:0	NTCADCValL [3:0]	0x0	Low 4 bits of the ADC sample value of NTC.

Reset by POR

<0x3A~0x3B>IBATADCVal

Addr	Type	Field	Name	Reset	Description
0x3A	R	7:0	IBATADCValH [11:4]	0x0	High 8 bits of the ADC sample value of IBAT.
0x3B	R	7:4	-	-	-
		3:0	IBATADCValL [3:0]	0x0	Low 4 bits of the ADC sample value of IBAT.

Reset by POR

1、 When StChip=3'b100 (CC) or 3'b101 (CV), <0x1E>.ICC=0x0~0x2, IBAT (mA)=IBATADCVAL [11:0] * 4600/ (4095*40)

2、 When StChip=3'b100 (CC) or 3'b101 (CV), <0x1E>.ICC=0x3~0x5, IBAT (mA)=IBATADCVAL [11:0] * 4600/ (4095*20)

3、 When StChip=3'b100 (CC) or 3'b101 (CV), <0x1E>.ICC=0x6~0x2C, IBAT (mA)=IBATADCVAL [11:0] * 4600/ (4095*10)

4、 When StChip=3'b100 (CC) or 3'b101 (CV), <0x1E>.ICC=0x2D~0x55, IBAT (mA)=IBATADCVAL [11:0] * 4600/ (4095*2)

5、 When StChip=3'b011 (TC), <0x1F>.ITC=0x0~0x5, IBAT (mA)=IBATADCVAL [11:0] * 4600/ (4095*40)

6、 When StChip=3'b011 (TC), <0x1F>.ITC=0x6~0x8, IBAT (mA)=IBATADCVAL [11:0] * 4600/ (4095*20)

7、 When StChip=3'b011 (TC), <0x1F>.ITC=0x9~0xF, IBAT (mA)=IBATADCVAL [11:0] * 4600/ (4095*10)

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x3C~0x3D>VINADCVal

Addr	Type	Field	Name	Reset	Description
0x3C	R	7:0	VINADCValH [11:4]	0x0	High 8 bits of the ADC sample value of VIN. VIN= VINADCVal [11:0] / 4095 * 4600 * 8 mV, VIN= 3V~6V
0x3D	R	7:4	-	-	-
		3:0	VINADCValL [3:0]	0x0	Low 4 bits of the ADC sample value of VIN.

Reset by POR

<0x3E~0x3F>IVINADCVal

Addr	Type	Field	Name	Reset	Description
0x3E	R	7:0	IVINADCValH [11:4]	0x0	High 8 bits of the ADC sample value of IVIN. IVIN= IVINADCVal [11:0] / (4095*2) * 4600 mA, IVIN= 0mA~1000mA
0x3F	R	7:4	-	-	-
		3:0	IVINADCValL [3:0]	0x0	Low 4 bits of the ADC sample value of IVIN.

Reset by POR

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x40~0x41>NTC_VH

Addr	Type	Field	Name	Reset	Description
0x40	R/W	7:0	VH [7:0]	0x0	NTC high level protection threshold, total 12 bits. Low 8 bits set register.
0x41	R/W	3:0	VH [11:8]	0x0	NTC high level protection threshold, total 12 bits. High 4 bits set register.

Reset by POR ,SoftRst and Watchdog

<0x42~0x43>NTC_VL

Addr	Type	Field	Name	Reset	Description
0x42	R/W	7:0	VL [7:0]	0x0	NTC low level protection threshold, total 12 bits. Low 8 bits set register.
0x43	R/W	3:0	VL [11:8]	0x0	NTC low level protection threshold, total 12 bits. High 4 bits set register.

Reset by POR ,SoftRst and Watchdog

<0x44>NTC_VTHSchm

Addr	Type	Field	Name	Reset	Description
0x44	R/W	1:0	NTC_VTHSchm [1:0]	0x0	Hysteresis configuration of NTC_VH and NTC_VL thresholds for NTC 00: 8 01: 12 10: 16 11: 20

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x45>ADCChx_CFG

Addr	Type	Field	Name	Reset	Description
0x45	R/W	7:5	SingleChxSel	3'b111	When the ADC channel is configured in SingleMode mode, select the input channel of the ADC in this register, and then make <0x5A>=0x2 to enable the AD conversion of that channel immediately. 000: VBAT 001: NTC 010: IBAT 011: VIN 100: IVIN Other values: Invalid channel
		4	IVINADC_Mode	0	0: IVIN disable AutoMode 1: IVIN enable AutoMode
		3	VINADC_Mode	0	0: VIN disable AutoMode 1: VIN enable AutoMode
		2	IBATADC_Mode	0	0: IBAT disable AutoMode 1: IBAT enable AutoMode
		1	NTCADC_Mode	0	0: NTC disable AutoMode 1: NTC enable AutoMode
		0	VBATADC_Mode	0	0: VBAT disable AutoMode 1: VBAT enable AutoMode

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x46>ADC_GF_Ctrl

Addr	Type	Field	Name	Reset	Description
0x46	R/W	7:6	-	-	-
		5:4	ADC_AverTimes	00	Set the conversion time for each channel: 00: 400uS 01: 800uS 10: 1600uS 11: 1600uS
		3	ChgNTCSampleTime	0	NTC sampling interval when charging: 0: consistent with the register Cal_rate 1: Under charging state, sample NTC voltage every 100ms
		2	GFEN	0	GF enable: 0: disable 1: enable
		1	ADCAutoModeStartup	0	Automode conversion enable: 0：disable 1：enable .The channel will perform AD conversion in the order of VIN, VBAT, NTC, IBAT and IVIN, and the conversion results will be saved in the corresponding registers。
		0	ADCEN	0	0：disable ADC 1：enable ADC

Reset by POR and SoftRst

<0x50>VINCMD_RX

Addr	Type	Field	Name	Reset	Description
0x50	R	7:0	VINCMD_RX	0x0	Received data of VINCMD

Reset by POR and SoftRst

<0x51>ACK_DATA

Addr	Type	Field	Name	Reset	Description
0x51	R/W	7:0	ACK_DATA[7:0]	0	Sent data of VINCMD ,MSB first . I2C starts data transmission after writing this register .

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x52>CommConfig0

Addr	Type	Field	Name	Reset	Description
0x52	R/W	7	COMMTimeOutChkMode	0	Sets how to clear the COMMTimeOut register: 0: when VINOK=1, COMMTimeOut register is cleared . When VINOK=0 ,COMMTimeOut register starts counting. 1：The VIN level toggle can clear the COMMTimeOut register。When the VIN level is remaining, the register starts counting. In addition to the above ways to clear the register, there are three ways to clear the register (1)TRX toggle (2)write register CommTimeOutClrIdle=0xAA (3)write register ACK_DATA to send VINCMD
		6:4	COMMTimeOutSet	000	Overflow time to close the COMM channel: 000: when VINOK=0 ,disable timeout. When VINOK=1 , timeout =10ms. 001: 10mS 010: 20mS 011: 80mS 100: 160mS 101: 320mS 110: 640mS 111: 1280mS
		3:2	ACKBitLen	11	Number of bits of ACK_DATA for transmission . MSB first . 00: ACK_DATA=1bit .Only send bit[7] 01: ACK_DATA=2bit .Only send bit[7:6] 10: ACK_DATA=4bit .Only send bit[7:4] 11: ACK_DATA=8bit .Send bit[7:0]
		1	ACK_DATA_SRC	0	Ring transceiver mode: 0: enable .Then the sent data of VINCMD is VINCMD_RX register . 1: disable .Then the sent data of VINCMD is ACK_DATA register .
		0	ACKTxMode	0	The form to acknowledge the VINCMD form case: 0: disable acknowledge 1: auto acknowledge . After receiving the correct VINCMD, GLF70602 will return the ACK_DATA defined by ACK_DATA_SRC immediately.

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x53>CommConfig1

Addr	Type	Field	Name	Reset	Description
0x53	R/W	7:6		-	-
		5	DecACK	0	0: ACK_DATA is returned only when 0x20~0x2F is received ,then trigger IRQ and set <0x34>. VINCMD_RX_OK=1 . 1: ACK is returned when any VINCMD is received ,then trigger IRQ and set <0x34>. VINCMD_RX_OK=1。
		4	ACK_Polarity	0	Polarity configuration for ACK_DATA : 0: No influence on the polarity of ACK_DATA .For example ,when ACK_DATA.bit[x]=1 ,the VIN=1 . 1: Send the ACK register data after negation .For example ,when ACK_DATA.bit[x]=1 ,the VIN=0 .
		3	TRX_Polarity	0	Polarity configuration for data from TRX pin to VIN pin: 0: No influence on the polarity of ACK_DATA .For example ,when TRX=1 ,the VIN=1 . 1: Send the ACK register data after negation .For example ,when TRX=1 ,the VIN=0 .
		2	Comm_DataSrc	0	When COMM on , select the data source to send to VIN: 0: ACK_DATA send to VIN 1: TRX send to VIN
		1:0	CommDirCtrlMode	0	When COMM on and Comm_DataSrc=1 ,TRX transmission direction control mode： 00: IODIR mode .DIR=0 ,data from VIN to TRX ;DIR=1 , data from TRX to VIN . 01: AutoDIR mode . Automatic switching of data direction. 10: RegDIR . Data from VIN to TRX . 11：RegDIR . Data from TRX to VIN . <0x54>.VinComOutDrv must be 0 ,when <0x53>.CommDirCtrlMode = 2'b01(AutoDIR) .

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x54>CommConfig2

Addr	Type	Field	Name	Reset	Description
0x54	R/W	7:6	ITX_VCCEN[1:0]	00	When GLF70602 COMM on and VINOK=1 ,then VCC and BFET state set . 00: VCC OFF 01: VCC ON , BFET charger OFF 1x: VCC ON , BFET charger ON
		5	VinComOutDrv	0	On IODIR/RegDIR mode ,VIN driving capacity . 0: VIN IOH = 3mA ,IOL=10mA . 1: VIN IOH = 3mA ,IOL=5mA <0x54>.VinComOutDrv must be 0 ,when <0x53>.CommDirCtrlMode = 2'b01(AutoDIR) .
		4:3	VIN_VOH	00	VOH of VIN when COMM ON: 00: VOH = 2.5V 01: VOH = VBAT 10: VOH = 3.3V 11: VOH = VBAT
		2	VIN_pulldown	0	VIN pull-down 500k resistance for IODIR and RegDIR when COMM ON: 0: no pull-down 1: pull-down
		1	TRX_pullup	0	TRX pull-up 10k resistance for IODIR and RegDIR when COMM ON: 0: no pull-up 1: pull-up
		0	ACK_RtnDly	0	When ACKTxMode =1 ,select delay time for respond ACK_DATA after received STOP bit: 0: t=1T 1: t=4T

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x55>VinPortConf0

Addr	Type	Field	Name	Reset	Description
0x55	R/W	7	VccOnAsChgEnd	0	VCC state after ChargeEnd: 0: VCC OFF 1: VCC ON
		6	VinOutMode	0	VIN output mode when COMM ON: 0: push-pull 1: open-drain
		5	CaseLowBatDet	0	Enable CaseLowPower detection when COMM off: 0: enable 1: disable
		4	DisCaseDet	0	CaseIn/CaseOut check configuration: 0: enable 1: disable
		3	CaseInVinPdEn	0	VinPulse enable after CaseIn detected: 0: disable 1: enable to send VinPulse
		2	ReChgVinPdEn	0	VinPulse enable after trigger 'recharge request': 0: disable 1: enable to send VinPulse
		1	VinPulseDrv	0	VINPluse driving capacity: 0: 100uA push-down and 80uA push-up 1: 10mA push-down and 1mA push-up
		0	VINPulse	0	VinPulse mode configuration: 0: open-drain mode of VIN for VinPulse 1: push-pull mode of VIN for VinPulse

Reset by POR ,SoftRst and Watchdog

<0x56>VinPortConf1

Addr	Type	Field	Name	Reset	Description
0x56	R/W	7:6	-	-	-
		5	I2C_Rup	0	I2C pull-up resistance configuration: 0: 10kΩ 1: 1kΩ
		4	AutoDIRExitComm	0	Condition to close COMM in AutoDIR mode: 0: when CaseOut is detected and AutoDIRTimeOut is timeout ,the COMM is closed . 1: When register CommTimeOut is timeout, close the COMM immediately
		3	AutoDIRTimeOut	0	AutoDIR mode timeout configuration : 0: disable timeout 1: enable timeout .when VINOK=1 and AutoDIRTimeOut = CommTimeOutSet ,COMM is closed .
		2	AutoDIRCaseInDet	0	Enable CaseLowPower detection in AutoDIR mode when COMM ON : 0: disable 1: enable
		1:0	ExtVinSnkPower	00	VIN Iq : 00: 8.5uA 01: 13.5uA 10: 19.5uA 11: 24.5uA

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x57>BATOCD_PWK

Addr	Type	Field	Name	Reset	Description
0x57	R/W	7:6	IBAT_OC[1:0]	00	VBAT discharge OC threshold: 00: 250mA 01: 500mA 10: 1000mA 11: 1500mA
		5:4	VBAT_OD[1:0]	00	VBAT over discharge voltage : 00: 2.60V 01: 2.80V 10: 3.00V 11: 3.20V
		3	ShipModeDelaySet	0	Delay time to trun off BFET when shipmode command is received . 0: 100ms 1: 4s
		2	ExitShipModeSendPwk	0	0: no action 1: send PWK when exit shipmode
		1	PwkLevelSet	0	PWK active level: 0: L level active ,NMOS open-drain 1: H level active ,PMOS open-drain
		0	EnCaseOutSendPwk	0	0: no action 1: send PWK when CaseOut detected

Reset by POR ,SoftRst and Watchdog

<0x58>RST_IRQ

Addr	Type	Field	Name	Reset	Description
0x58	R/W	7	IRQ_WidthSet	0	Effective duration time of IRQ: 0: 8ms of the low level pulse 1: 2s of the low level pulse, and clear this pulse when write <0x5A>=0x8
		6	EnCaseInSendRst	0	0: no action 1: send RST when CaseIn detected
		5:4	RST_WidthSet[1:0]	01	RST pulse duration time: 00: 50mS 01: 100mS 10: 200mS 11: 500mS
		3	RstLevelSet	0	RST valid voltage level configuration : 0: Low level, and NMOS outputs with open-drain 1: High level, PMOS outputs with open-drain, and PMOS is pulled up to VSYS
		2:0	RST_DelaySet[2:0]	001	Delay time of sending RST when earbuds enter the cradle: 000: 1S 001: 2S 010: 4S 011: 8S 100: 10S 101: 12S 110: 16S 111: 20S

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x59>PWK_Wave_Conf

Addr	Type	Field	Name	Reset	Description
0x59	R/W	7:6	PWK_IntervalSet[1:0]	00	Time interval between two single click pulses when PWK double click: 00: 100mS 01: 200mS 10: 300mS 11: 400mS
		5:4	PWK_LPressTime[1:0]	00	Long-press time of PWK indication: 00: 2S 01: 3S 10: 4S 11: 5S
		3	PWK_SPressTime	0	Effective time of PWK single click, double clicks and triple clicks: 0: 200mS 1: 500mS
		2:0	PWK_LLPressTime[2:0]	000	Effective time of PWK long long-press: 000: 4S 001: 6S 010: 8S 011: 10S 100: 12S 101: 14S 110: 16S 111: 20S

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0x5A>I2C_CMD

<table>
<tr><th>Addr</th><th>Type</th><th>Field</th><th>Name</th><th>Reset</th><th colspan="2">Description</th></tr>
<tr><td rowspan="14">0x5A</td><td rowspan="14">W</td><td>7:4</td><td>-</td><td>-</td><td colspan="2">-</td></tr>
<tr><td rowspan="13">3:0</td><td rowspan="13">i2c_cmd [3:0]</td><td rowspan="13">0</td><td colspan="2">I2C 指令操作</td></tr>
<tr><td>指令</td><td>描述</td></tr>
<tr><td>0001</td><td>EnReChg:
(1) when StChip=standby , VINPulse will be sent .
(2) when VINOK=1 ,restart charging .</td></tr>
<tr><td>0010</td><td>ADC_SingleStart: start ADC conversion</td></tr>
<tr><td>0011</td><td>TurnOnShipmode:
when StChip=standby ,enter shipmode</td></tr>
<tr><td>0100</td><td>Restart:
When StChip= standby or Chg ,restart VSYS .But when COMMON ,the command will be ignored .</td></tr>
<tr><td>0101</td><td>TurnOffCOMM:
Turn off COMM immediately .</td></tr>
<tr><td>0110</td><td>TurnOnComm:
Trun on COMM immediately .</td></tr>
<tr><td>0111</td><td>Clr_Rst: reset RST pulse</td></tr>
<tr><td>1000</td><td>Clr_Irq:
When IRQ_WidthSet=1 ,reset IRQ</td></tr>
<tr><td>1001</td><td>CRC32_Calc:
Start CRC32 calculation</td></tr>
<tr><td>1010</td><td>-</td></tr>
<tr><td>1011</td><td>Reset 2s fault hiccup</td></tr>
<tr><td>-</td><td>-</td></tr>
</table>

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x5B>IRQ_EN0

Addr	Type	Field	Name	Reset	Description
0x5B	R/W	7	VIN_STAT_IRQ_EN	1	VIN_OVP、VIN_OK、VIN_UVLO IRQ : 0: disable 1: enable
		6	VCC_OCP_IRQ_EN	1	VCC_OCP IRQ : 0: disable 1: enable
		5	CHG_TimeOut_IRQ_EN	1	ITC Timeout、FC Timeout IRQ : 0: disable 1: enable
		4	CHIP_OTP_IRQ_EN	1	Chip OTP IRQ : 0: disable 1: enable
		3	CaseSTAT_IRQ_EN	1	CaseIn ,Case out IRQ : 0: disable 1: enable
		2	Init_OK_IRQ_EN	1	INIT_OK IRQ : 0: disable 1: enable
		1	ReChg_IRQ_EN	1	VBAT recharge IRQ : 0: disable 1: enable
		0	NTC_IRQ_EN	1	NTC threshold overflow IRQ : 0: disable 1: enable

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x5C>IRQ_EN1

Addr	Type	Field	Name	Reset	Description
0x5C	R/W	7	ADCEndOfConv_IRQ_EN	1	ADC end of convertion IRQ : 0: disable 1: enable
		6	ACK_IRQ_EN	1	ACK_DATA sent IRQ : 0: disable 1: enable
		5	VINCMD_RX_IRQ_EN	1	VINCMD received IRQ : 0: disable 1: enable
		4	1%SOC_IRQ_EN	0	Every 1% change of GF SOC IRQ : 0: disable 1: enable
		3	100%SOC_IRQ_EN	0	GF SOC from 99% to 100% IRQ : 0: disable 1: enable
		2	0%SOC_IRQ_EN	0	GF SOC from 1% to 0% IRQ : 0: disable 1: enable
		1	LowSOC_IRQ_EN	0	GF low SOC IRQ : 0: disable 1: enable
		0	CRC32_IRQ_EN	0	GF CRC32 finished IRQ : 0: disable 1: enable

Reset by POR ,SoftRst and Watchdog

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x5D>IRQ_EN2

Addr	Type	Field	Name	Reset	Description
0x5D	R/W	7:5	-	-	-
		4	INT_SHT_IRQ_EN	1	Inductor short IRQ: 0: disable 1: enable
		3	VCCDPM_IRQ_EN	1	VCCDPM IRQ : 0: disable 1: enable
		2	IINDPM_IRQ_EN	1	IINDPM IRQ : 0: disable 1: enable
		1	SysStat_IRQ_EN	1	StChip stat change IRQ : 0: disable 1: enable
		0	CommTimeOut_IRQ_EN	1	CommTimeOut IRQ : 0: disable 1: enable

Reset by POR ,SoftRst and Watchdog

<0x69>I2C_ChipID

Addr	Type	Field	Name	Reset	Description
0x69	R	7:0		0x68	Chipid ,default: 0x68

<0x6A>RstWdg

Addr	Type	Field	Name	Reset	Description
0x6A	W	7:0	RstWdg	0x0	Write <0x6A>=0x55 to reset Watchdog

<0x6B>CommTimeOutClrIdle

Addr	Type	Field	Name	Reset	Description
0x6B	W	7:0	CommTimeOutClrIdle	0x0	Write <0x6B>=0xAA to reset CommTimeOut counter

<0x6C>SoftRst

Addr	Type	Field	Name	Reset	Description
0x6C	W	7:0	SoftRst	0x0	Write <0x6C>=0x17 to reset GLF70602 all register .

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0x80~0xFF>GF Register

<0x80~0xD4>GF parameter register

<0xD5>C_Ratio_Customer

Addr	Type	Field	Name	Reset	Description
0xD5	R/W	6:0	C_Rate[7:0]	0x0	Battery capacity compensation

<0xE0~0xE1>VBATGF

Addr	Type	Field	Name	Reset	Description
0xE0	R	7:0	VBAT [12:5]	0x0	VBAT= VBAT [12:5]*32 + VBAT [4:0] , unit: mV
0xE1	R	7:5	-	-	-
		4:0	VBAT [4:0]	0x0	VBAT= VBAT [12:5]*32 + VBAT [4:0] , unit: mV

<0xE2>TempGF

Addr	Type	Field	Name	Reset	Description
0xE2	R	7:0	TempFG[7:0]	0x0	NTC temperature ,range -128℃~127℃ , step=1℃ . When bit7=1, the temperature is negative .

<0xE3>IBATGF

Addr	Type	Field	Name	Reset	Description
0xE3	R	7:0	IBAT[7:0]	0x0	Charge IBAT ,range 0~500mA，step=2mA

<0xE4~0xE5>OCV

Addr	Type	Field	Name	Reset	Description
0xE4	R	7:0	OCV[7:0]	0x0	OCV value
0xE5	R	7:0	OCV[15:8]	0x0	

<0xE6~0xE7>Kint

Addr	Type	Field	Name	Reset	Description
0xE6	R	7:0	Kint[7:0]	0x0	Kint value
0xE7	R	7:0	Kint[15:8]	0x0	

<0xE8>SOC_Report

Addr	Type	Field	Name	Reset	Description
0xE8	R	7:0	SOC_Report [7:0]	0x0	Report the smoothed SOC value

<0xE9>SOC_Int

Addr	Type	Field	Name	Reset	Description
0xE9	R	7:0	SOC_Int[7:0]	0x0	Report the SOC value corresponding to OCV table

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0xEA>SOC_Dsg

Addr	Type	Field	Name	Reset	Description
0xEA	R	7	CALCU_DONE	0	GF calculation state : 0: calculating 1: done
		6:0	SOC_Dsg[6:0]	0x0	SOC_Dsg report value

<0xEB>BAT_COMP_IBAT

Addr	Type	Field	Name	Reset	Description
0xEB	R	7:0	BatComp_IBAT[7:0]	0x0	IBAT of battery internal resistance compensation: 0~500mA，step=2mA

<0xEC~0xEF>CRC32

Addr	Type	Field	Name	Reset	Description
0xEC	R	7:0	CRC32 [7:0]	0x0	CRC32 for <0x80>~<0xD4> registers .The result is <0xEF>~<0xEC>=0x3F97981F。
0xED	R	7:0	CRC32 [15:8]	0x0	
0xEE	R	7:0	CRC32 [23:16]	0x0	
0xEF	R	7:0	CRC32 [31:24]	0x0	

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0xF0>GF_Config1

Addr	Type	Field	Name	Reset	Description
0xF0	R/W	7	OSC_MODE	0	GF OSC selection : 0: when StChip=010~101 ,GF OSC select HOSC ;when Stchip=others ,GF OSC select LOSC 1: when GF_SLEEP_MODE =1 ,GF OSC select HOSC ;when GF_SLEEP_MODE =0 ,GF OSC select LOSC .
		6	GaugeEncg	0	When BypassMode=1 , Configure the GF charging and discharging state : 0: discharging 1: charging
		5	Bypass_Start	0	When BypassMode=1 , the GF can be started in the following two ways: 0: write <0Xfb>=0x1 to startup GF 1: GF can be startup every fixed time which defined by Cal_rate[1:0]
		4	BypassMode	0	GF working mode configuration : 0: normal mode 1: bypass mode
		3	Gauge_suspend	0	GF suspend enable : 0: disable 1: enable ,then GF will hold OCV and SOC value
		2	Kint_WR	0	When BypassMode=1 ,source of Kint : 0: Kint is called in default vaule 1: Kint is called in register UserKint<0xF7>~<0xF8>
		1	TEMP_WR	0	When BypassMode=1 ,source of Temp : 0: Temp is called in default vaule 1: Temp is called in register UserTemp<0xF5>
		0	VBAT_WR	0	When BypassMode=1 ,source of VBAT : 0: VBAT is called in default vaule 1: VBAT is called in register UserVBAT <0xF3>~<0xF4>

Reset by POR ,SoftRst

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

<0xF1>GF_Config2

Addr	Type	Field	Name	Reset	Description
0xF1	R/W	7:6	-	-	-
		5:4	Cal_rate	00	Working time cycle of GF : 00: every 2S 01: every 4S 10: every 0.5S 11: every 1S
		3:2	SOC_LOW	00	SOC low battery alarm threshold : 00：SOC_LOW=1% 01：SOC_LOW=5% 10：SOC_LOW=10% 11：SOC_LOW=20%
		1	99%HOLD	0	mode of reporting 100%SOC : 0: do not hold 1: SOC will not report 100% during charging until charge reports chgdone
		0	100%FORCE	0	force100% enable : 0: disable 1: enable ,then OCV、SOC_Report、SOC_INIT、SOC_DSG will be max value

Reset by POR ,SoftRst

<0xF2>GF_Sleep

Addr	Type	Field	Name	Reset	Description
0xF2	R/W	7:3	-	-	-
		2:1	GF_IterationTime	01	When GF_SLEEP_MODE=1 ,GF iteration time configuration bits .GF will calculate n times every time sampling . 00: 2 times 01: 4 times 10: 8 times 11: 16 times
		0	GF_SLEEP_MODE	0	Sleepmode enable : 0: nomal .when VINOK=1 ,this bit will be clear automatically . 1: enable sleepmode

Reset by POR ,SoftRst

<0xF3~0xF4>UserVBAT

Addr	Type	Field	Name	Reset	Description
0xF3	R/W	7:0	UserVBAT[7:0]	0x0	lower 8 bits of UserVBAT , written by host
0xF4	R/W	4:0	UserVBAT [12:8]	0x0	master 5 bits of UserVBAT , written by host

If the actual battery voltage is VBAT, then UserVBAT [12:0]=VBAT . For example, when VBAT=3000mV, UserVBAT [12:0]=3000 .When BypassMode=1 and VBAT_WR=1 ,user must write UserVBAT register .

Reset by POR ,SoftRst

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

<0xF5>UserTemp

Addr	Type	Field	Name	Reset	Description
0xF5	R/W	7:0	UserTemp[7:0]	0x0	The temperature value written by the host. The temperature range is - 128 ℃~+127 ℃. Bit7=1 represents negative temperature, Bit7=0 represents positive temperature.

If the actual battery temperature is Temp, then UserTemp [7:0]=Temp. For example, if Temp=10 ℃, UserTemp [7:0]=10; Temp = -10℃， UserTemp[7:0]=0x8A .When BypassMode=1 and TEMP_ WR=1, user need to configure UserTemp register .

Reset by POR ,SoftRst

<0xF6>UserIBAT

Addr	Type	Field	Name	Reset	Description
0xF6	R/W	7:0	UserIBAT[7:0]	0x0	IBAT written by host

When the actual battery current is IBAT, UserIBAT [7:0]=IBAT/2. For example, if IBAT=10mA, UserIBAT [7:0]=5.

Reset by POR ,SoftRst

<0xF7~0xF8>UserKint

Addr	Type	Field	Name	Reset	Description
0xF7	R/W	7:0	UserKint[7:0]	0x0	Kint IBAT written by host
0xF8	R/W	7:0	UserKint[15:8]	0x0	Kint IBAT written by host

Reset by POR ,SoftRst

<0xFB>GF_BP_Startup

Addr	Type	Field	Name	Reset	Description
0xFB	R	7	GF_BP_Startup	0	When BypassMode=1, write <0xFB>=0x1, and the GF will start to calculate once.

Reset by POR ,SoftRst

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

9 Application and Implementation

9.1 System Example

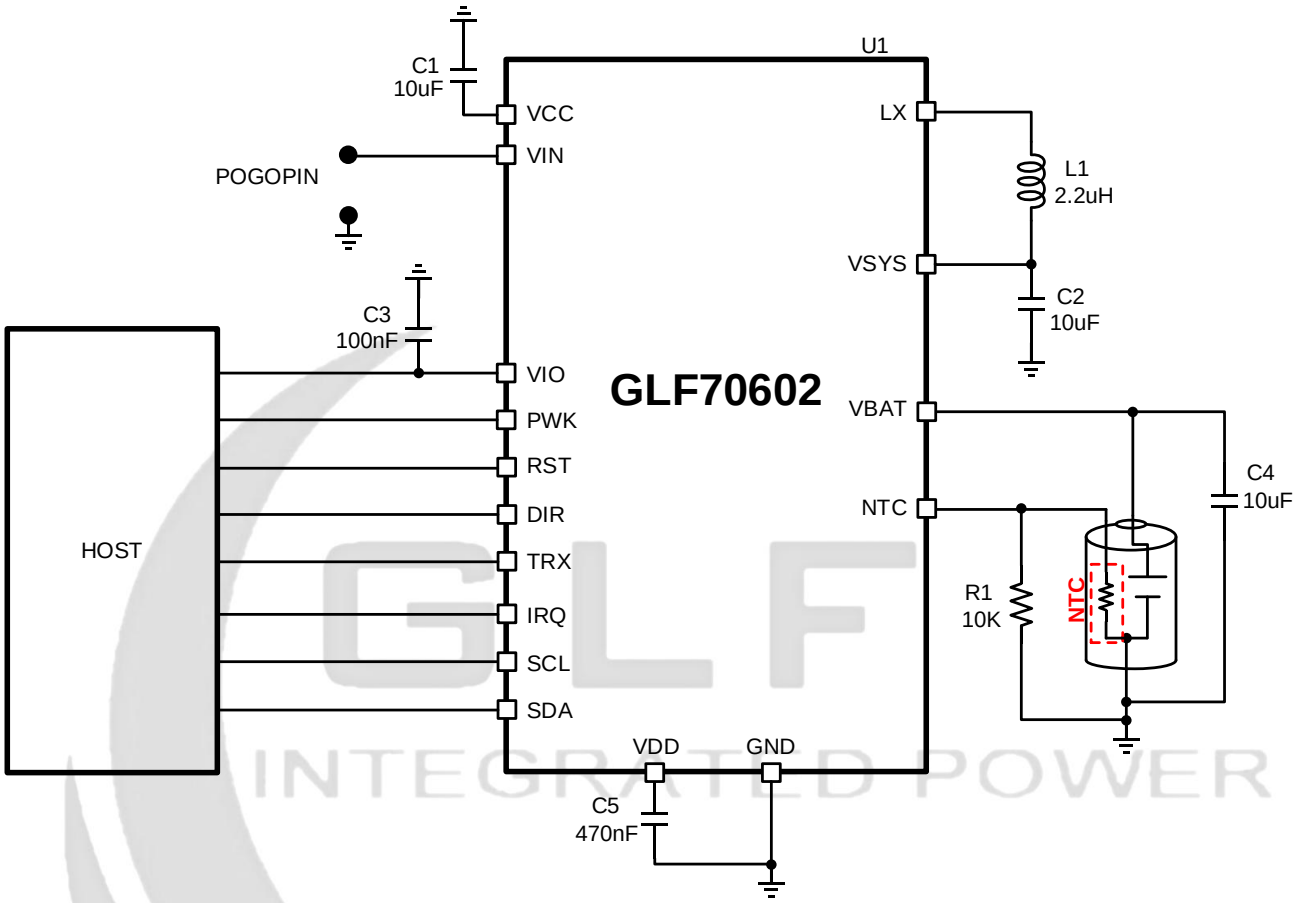


Figure 9-1. System Application

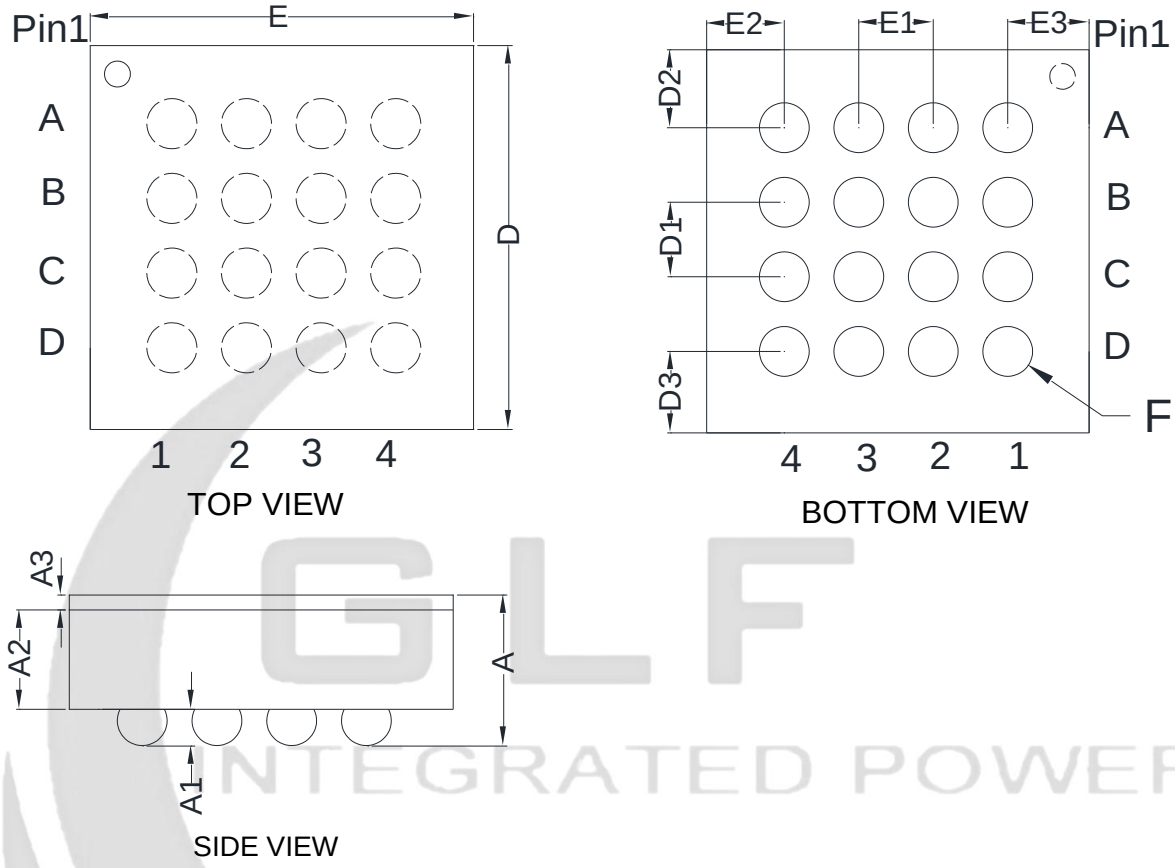
9.2 Bill of Materials

Components	Device type	Device description	Manufacturer	Parameter	Quantity
U1	GLF70602		GLF		1
C1、C2、C4	Cap	0402/X5R/10V/10μF	Samsung	10μF	3
C3	Cap	0402/X5R/10V/100nF	Samsung	100nF	1
C5	Cap	0402/X5R/10V/470nF	Samsung	470nF	1
R1	Res	0402/1%/10K	YAGEO	10K	1
NTC	Res	0402/NTC/10K/B=3380K	muRata	10K	1
L1	Indutor	1206/2.2μH/1.2A	YAGEO	2.2μH	1

Copyright © 2023 GLF Integrated Power. All Rights Reserved.

10 Package Outline and Layout

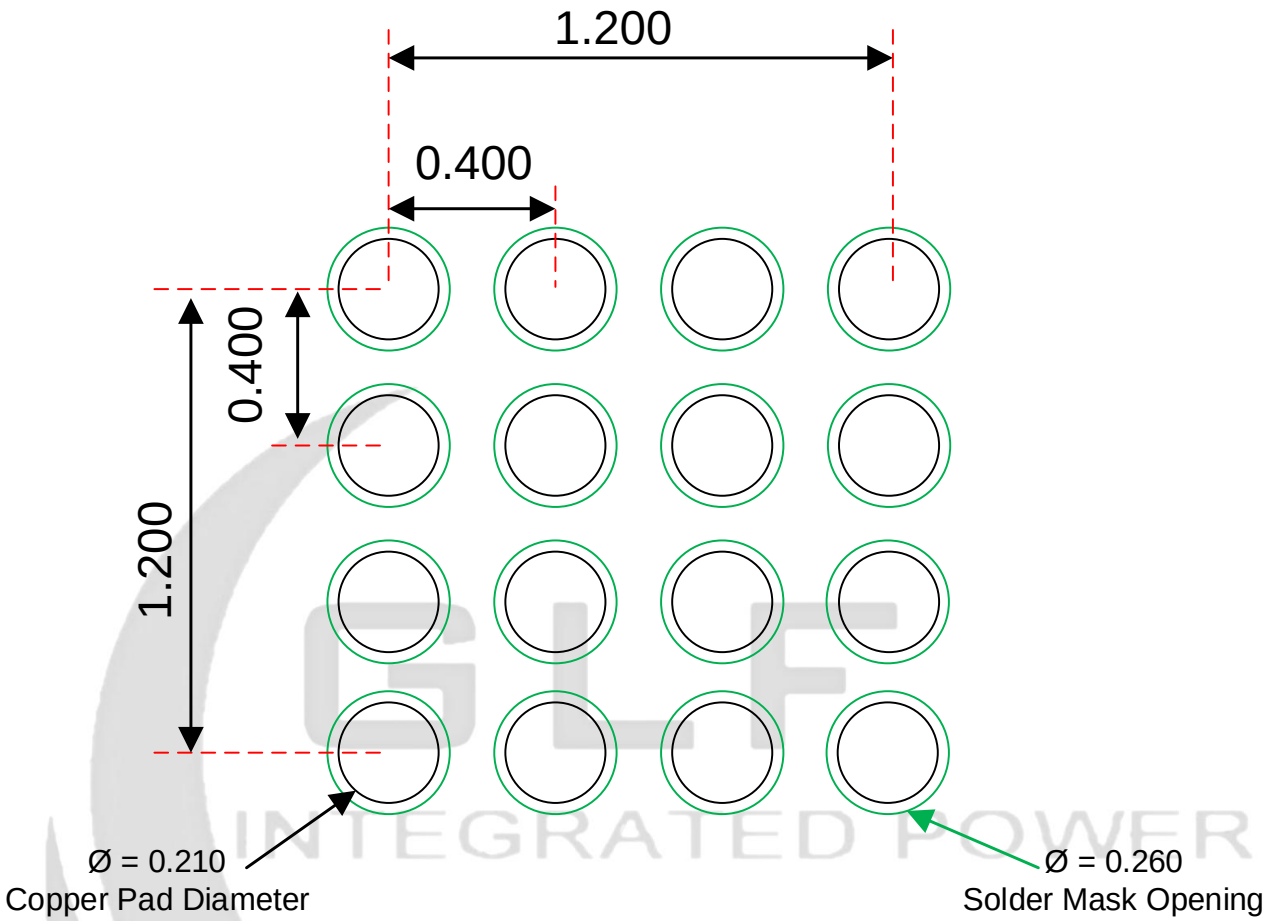
10.1 Package Outline(CSP)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.545	0.625	0.021	0.025
A1	0.170	0.220	0.007	0.009
A2	0.335	0.365	0.013	0.014
A3	0.035	0.045	0.001	0.002
D	2.030	2.080	0.080	0.082
E	2.030	2.080	0.080	0.082
D1	0.400 BSC.		0.016 BSC.	
D2	0.4175 BSC.		0.016 BSC.	
D3	0.4375BSC.		0.017 BSC.	
E1	0.400 BSC.		0.016 BSC.	
E2	0.4175 BSC.		0.016 BSC.	
E3	0.4375BSC.		0.017 BSC.	
F	0.245	0.290	0.010	0.011

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

10.2 Recommended Land Pattern(CSP)



Unit: mm

Figure 10-1. Recommended Land Pattern

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

10.3 Layout Guidelines

1. Via will cause high impedance of the path. If a large current needs to pass through the via in the design, it is recommended to use multiple vias to reduce the impedance.
2. The chip GND is directly connected to the system ground, and the connected copper foil needs to be short, thick and intact as far as possible, without being cut off by other traces.
3. The capacitor used in the application must be made of X5R or higher.

10.4 Layout Example

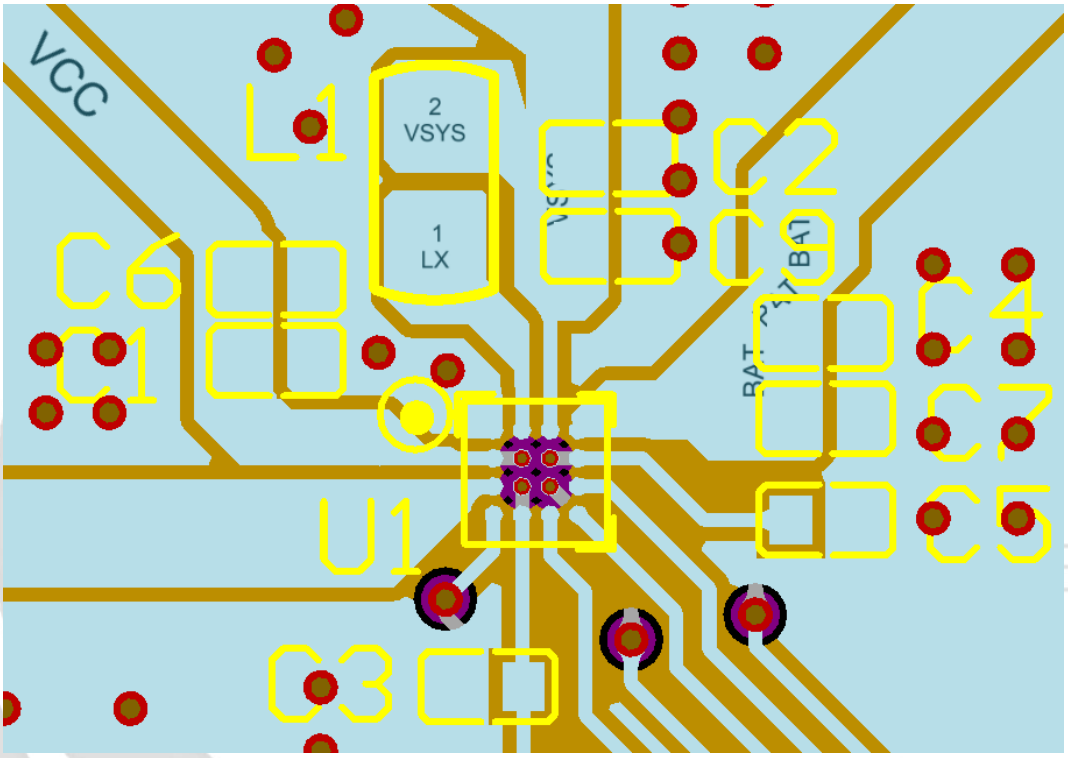


Figure 10-2. Layout Example

Copyright © 2023 GLF Integrated Power. All Rights Reserved.
www.glfipower.com

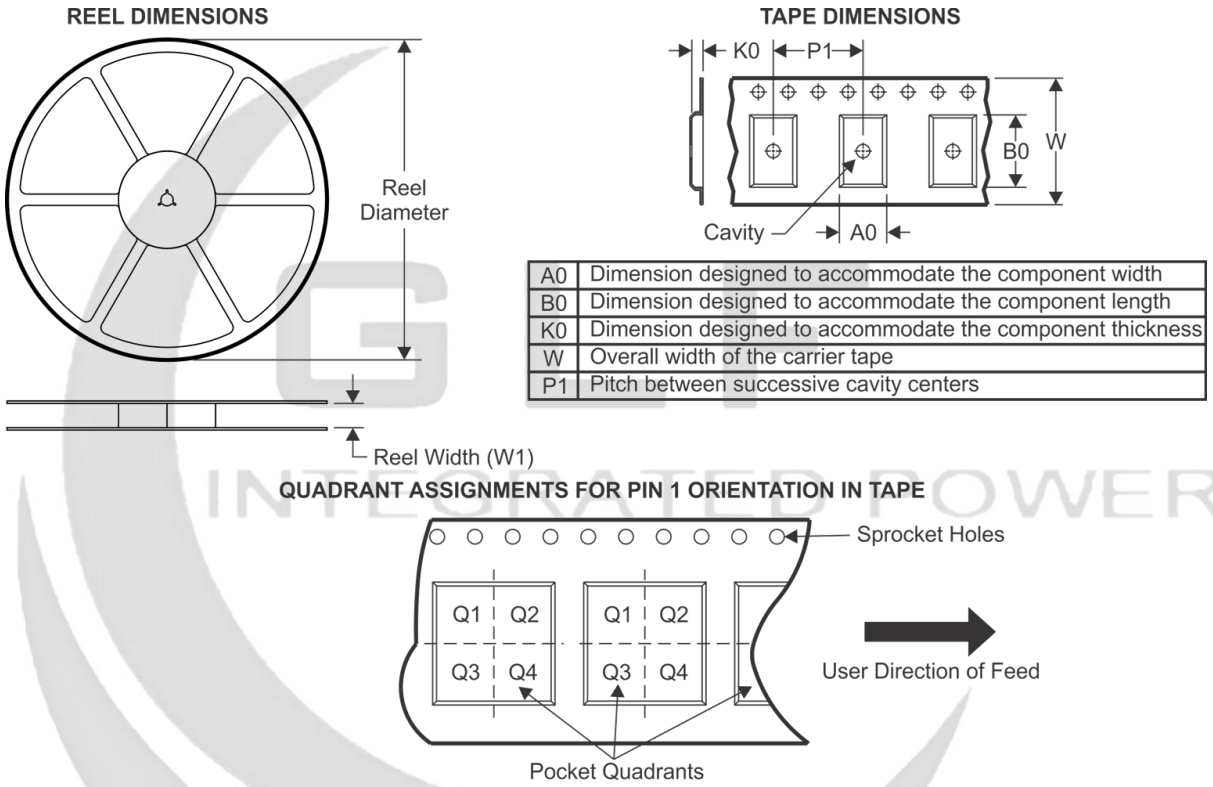
11 Packaging and Ordering Information

11.1 Ordering Information

Part Number	Package	Description	Package Qty (item)
GLF70602-S87	CSP16	-	3000

11.2 Tape and Reel Information

(The following is an example)



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
GLF70602	CSP	CSP	16	3000	180	9.5	2.2	2.2	0.75	4.0	8.0	Q1

11.3 Package Quantity Information

Orderable Device	Package Type	MSL	Quantity per plate	Quantity per box	Quantity per trunk
GLF70602-S87	CSP16	MSL1	3000	-	-

Copyright © 2023 GLF Integrated Power. All Rights Reserved.