GLF70581

Power Management Integrated Circuit with 4 Bucks and 2 LDOs

Preliminary Specification

1. Description

The GLF70581 is a power management IC (PMIC) designed for notebook, desktop, and embedded computing platforms. There are four DCDC converters and two linear regulators integrated into the GLF70581, which can minimize the need for external components so that it can ease the layout in a constrained PCB area. The DCDC converters are of high accuracy, high efficiency, and high flexibility. Two LDOs provide power rails for peripherals and pull-up resistors.

The GLF70581 provides protection for a device when a fault occurs, such as overcurrent, output overvoltage, output undervoltage, short circuit, input overvoltage, and over temperature.

The GLF70581 is a halogen- and lead-free device, compliant with RoHS. The package is WLCSP-36 2.4 x 2.4.

2. Applications

Solid-state drive

Video system

3. Features

- AVIN input supply range: 2.7V to 5.5V
- Four buck regulators
  - BUCK1, output range 1.7V ~ 3.3V
  - BUCK2, output range 0.9V ~ 2.0V
  - BUCK3, output range 0.5V ~ 1.3V
  - BUCK4, output range 0.675V ~ 2.0V
- 2 linear regulators
  - LDO1, 1V ~ 3.3V, 50mV/Step, 0.4A
  - LDO2, 1V ~ 3.3V, 50mV/Step, 0.4A
- 2 external converters
- DCDC voltage accuracy: ±1% FB Voltage
- PWM frequency adjustable:
  1Mhz~3Mhz, step 500Khz
- BUCK1 can be set as load switch
- BUCK4 can be set as linear regulator
- LDO1/LDO2 can be set as load switch
- Configurable Soft-start Time for All output
- Configurable power on sequence
- Configurable sleep and wake-up sequence
- I2C Interface 400kHz/1MHz/3.4MHz
- Built-in AVIN OV/UV warning indication and fault protection
- Built-in VOUT OVP/UVP/OCL
- Built-in Overed Temperature Protection
- Built-in EFUSE for configurable default value of registers
- 8 multifunctional IOs

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4. Typical Application Circuit

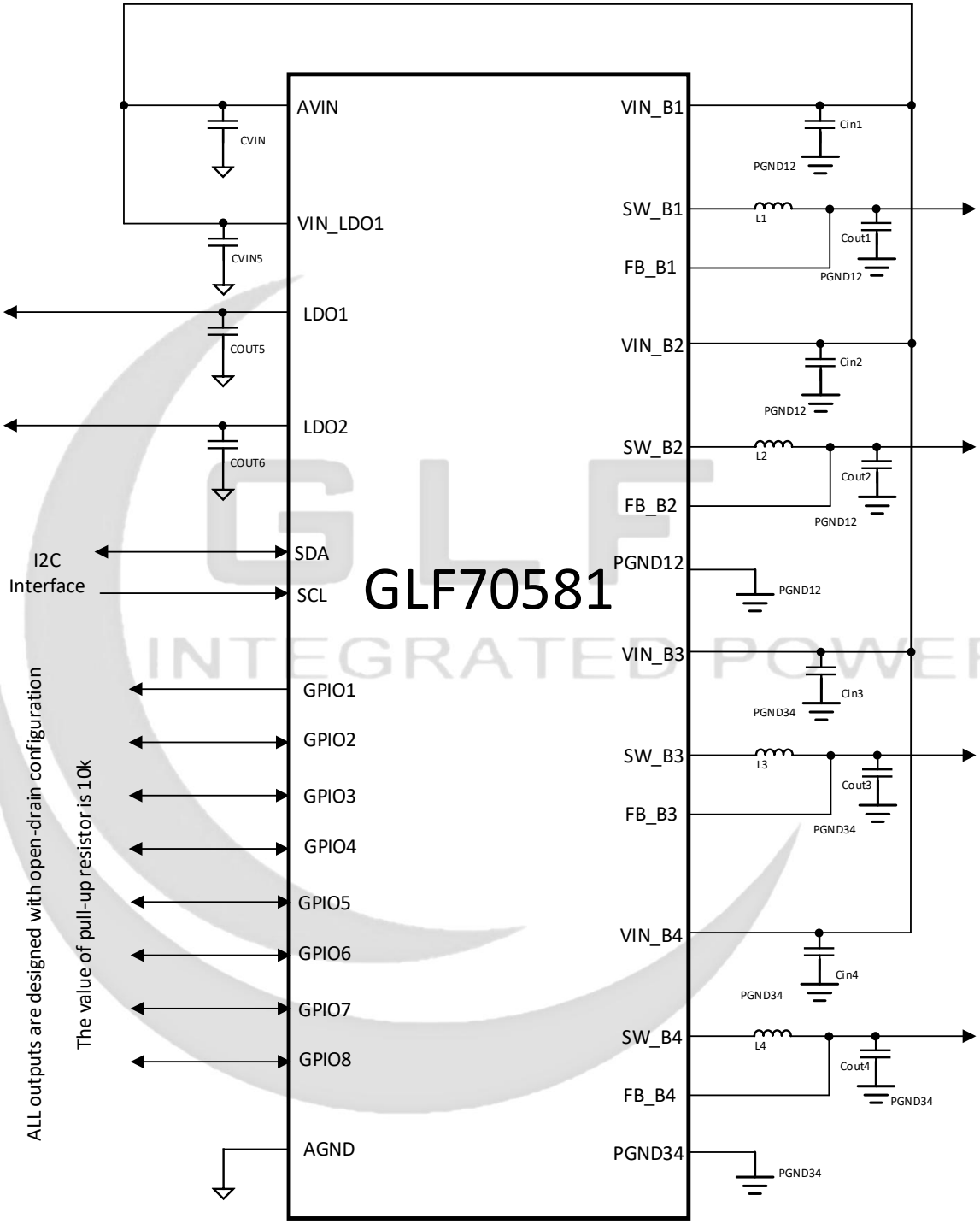

Figure 4-1. Typical Application Circuit

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5. Pin Configuration and Functions

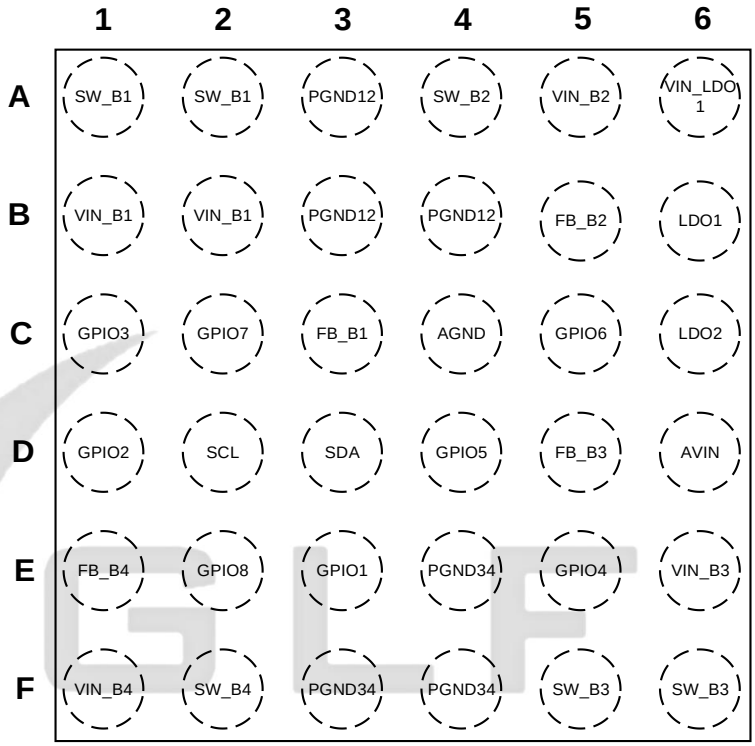

Figure 5-1. Pin Configuration

Pin Description

Name	No.	I/O	Description
PGND12	A3, B3, B4	G	Dedicated Power Ground for Buck1 and Buck2 Regulator.
PGND34	E4, F3, F4	G	Dedicated Power Ground for Buck3 and Buck4 Regulators
SW_B1	A1, A2	O	Switch Pin for Buck 1 Regulator.
VIN_B1	B1, B2	P	Dedicated VIN power input for Buck 1 Regulator.
FB_B1	C3	I	Feedback for Buck 1 Regulator. Connect to the Buck 1 output capacitor.
SW_B2	A4	O	Switch Pin for Buck 2 Regulator.
VIN_B2	A5	P	Dedicated VIN power input for Buck 2 Regulator.
FB_B2	B5	I	Feedback for Buck 2 Regulator. Connect to the Buck 2 output capacitor.
SW_B3	F5, F6	O	Switch Pin for Buck 3 Regulator.
VIN_B3	E6	P	Dedicated VIN power input for Buck 3 Regulator.

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FB_B3	D5	I	Feedback for Buck 3 Regulator. Connect to the Buck 3 output capacitor.
SW_B4	F2	O	Switch Pin for Buck 4 Regulator.

Pin Description (continued)

Name	No.	I/O	Description
VIN_B4	F1	P	Dedicated VIN power input for Buck 4 Regulator.
FB_B4	E1	I	Feedback for Buck 4 Regulator. Connect to the Buck 4 output capacitor.
LDO1	B6	O	Output for LDO1 Regulator (Leave unconnected if LDO is not used and disabled).
VIN_LDO1	A6	P	Dedicated VIN power input for LDO Regulator.
LDO2	C6	O	Output for LDO2 Regulator (Leave unconnected if LDO is not used and disabled).
SCL	D2	I	I^2C Clock Input.
SDA	D3	I/O	I^2C Data Input and Output.
AGND	C4	G	Analog Ground. Kelvin connects to the other ground pins on the IC.
GPIO1	E3	O	Configurable general-purpose input/open drain output.
GPIO2	D1	I/O	Configurable general-purpose input/open drain output.
GPIO3	C1	I/O	Configurable general-purpose input/open drain output.
GPIO4	E5	I/O	Configurable general-purpose input/open drain output.
GPIO5	D4	I/O	Configurable general-purpose input/open drain output.
GPIO6	C5	I/O	Configurable general-purpose input/open drain output.
GPIO7	C2	I/O	Configurable general-purpose input/open drain output.
GPIO8	E2	I/O	Configurable general-purpose input/open drain output.
AVIN	D6	P	Analog Input supply and power input for LDO2. This is also the pin that is monitored for VIN OV and UV.

P - Power supply; G - Gnd; I - Input; O - Output

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6 Specifications

6.1 Absolute Maximum Ratings

PARAMETER	Min	Max	Unit
ALL VIN to all GND	-0.3	6.5	V
All PGND to GND	-0.3	6.5	V
SW_Bx to PGNDx	-1	VIN_Bx+1	V
FB_Bx to PGNDx	-0.3	VIN_Bx+0.3	V
LDO1 to AGND	-0.3	VIN_LDO+0.3	V
All I/O to PGND12，PGND34，GND	-0.3	6.5	V
Operating Junction Temperature	-40	125	℃
Storage Temperature	-65	150	℃
MSL Rating	1		

6.2 Recommended Operating Conditions

		Min	Nom	Max	Unit
T_A	Ambient temperature	-40		85	℃
T_J	Junction temperature	-40		125	℃
AVIN / VINx	Supply Input Voltage	2.7		5.5	V
Other Pins	Other Pins	0		5.5	V

6.3 ESD Rating

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per Mil-Std-883H Method 3015.8 1, all pins	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	V

6.4 Thermal Information

Thermal Metric		Package Type	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	℃/W

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6.5 Electrical Characteristics

VIN_Bx = VIN_LDO1 = AVIN = 3.3V, T_A=25℃ for typical values (unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VSYS						
VIN UVLO	UVLO	Falling Threshold	2.25	2.4	2.55	V
		hysteresis	--	0.15	--	V
VIN UV_SHUT	V_{UV_SHUT}	Falling Threshold	2.55	2.6	2.65	V
		hysteresis	--	0.05	--	V
VIN VSYSMON	V_{SYSMON}	Falling Threshold,sysmon_sel=0000	2.7	2.725	2.75	V
		hysteresis	--	0.05	--	V
VIN VSYSWARN	$V_{SYSWARN}$	Falling Threshold,syswarn_sel=0000	2.725	2.775	2.825	V
		hysteresis	--	0.05	--	V
VIN over voltage warning Threshold	V_{POK_OV}	Rising Threshold,pok_ov_sel=010	3.6	3.7	3.8	V
		hysteresis	--	0.2	--	V
VIN over voltage Protection Threshold	V_{AVIN_OV}	Rising Threshold,vin_ov_sel=010	3.8	3.9	4.0	V
		hysteresis	--	0.2	--	V
Over Temperature Warning	T_{WARN}	Rising Threshold	--	120	--	℃
		Falling Threshold	--	100	--	℃
Over Temperature Protection	T_{SHUT}	Rising Threshold	--	150	--	℃
		Falling Threshold	--	125	--	℃
Operating Supply Current						
AVIN Supply Current	I_{AVIN}	All Rails off	--	26	30	uA
VIN_LDO1	I_{LDO1}	Normal Mode	--	35	40	uA
		Low Power Mode	--	22	25	uA
VIN_B1	I_{Buck1}	Normal Mode	--	50	60	uA
		Low Power Mode	--	40	50	uA
VIN_B2 / VIN_B3 / VIN_B4	I_{Buckx}	Normal Mode	--	35	40	uA
		Low Power Mode	--	25	30	uA
BUCK1						
Output Voltage range	V_{B1_VOUT}	Configured for 20mV steps	1.7	--	3.3	V
Output Voltage Offset	V_{B1_ERR}		-1		1	%Vout
Line Regulation		VIN = 2.7V to 5.5V	--	0.5	--	%/V
Load Regulation		IOUT= 0 to OCL	--	0.5	--	%/A
Load Transient		VIN = 3.3V,VOUT = 2.5V, L = 0.47uH,COUT = 22uFx2. 1.Load = 1A to 2A @ 0.2A/us. 2.Load = 50mA to 1A @ 0.2A/us.	--	4	--	%Vout

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Electrical Characteristics(continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
UVP Threshold	V_{B1_UV}	Falling Threshold	87	90	93	%Vout
		hysteresis	--	3	--	%Vout
OVP Threshold	V_{B1_OV}	Rising Threshold	107	110	113	%Vout
		hysteresis	--	3	--	%Vout
OCL Threshold	V_{B1_OC}	B1_IMAX = 00	3.5	4	--	A
		B1_IMAX = 01	4.5	5	--	A
		B1_IMAX = 10	5.5	6	--	A
		B1_IMAX = 11	6.5	7	--	A
Switching Frequency	f_{SW_B1}	B1_FREQ = 101	--	2	--	MHz
Min Off-Time			--	120	--	nS
PMOS On- Resistance	R_{DSON_B1P}	VIN_B1 = 3.3V	--	30	--	mΩ
NMOS On Resistance	R_{DSON_B1N}	VIN_B1 = 3.3V	--	35	--	mΩ
Output Discharge Resistance	R_{DISCH_B1}	B1_DISRES = 0	--	10	--	Ω
		B1_DISRES = 1	--	4	--	Ω
efficiency	Eff_{B1}	AVIN = 3.3V,VOUT = 2.5V,IOUT=10mA	--	92	--	%
		AVIN = 3.3V,VOUT = 2.5V,IOUT=1A	--	96	--	%
		AVIN = 3.3V,VOUT = 2.5V,IOUT=2A	--	94	--	%
BUCK1 Load Switch Mode						
VIN_B1 Voltage			2.7	3.3	3.7	V
PMOS On Resistance	R_{DSON_B1P}	VIN_B1 = 3.3V	--	30	--	mΩ
OCL Threshold	V_{B1LSW_OC}		--	5	--	A
UVP Threshold	V_{B1LSW_UV}	Falling Threshold	87	90	93	%Vout
		Rising Threshold	--	3	--	%Vout
BUCK2						
Output Voltage range	V_{B2_VOUT}	Configured for 10mV steps	0.9	--	2.0	V
Output Voltage Offset	V_{B2_ERR}		-1		1	%Vout
Line Regulation		VIN = 2.7V to 5.5V	--	0.5	--	%/V
Load Regulation		IOUT= 0 to OCL	--	0.5	--	%/A
Load Transient		VIN = 3.3V,VOUT = 1.2V, L = 0.47uH,COUT = 22uF. 1.Load = 1A to 2A @ 0.2A/us. 2.Load = 50mA to 1A @ 0.2A/us.	--	4	--	%Vout
UVP Threshold	V_{B2_UV}	Falling Threshold	87	90	93	%Vout
		hysteresis	--	3	--	%Vout
OVP Threshold	V_{B2_OV}	Rising Threshold	107	110	113	%Vout

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		hysteresis	--	3	--	%Vout

Electrical Characteristics(continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OCL Threshold	V_{B2_OC}	B2_IMAX = 00	1.5	2	--	A
		B2_IMAX = 01	2.5	3	--	A
		B2_IMAX = 10	3.5	4	--	A
		B2_IMAX = 11	4.5	5	--	A
Switching Frequency	f_{SW_B2}	B2_FREQ = 101	--	2	--	MHz
Soft-Start Time		B2_SST = 01	--	250	--	uS
PMOS On- Resistance	R_{DSON_B2P}	VIN_B2 = 3.3V	--	70	--	mΩ
NMOS On Resistance	R_{DSON_B2N}	VIN_B2 = 3.3V	--	40	--	mΩ
Output Discharge Res	R_{DISCH_B2}	VIN_B2 = 3.3V	--	10	--	Ω
efficiency	Eff_{B2}	AVIN = 3.3V,VOUT = 1.2V,IOUT=10mA	--	86	--	%
		AVIN = 3.3V,VOUT = 1.2V,IOUT=1A	--	89	--	%
		AVIN = 3.3V,VOUT = 1.2V,IOUT=2A	--	85	--	%
BUCK3						
Output Voltage range	V_{B3_VOUT}	Configured for 10mV steps	0.5	--	1.3	V
Output Voltage Offset	V_{B3_ERR}		-1		1	%Vout
Line Regulation		VIN = 2.7V to 5.5V	--	0.5	--	%/V
Load Regulation		IOUT= 0 to OCL	--	0.5	--	%/A
Load Transient		VIN = 3.3V,VOUT = 0.8V, L = 0.47uH,COUT = 22uFx2. Load = 2A to 4A @ 0.2A/us. Load = 50mA to 2A @ 0.2A/us.	--	4	--	%Vout
UVP Threshold	V_{B3_UV}	Falling Threshold	87	90	93	%Vout
		hysteresis	--	3	--	%Vout
OVP Threshold	V_{B3_OV}	Rising Threshold	107	110	113	%Vout
		hysteresis	--	3	--	%Vout
OCL Threshold	V_{B3_OC}	B3_IMAX = 00	3.5	4	--	A
		B3_IMAX = 01	4.5	5	--	A
		B3_IMAX = 10	5.5	6	--	A
		B3_IMAX = 11	6.5	7	--	A
Switching Frequency	f_{SW_B3}	B3_FREQ = 101	--	2	--	MHz
Soft-Start Time		B3_SST = 01	--	250	--	uS
PMOS On Resistance	R_{DSON_B3P}	VIN_B3 = 3.3V	--	45	--	mΩ
NMOS On Resistance	R_{DSON_B3N}	VIN_B3 = 3.3V	--	22	--	mΩ
Output Discharge Res	R_{DISCH_B3}	VIN_B3 = 3.3V	--	10	--	Ω
efficiency	Eff_{B3}	AVIN = 3.3V,VOUT = 0.8V,IOUT=1mA	--	80	--	%

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		AVIN = 3.3V,VOUT = 0.8V,IOUT=1A	--	88	--	%
		AVIN = 3.3V,VOUT = 0.8V,IOUT=2A	--	84	--	%

Electrical Characteristics(continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BUCK4						
Output Voltage range	V_{B4_VOUT}	Configured for 10mV steps	0.9	--	2.0	V
Output Voltage Offset	V_{B4_ERR}		-1		1	%Vout
Line Regulation		VIN = 2.7V to 5.5V	--	0.5	--	%/V
Load Regulation		IOUT= 0 to OCL	--	0.5	--	%/A
Load Transient		VIN = 3.3V,VOUT = 1.2V, L = 0.47uH,COUT = 22uF. Load = 1A to 2A @ 0.2A/us. Load = 50mA to 1A @ 0.2A/us.	--	4	--	%Vout
UVP Threshold	V_{B4_UV}	Falling Threshold	87	90	93	%Vout
		hysteresis	--	3	--	%Vout
OVP Threshold	V_{B4_OV}	Rising Threshold	107	110	113	%Vout
		hysteresis	--	3	--	%Vout
OCL Threshold	V_{B4_OC}	B4_IMAX = 00	1.5	2	--	A
		B4_IMAX = 01	2.5	3	--	A
		B4_IMAX = 10	3.5	4	--	A
		B4_IMAX = 11	4.5	5	--	A
Switching Frequency	f_{SW_B4}	B4_FREQ = 101	--	2	--	MHz
PMOS On Resistance	R_{DSON_B4P}	VIN_B4 = 3.3V	--	70	--	mΩ
NMOS On Resistance	R_{DSON_B4N}	VIN_B4 = 3.3V	--	45	--	mΩ
Output Discharge Res	R_{DISCH_B4}	VIN_B4 = 3.3V	--	10	--	Ω
efficiency	Eff_{B4}	AVIN = 3.3V,VOUT = 1.2V,IOUT=10mA	--	85	--	%
		AVIN = 3.3V,VOUT = 1.2V,IOUT=1A	--	89	--	%
		AVIN = 3.3V,VOUT = 1.2V,IOUT=2A	--	86	--	%
BUCK4 LDO Mode						
Output Voltage range	V_{B4LDO_VOUT}	Configured for 10mV steps	0.9	--	2.0	V
Output Voltage Offset	V_{B4LDO_ERR}		-1		1	%Vout
Line Regulation		VIN = 2.7V to 5.5V	--	0.5	--	%/V
Load Regulation		IOUT= 0 to OCL	--	0.5	--	%/A
Load Transient		VIN = 3.3V,VOUT = 1.8V, COUT = 2.2uF Load = 5mA to 50mA @ 0.2A/us Load=50mA to 100mA@ 0.2A/us.	--	4	--	%Vout

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UVP Threshold	V_{B4LDO_UV}	Falling Threshold	77	80	83	%Vout
		hysteresis	--	3	--	%Vout
OVP Threshold	V_{B4LDO_OV}	Rising Threshold	107	110	113	%Vout
		hysteresis	--	3	--	%Vout

Electrical Characteristics(continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OCL Threshold	V_{B4LDO_OC}	B4_LDO_IMAX = 0	--	0.4	--	A
		B4_LDO_IMAX = 1	--	0.5	--	A
Soft-Start Time			--	360	--	uS
Output Discharge Res	R_{DISCH_B4}	VIN_B4 = 3.3V	--	10	--	Ω
Foldback Current		MAX current when soft-start	--	40	--	%OCL
LDO1						
Output Voltage range	V_{LDO1_VOUT}	Configured for 10mV steps	1.0	--	3.3	V
Output Voltage Offset	V_{LDO1_ERR}		-1		1	%Vout
Line Regulation		VIN = 2.7V to 5.5V	--	0.5	--	%/V
Load Regulation		IOUT= 0 to OCL	--	0.5	--	%/A
Load Transient		VIN = 3.3V,VOUT = 1.8V, COUT = 2.2uF Load = 5mA to 50mA @ 0.2A/us Load=50mA to 100mA@0.2A/us.	--	3.5	--	%Vout
UVP Threshold	V_{LDO1_UV}	Falling Threshold	77	80	83	%Vout
		hysteresis	--	3	--	%Vout
OVP Threshold	V_{LDO1_OV}	Rising Threshold	107	110	113	%Vout
		hysteresis	--	3	--	%Vout
OCL Threshold	V_{LDO1_OC}	LDO1_ILIMSEL = 0	--	0.4	--	A
		LDO1_ILIMSEL = 1	--	0.5	--	A
Soft-Start Time			--	360	--	uS
Output Discharge Resistance	R_{DISCH_LDO1}	AVIN = 3.3V	--	16	--	Ω
Foldback Current			--	40	--	%OCL
LDO1 PMOS Load Switch Mode						
VIN_L1 Voltage			2.7	3.3	3.7	V
PMOS On Resistance	R_{DSON_L1P}	VIN_L1 = 3.3V	--	200	--	mΩ
OCL Threshold	V_{LSW1P_OC}	LDO1_ILIMSEL = 0	0.3	0.4	--	A
		LDO1_ILIMSEL = 1	0.4	0.5	--	A
UVP Threshold	V_{LSW1P_UV}	Falling Threshold	77	80	83	%Vout
		hysteresis	--	3	--	%Vout

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Foldback Current			--	40	--	%OCL
LDO1 NMOS Load Switch Mode						
VIN_LDO1 Voltage			0.4	--	AVIN-1	V
NMOS On Resistance	R_{DSON_L1N}	VIN_L1 = 0.4V，AVIN = 3.3V	--	50	--	mΩ
OCL Threshold	V_{LSW1N_OC}	LDO1_ILIMSEL = 0	--	0.6	--	A
		LDO1_ILIMSEL = 1	--	1.2	--	A
Foldback Current			--	40	--	%OCL

Electrical Characteristics(continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LDO2						
Output Voltage	V_{LDO2_VOUT}	LDO2 VID range	1.0	--	2.7	V
		step	--	50	--	mV
Output Voltage Accuracy	V_{LDO2_ERR}	GPIO6 = High	1.782	1.8	1.818	V
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		IOUT= 0 to OCL	--	0.5	--	%/A
Load Transient		VIN = 3.3V,VOUT = 1.8V, COUT = 2.2uF Load = 5mA to 50mA @ 0.2A/us Load=50mA to 100mA@0.2A/us.	-3.5	--	--	%Vout
UVP Threshold	V_{LDO2_UV}	Falling Threshold	77	80	83	%Vout
		hysteresis	--	3	--	%Vout
OVP Threshold	V_{LDO2_OV}	Rising Threshold	107	110	113	%Vout
		hysteresis	--	3	--	%Vout
OCL Threshold	V_{LDO2_OC}	LDO2_ILIMSEL = 0	0.3	0.4	--	A
		LDO2_ILIMSEL = 1	0.4	0.5	--	A
Soft-Start Time			--	360	--	uS
Output Discharge Resistance	R_{DISCH_LDO2}	AVIN = 3.3V	--	16	--	Ω
Foldback Current			--	40	--	%OCL
LDO2 Load Switch Mode						
PMOS On Resistance	R_{DSON_L1P}	AVIN = 3.3V	--	200	--	mΩ
OCL Threshold	V_{LSW2P_OC}	LDO2_ILIMSEL = 0	--	0.4	--	A
		LDO2_ILIMSEL = 1	--	0.5	--	A
UVP Threshold	V_{LSW2P_UV}	Falling Threshold	77	80	83	%Vout
		hysteresis	--	3	--	%Vout
Foldback Current			--	40	--	%OCL

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Electrical Characteristics(continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I2C INTERFACE						
SCL, SDA Input Low		AVIN = 3.3	--	--	0.4	V
SCL, SDA Input High		AVIN = 3.3	1.05	--	--	V
SDA Leakage Current		SDA = 3.3V	--	--	1	uA
SDA sink Current		SDA = 0.3V	5	--	--	mA
SCL Clock Frequency	f_{SCL}		--	--	3400	khz
SCL Low Period	t_{LOW}		125	--	--	nS
SCL High Period	t_{HIGH}		62.5	--	--	nS
SDA Data Setup Time	$T_{SU;DAT}$		10	--	--	nS
SDA Data Hold Time	$T_{HD;DAT}$		0	--	--	nS
Start Setup Time	$T_{SU;STA}$		65	--	--	nS
Stop Setup Time	$T_{SU;STO}$		65	--	--	nS
Capacitance on SCL or SDA Pin			--	--	10	pF
GPIO INTERFACE						
GPIOs Output Low (Open Drain)		AVIN = 3.3， R_{PULLUP}=10KΩ	--	--	0.2	V
GPIO2/3/4/6 Input High		AVIN = 3.3	2.3	--		V
GPIO2/3/4/6 Input High-z		AVIN = 3.3	0.9	--	1.1	V
GPIO2/3/4/6 Input Low		AVIN = 3.3	--	--	0.25	V
GPIO5/7/8 Input High		AVIN = 3.3	1.0	--		V
GPIO5/7/8 Input Low		AVIN = 3.3	--	--	0.5	V

NOTE1. Because of the Min Off-Time, the Switching Frequency will become lower than 1.8MHz when BUCK1 has a heavy load.

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7 Functional Description

7.1 Block Diagram

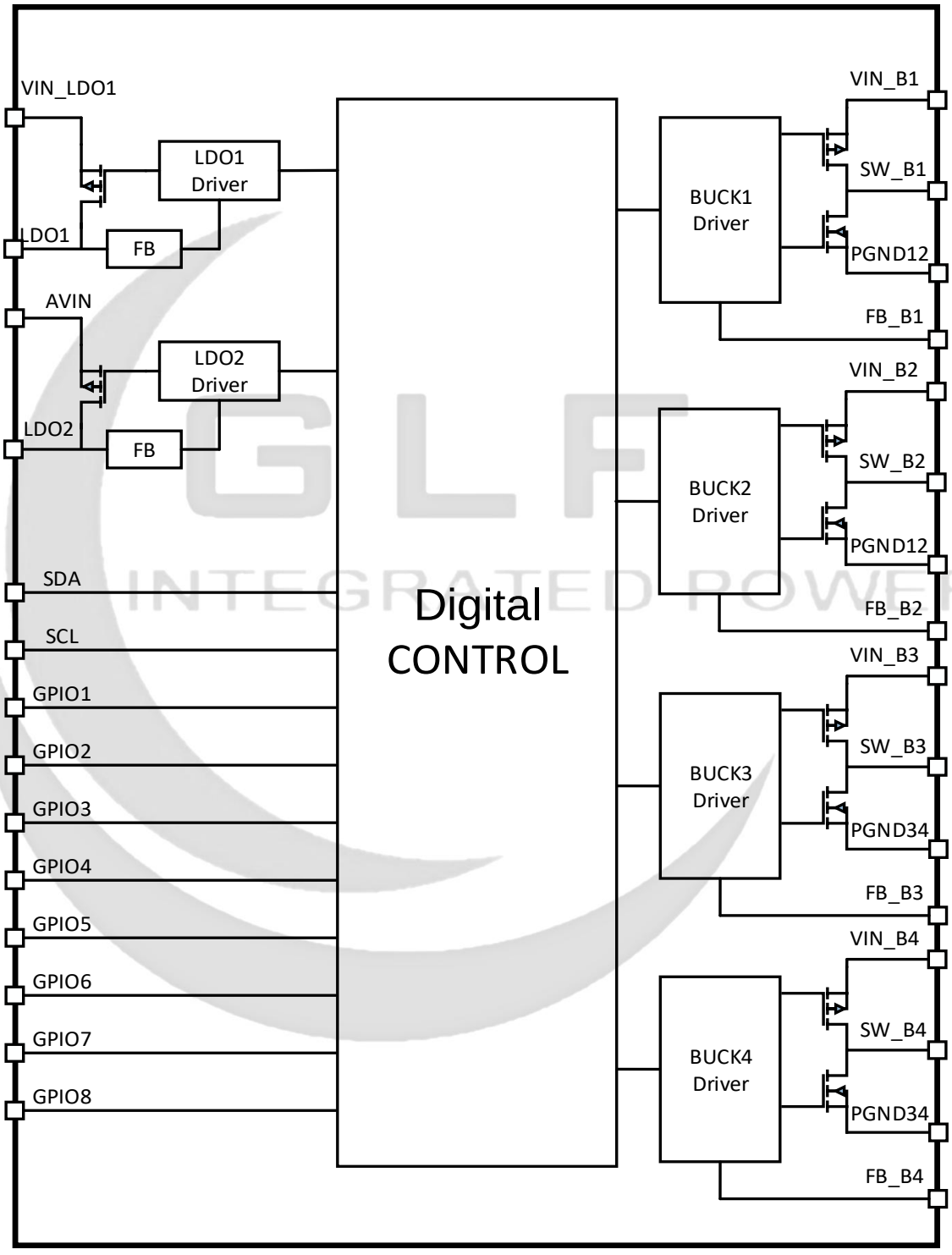

Figure 7-1. Block Diagram

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7.2 General

The GLF70581 is a power management IC (PMIC) with four highly efficient buck regulators and two LDOs. It provides enable signals and power-good signals to control external converters for expanding more rails to use. It contains a master controller that manages startup sequencing, voltages, sleep states, and fault conditions. Default output voltage can be changed by GPIO configuration.

7.3 Buck Converter

The GLF70581 contains four buck converters. Advanced control features such as advanced constant-on-time voltage mode (ACOT) provide fast transient response and low quiescent current. These buck converters are also built with standard protections, such as OVP, UVP, and OCL.

7.3.1 Buck Overvoltage Protection

The OVP (Overvoltage Protection) is a level detection mechanism. If the output voltage exceeds +10% of the reference voltage, overvoltage protection will be triggered, and both the high-side and low-side MOSFETs will be turned off immediately.

7.3.2 Buck Undervoltage Protection

The UVP is a level detection mechanism. If the output voltage falls below 10% of the reference voltage, undervoltage protection will be triggered, and both the high-side and low-side MOSFETs will be turned off immediately.

7.3.3 Buck Overcurrent Limit

The current limited architecture of all rails is designed to detect both peak and valley current. When the High-Side MOS turns on, the inductor current will be sensed from the RDS(ON) of the PMOS by an internal OC (overcurrent) circuit. If the inductor current exceeds the internal set current limit, the OC circuit will activate and force the High-Side MOS to turn off and the Low-Side MOS to turn on, in order to lower the inductor current. The Low-Side MOS will not turn off until the inductor current is lower than the internal release current. The OCL (overcurrent limit) current set by the register represents the average inductor current when the OC circuit is active. Once the inductor current falls below the OC level, the rail will return to normal operation.

7.4 Linear Dropout Regulator

The GLF70581 includes two linear dropout regulators (LDOs). The LDOs feature an independent current limit and both overvoltage and undervoltage protection circuits to prevent unexpected applications. When the path current exceeds the current-limit threshold, the current limit circuit adjusts the gate voltage of the power stage to limit the output current. If the output voltage is lower than −15% of the reference voltage, the LDO will be shut off immediately by the undervoltage protection (UVP) circuit. If the output voltage is higher than +10% of the reference voltage, the overvoltage protection (OVP) circuit will also shut off the LDO immediately.

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7.5 External Power Control

In addition to its six internal power rails, the GLF70581 can integrate two external power supplies into its power-up sequence. These external supplies are enabled via the EXT_EN1_O and EXT_EN2_O outputs. Setting GPIO.EXT_ENx_O = 1 activates the corresponding external supply.

After configuring a GPIO to function as an EXT_ENx_O output, its activation can be triggered through one of four selectable modes. These modes are selected via the EXT_ENx_O_INPUT_SEL field in the corresponding configuration register.

When EXT_ENx_O_INPUT_SEL = 00: The EXT_ENx_O output is triggered by the POK status of a selected rail. The target rail is specified by EXT_ENx_POK_SEL. During system power-up, when the selected rail's POK asserts, the GLF70581 asserts EXT_ENx_O = 1 after a delay period defined by EXT_ENx_O_DLY.

When EXT_ENx_O_INPUT_SEL = 01: The EXT_ENx_O output is triggered by the EXT_ENx_I signal (configurable via GPIO5/7/8). When EXT_ENx_I asserts to 1, the GLF70581 asserts EXT_ENx_O = 1 after a delay period defined by EXT_ENx_O_DLY.

When EXT_ENx_O_INPUT_SEL = 10: The EXT_ENx_O output is triggered by the GPIOx_GENERAL_CTRL register. Writing GPIOx_GENERAL_CTRL = 1 asserts EXT_ENx_O = 1 immediately.

When EXT_ENx_O_INPUT_SEL = 11: The EXT_ENx_O output is triggered by a delay timer configured via the EXT_ENx_O_TIME_SLOT register. During system power-up, when the TIME_SLOT delay expires, the GLF70581 asserts EXT_ENx_O = 1 after a further delay period defined by EXT_ENx_O_DLY.

Following successful enablement of an external supply, the EXT_PGx signals are monitored. If a power fault is detected without a manual shutdown command, EXT_PGx transitions from 1 to 0. This event initiates fault handling procedures according to register configurations, which may affect internal state machines and trigger a re-power sequence as required.

7.6 I2C Serial Interface

To ensure compatibility with a wide range of systems, the GLF70581 uses standard I2C commands. The GLF70581 always operates as a slave device, and its I2C slave address is 0x25. This serial interface supports the I2C protocol 2.1 with standard slave mode (100Kbps), fast mode (400Kbps), and high-speed mode (3.4Mbps). Multiple-byte reading or writing over the I2C interface of the GLF70581 can also be done with standard slave mode (100Kbps) and fast mode (400Kbps). When performing a multiple-byte read or write, the GLF70581 will automatically increment to the next address for subsequent bytes.

I2C commands are communicated via the SCL and SDA pins. SCL serves as the I2C serial clock input, while SDA functions as the data input and output. The SDA pin is of open-drain design and must be accompanied by a pullup resistor. Signals transmitted through these pins must adhere to the timing requirements specified in the Electrical Characteristics Table.

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The user can modify the output voltage, fault threshold, interrupt masks, and other settings via the I2C interface. There are three types of registers: Volatile Registers - These include R/W (Read and Write), RO (Read Only), and RC (Read and Clear). After a certain condition (e.g., AVIN exceeding a UVHL threshold), the user can modify the R/W register values to change the register functions. The RO registers provide information such as the status of rails and GLF70581 details, including various ID numbers. The RC type registers are special: reading a bit in these registers will clear that bit to 0. Any changes made to these volatile registers will be lost if AVIN falls below a UVLO (under-voltage lockout) threshold. The default values of these registers are fixed and cannot be modified.

Non-Volatile Registers - These registers possess Read/Write (R/W) functionality. Once the AVIN (Analog Voltage Input) exceeds the UVHL (Under-Voltage High Limit) threshold, the user can modify the R/W register values to adjust the register functions. However, any changes made to these non-volatile registers will be lost if the AVIN falls below the UVLO (Under-Voltage Lockout) threshold or there is a low-to-high transition on the PWREN GPIO (Power Enable General-Purpose Input/Output).

The default values of these registers can be modified at the factory to optimize the IC's functionality for specific applications. If you require custom configurations to meet your system requirements, please contact THINK FUTURE SEMICONDUCTOR for assistance.

7.7 GPIO CONFIGURATION

The GLF70581 has 8 configurable GPIOs. GPIO1 is fixed to the nRESET signal. GPIO2, GPIO3, GPIO4, and GPIO6 are 3-status GPIOs. GPIO5, GPIO7, and GPIO8 are 2-status GPIOs. Please see Table 7-1 for the description of all GPIOs' default functions.

Table 7-1. GPIO default function

GPIO	Default Functions
GPIO1	nRESET
GPIO2	B1 mode set and B1/B2 voltage set
GPIO3	B3 voltage set and B4/L1/L2 extra delay time set
GPIO4	L1/B4 mode and voltage set
GPIO5	nIRQ
GPIO6	LDO2 LDO/LS selection
GPIO7	PWRDIS
GPIO8	DPSLP

These GPIOs can be configured for many other functions, including: external enable, external power good, external enable input, PWRDIS, sleep mode, deep sleep mode, DVS control, input voltage monitoring, and input voltage warning.

7.7.1 GPIO status detection

All GPIOs have default functions. GPIO1 is fixed to the nRESET signal. GPIO2/3/4/6 have default functions before nRESET goes to a high level. When AVIN first goes above UVHL, the GLF70581 detects the status

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of GPIO2/3/4/6 and records the result. These functions can be changed to other functions by configuring GPIOx_CFG.GPIOx_FUNC_SEL.GPIO5/7/8 can select their default functions by configuring GPIOx_CFG.GPIOx_FUNC_SEL.

7.7.2 GPIO1

GPIO1 is fixed to the nRESET signal. After the power-up sequence, nRESET = H indicates that outputs related to the controller are power good, while nRESET = L indicates that one or more outputs related to the controller are power bad.

The nRESET_MASK_CFG0 provides the function to mask any output PBAD event. By setting the corresponding bits to “1” in the nRESET_MASK_REG register, nRESET will ignore any PBAD events on the rail. Any PBAD events on an unmasked rail will cause nRESET to go low. In addition, the Power Good delay time from the rising edge of the PG flag to the rising edge of nRESET can be set in the GPIO1_REG.POR_DELAY_TIME register.

7.7.3 GPIO2

GPIO2 has a default function, B1/B2 VSEL. Once the AVIN voltage exceeds the UVHL voltage, the selected default values of the B1/B2 VSEL functions will be recorded into the relevant register values, such as B1_CFG1 and B2_CFG1. Please see Table 7-2 for the description of B1/B2 VSEL.

Table 7-2. GPIO2 function

	GPIO2 status		
	high	**high-Z**	**low**
Buck1	LSW	b1_set0	b1_set1
Buck2	b2_set0	b2_set0	b2_set1

After the power-up sequence and when nRESET goes to a high level, the GPIO2 function can be changed to another function by configuring GPIO2_REG.GPIO2_FUNC_SEL. If GPIO2_FUNC_EN = 0, the GPIO2 function will not be changed.

7.7.4 GPIO3

GPIO3 has a default function, B3 VSEL, before nRESET = H. Once the AVIN voltage exceeds the “UVLO+HYS” voltage, the selected default value of the B3 VSEL function will be recorded immediately into the relevant register value, such as B3_SEL, as well as some delay times for other rails. Additionally, if the PMIC enters Deeper Sleep Mode (PS4), B3 VSEL will be set to Dynamic Voltage Scaling (DVS) mode, such as B3_DVS. Please see Table 2 for the description of B3 VSEL.

Table 7-3. GPIO3 function

	GPIO3 status		
	high	**high-Z**	**low**

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Buck3	B3_sel	b3_set0	b3_set1	b3_set2
Power Up Extra Delay Time for B4/ L1/ L2	B4_EXT_DLY	B4_EXT_DLY_SET0	B4_EXT_DLY_SET1	B4_EXT_DLY_SET2
	LD1_EXT_DLY	LD1_EXT_DLY_SET0	LD1_EXT_DLY_SET1	L1_EXT_DLY_SET2
	LD2_EXT_DLY	LD2_EXT_DLY_SET0	LD2_EXT_DLY_SET1	L2_EXT_DLY_SET2

After the power-up sequence and when nRESET goes to a high level, the GPIO3 function can be changed to another function by configuring GPIO3_REG.GPIO3_FUNC_SEL. If GPIO3_FUNC_EN = 0, the GPIO3 function will not be changed.

7.7.5 GPIO4

GPIO4 has a default function, L1/B4 VSEL. Once the AVIN voltage exceeds the UVHL voltage, the selected default values of the L1/B4 VSEL functions will be recorded into the relevant register values, such as B4_CFG1 and LDO1_CFG1. Please see Table 7-4 for the description of L1/B4 VSEL.

Table 7-4. GPIO4 function

	GPIO4 status		
	high	**high-Z**	**low**
Buck4	b4_set0	LDO/b4_ldo_sel	b4_set1
L1	ldo1_set0	PLSW/NLSW	ldo1_set1

After the power-up sequence and when nRESET goes to a high level, the GPIO4 function can be changed to another function by configuring GPIO4_REG.GPIO4_FUNC_SEL. If GPIO4_FUNC_EN = 0, the GPIO4 function will not be changed.

7.7.6 GPIO6

GPIO6 has a default function, LDO2 MODE. Once the AVIN voltage exceeds the UVHL voltage, the selected default value for the LDO2 MODE function will be recorded in the relevant register value, such as LDO2_CFG. Please see Table 7-5 for the description of LDO2 MODE.

Table 7-5. GPIO6 function

	GPIO6 status		
	high	**——**	**low**
L2	LDO/ldo2_sel	——	PLSW

7.7.7 GPIO5/7/8

The default function of GPIO5/7/8 is decided by the default register value of GPIOx_CFG.GPIOx_FUNC_SEL. The GLF70581 applies these functions, which can be assigned to GPIO5/7/8 pins. GPIO5/7/8 will serve as the enable/disable controlled signal for the selected function, as shown in Table 7-6. In addition, GPIO2/3/4/6 can also be adjusted to the functions shown in Table 7-6 after nRESET = H.

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Table 7-6. GPIO2~8 function

GPIOx_FUNC_SEL	I/O	FUNC_NAME	Function Descriptions
0x0	O	General IO1 (as EXT_EN1_O)	General Purpose I/O1 is as the EXT_EN1_O for external enable signal.
0x1	O	General IO2 (as EXT_EN2_O)	General Purpose I/O2 is as the EXT_EN2_O for external enable signal.

(continued)

GPIOx_FUNC_SEL	I/O	FUNC_NAME	Function Descriptions
0x2	O	nIRQ	As interrupt signal.
0x3	I	Sleep Mode (PS3.5)	As the controlled signal for SLEEP. High = Wake up from SLEEP Mode Low = Enable SLEEP Mode
0x4	I	Deeper Sleep Mode(PS4)	As the controlled signal for DPSLEEP. High = Wake up from DPSLP Mode Low = Enable DPSLP Mode
0x5	I	B1/B2 enable/disable	As the signal for controlling B1/B2. High = Enable B1/B2 Low = Disable B1/B2
0x6	I	PWRDIS	As the Power Disable signal for controlling GLF70581. High = Disable GLF70581 Low = Enable GLF70581
0x7	I	EXT_EN1_I	Input Signal for EXT_EN1_O. High = EXT_EN1_O will go high. Low = No action.
0x8	I	EXT_EN2_I	Input Signal for EXT_EN2_O. High = EXT_EN2_O will go high. Low = No action.
0x9	O	SYSMON	High = AVIN > SYSMON Low = AVIN < SYSMON
0xa	O	SYSWARN	High = AVIN > SYSWARN Low = AVIN < SYSWARN
0xb	I	B3_DVS	As the signal for controlling B3 voltage. High = B3 voltage is b3_sel Low = B3 voltage is b3s_sel
0xc	I	EXT_PG1	Input Signal for EXT1 power good
0xd	I	EXT_PG2	Input Signal for EXT2 power good

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7.8 STATE MACHINE

The GLF70581 contains an internal state machine with six states. The definitions of the states described below are related to various signals, such as AVIN, POWER_DIS, Sleep1, Sleep2, and some related register settings. The following are the classifications of the states.

7.8.1 Off State

If the AVIN voltage drops below the "UVLO + HYS" threshold from 0V, all the internal circuits of the GLF70581 will not function in this state.

7.8.2 Standby State

If AVIN is between the “UVLO + HYS” voltage and the SYSMON voltage, or if AVIN is over the AVIN_OV voltage, the internal digital controller of the GLF70581 starts to work. Once the digital core is active, it will process the step of detecting GPIO status and reloading register values from the efuses configuration. After completing the reload step, any register function value can still be modified via the I2C interface. In addition, the GLF70581 also remains in the “Standby State” when the AVIN range is within normal operation with PWRDIS = H.

7.8.3 Normal State

If AVIN is within the range between the SYSMON voltage and the VIN OVP voltage, and POWER_DIS = L, the rails will follow their GPIOs' settings and their internal configurations for the turn-on delay functions (x_ON_DLY) and the soft-start time functions (x_SST_SEL) to perform the power-up sequence. Once the nRESET signal rises to a high level, the GLF70581 receives the power good flags and remains in the Normal State. The above description covers the transition from standby state to normal state.

In the Normal State, a rail can be controlled to turn ON/OFF by configuring the x_EN register function. If the rail powers up by setting x_EN from b0 to b1, it will simply follow the x_SST_SEL function setting to immediately initiate soft-start, ignoring any configured delay time.

7.8.4 Sleep State

When the GLF70581 is operating in the Normal State, it will transition to the SLEEP/DPSLP State if one of the following conditions is met:

1. A GPIOx that is configured for the SLEEP/DPSLP function transitions from high voltage to low voltage. This will cause the state machine of the GLF70581 to enter the SLEEP/DPSLP State.

2. If SLP_CFG.SLP_EN or DPSLP_CFG.DPSLP_EN is set to b1, the state machine of the GLF70581 will transition to the SLEEP/DPSLP State

When the GLF70581 changes from normal mode to sleep mode, the rails will follow the SLP_CFG/DPSLP_CFG settings to power off. Specifically, only Buck3 can change its voltage from B3_SEL to B3_DVS_SEL if Buck3 remains active when entering DPSLP mode. All active rails will disable

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some internal circuits to enter a low-power mode, reducing the VIN supply current for power saving when the GLF70581 is in Sleep State. The GLF70581 can easily return to normal state from sleep state by disabling the sleep mode condition. To return to normal state, the disabled rails will follow their WAKEUP_DELAY function and SST_SEL function to perform their wake-up sequence.

7.8.5 Thermal Recovery State

When the die temperature of the GLF70581 reaches a critical overtemperature event (approximately 150℃), all the rails are forced to power off, but the digital controller remains active. The PMIC remains in the Thermal Recovery State. The PMIC will return to the normal state when the die temperature drops below 125℃.

In addition, the PMIC also remains in the Thermal Recovery State when AVIN is greater than VINOV. The PMIC will return to the normal state when AVIN is less than OVHL.

7.8.6 Hiccup State

If any rail get the fault flag for an overvoltage event or undervoltage event, GLF70581 will go into Hiccup State and all rails will power off. After the retry times are up (default 200ms), the PMIC will go back to normal state.

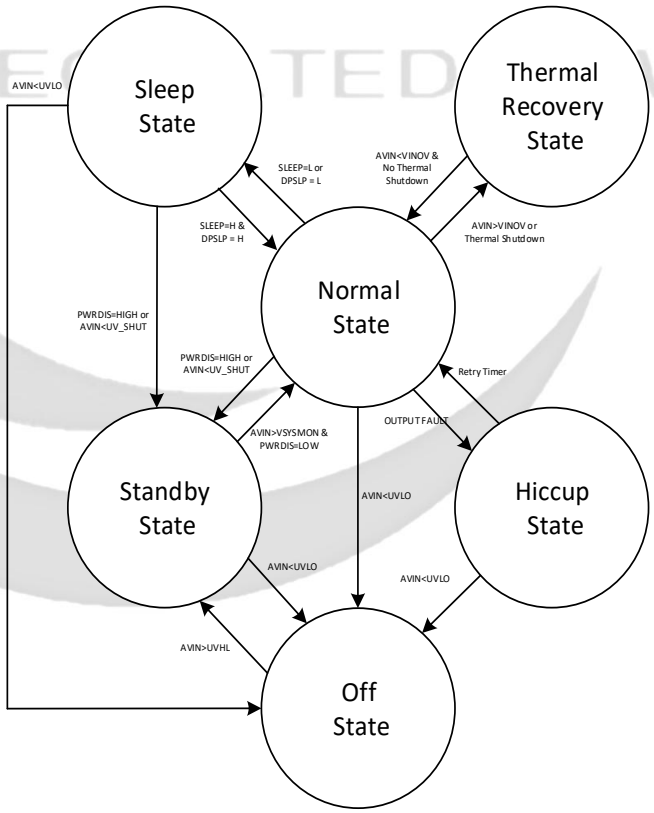

Figure 7-2. State Machine

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7.9 Registers

7.9.1 Register Attribute Description

Attribute	Description
R	This bit can be read by host. Write has no effect.
RC	This bit can be read by host and will be clear to '0' after read.Write has no effect.
RW	This bit can be read or written by host.
RWE	This bit can be read or written by the host, and its default value can be customized.

7.9.2 TOP_STAT

Address: 00h Reset: 00h

Bit	Name	Attribute	Default	Description
7	VSYSMON	R	0	Real Time bit. Indicates VIN > VSYSMON
6	VSYSWARN	R	0	Real Time bit. Indicates VIN > VSYSWARN
5	POK_OV	R	0	Real Time bit. Indicates VIN > POK_OV
4	VIN_OV	R	0	Real Time bit. Indicates VIN OV
3	OT_WARN	R	0	Real Time bit. Indicates OT_WARN on PMIC
2	OT_PMIC	R	0	Real Time bit. Indicates PMIC OT
1	nRESET	R	0	Real Time bit. Indicates nRESET = 1
0	IRQ	R	0	Real Time bit. Indicates IRQ = 1. (nIRQ = 0)

7.9.3 IRQ_PD0

Address: 01h Reset: 00h

Bit	Name	Attribute	Default	Description
7	B1_UV	RC	0	This bit will be set to 1 when BUCKx_UV happens. This bit will be cleared after read.
6	B2_UV	RC	0	
5	B3_UV	RC	0	
4	B4_UV	RC	0	
3	LDO1_UV	RC	0	This bit will be set to 1 when LDOx_UV happens. This bit will be cleared after read.
2	LDO2_UV	RC	0	
1	VSYSMON_UV	RC	0	This bit will be set to 1 when AVIN<VSYSMON. This bit will be cleared after read.
0	VSYSWARN_UV	RC	0	This bit will be set to 1 when AVIN<VSYSWARN. This bit will be cleared after read.

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7.9.4 IRQ_PD1

Address: 02h Reset: 00h

Bit	Name	Attribute	Default	Description
7	B1_OV	RC	0	This bit will be set to 1 when BUCKx_OV happens. This bit will be cleared after read.
6	B2_OV	RC	0	
5	B3_OV	RC	0	
4	B4_OV	RC	0	
3	LDO1_OV	RC	0	This bit will be set to 1 when LDOx_OV happens. This bit will be cleared after read.
2	LDO2_OV	RC	0	
1	POK_OV	RC	0	This bit will be set to 1 when AVIN>POK_OV. This bit will be cleared after read.
0	VIN_OV	RC	0	This bit will be set to 1 when AVIN>VIN_OV. This bit will be cleared after read.

7.9.5 RAIL_POK_STAT

Address: 03h Reset: 00h

Bit	Name	Attribute	Default	Description
7	B1_POK	R	0	Real time for rail's flag bit. Indicates POK on BUCK1.
6	B2_POK	R	0	Real time for rail's flag bit. Indicates POK on BUCK2.
5	B3_POK	R	0	Real time for rail's flag bit. Indicates POK on BUCK3.
4	B4_POK	R	0	Real time for rail's flag bit. Indicates POK on BUCK4.
3	LDO1_POK	R	0	Real time for rail's flag bit. Indicates POK on LDO1.
2	LDO2_POK	R	0	Real time for rail's flag bit. Indicates POK on LDO2.
1	EXT1_POK	R	0	Real time for rail's flag bit. Indicates POK on EXT1.
0	EXT2_POK	R	0	Real time for rail's flag bit. Indicates POK on EXT2.

7.9.6 IRQ_PD2

Address: 04h Reset: 00h

Bit	Name	Attribute	Default	Description
7	B1_OC	RC	0	This bit will be set to 1 when BUCKx_OC happens. This bit will be cleared after read.
6	B2_OC	RC	0	
5	B3_OC	RC	0	
4	B4_OC	RC	0	
3	LDO1_OC	RC	0	This bit will be set to 1 when LDOx_OV happens. This bit will be cleared after read.
2	LDO2_OC	RC	0	
1	OT_WARN	RC	0	This bit will be set to 1 when temperature upon OT_WARN. This bit will be cleared after read.
0	OT_PMIC	RC	0	This bit will be set to 1 when temperature upon OT. This bit will be cleared after read.

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7.9.7 GPIO1_CFG

Address: 05h Reset: 04h

Bit	Name	Attribute	Default	Description
7	GPIOTRI_REDET_EN	RWE	0	Whether tri-state GPIO redetect when GLF70581 return to STANDBY mode. 0 : don't redetect 1 : redetect
6:3	RSV	R	0000	reserved
2:0	NRESET_DLY	RWE	100	The timing from the POK signal of rail which determine nRESET signal in the power up sequence to nRESET signal. 000 : delay 0.5ms. 001 : delay 1ms. 010 : delay 2ms. 011 : delay 4ms. 100 : delay 8ms. (default) 101 : delay 16ms. 110 : delay 32ms. 111 : delay 64ms

7.9.8 GPIO2_CFG0

Address: 06h Reset: 40h

Bit	Name	Attribute	Default	Description
7	GPIO2_FUNC_EN	RWE	0	GPIO2 has an initial function before nRESET=1. This bit can disable the function of "GPIO2_FUNC_SEL" after nRESET=1. 0: disable 1: enable
6:3	GPIO2_FUNC_SEL	RW	1000	0000 : General IO1 (as EXT_EN1_O output) 0001 : General IO2 (as EXT_EN2_O output) 0010 : nIRQ (output) 0011 : Sleep Mode (input) 0100 : Deeper Sleep Mode (input) 0101 : B1/B2 enable/disable (input) 1000 : Nothing (default) 1001 : SYSMON 1010 : SYSWARN 1011 : DVS 1100 : EXT_PG1 (input) 1101 : EXT_PG2 (input)

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2:1	GPIO2_INIT_STAT	R	00	00 : low 01 : high-Z 11 : high
0	GPIO2_GENERAL_CTRL	RW	0	If the function selection is as “General IO1/2”, these bits can control the voltage level of the General IO1/2. 00 : low level 01 : high level

7.9.9 GPIO3_CFG0

Address: 07h Reset: 40h

Bit	Name	Attribute	Default	Description
7	GPIO3_FUNC_EN	RW	0	GPIO3 has an initial function before nRESET=1. This bit can disable the function of “GPIO2_FUNC_SEL” after nRESET=1. 0: disable 1: enable
6:3	GPIO3_FUNC_SEL	RWE	1000	0000 : General IO1 (as EXT_EN1_O output) 0001 : General IO2 (as EXT_EN2_O output) 0010 : nIRQ (output) 0011 : Sleep Mode (input) 0100 : Deeper Sleep Mode (input) 0101 : B1/B2 enable/disable (input) 1000 : Nothing (default) 1001 : SYSMON 1010 : SYSWARN 1011 : B3_DVS 1100 : EXT_PG1 (input) 1101 : EXT_PG2 (input)
2:1	GPIO3_INIT_STAT	R	00	00: low 01: high-Z 11:high
0	GPIO3_GENERAL_CTRL	RW	0	If the function selection is as “General IO1/2”, these bits can control the voltage level of the General IO1/2. 00 : low level 01 : high level

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7.9.10 GPIO4_CFG0

Address: 08h Reset: 40h

Bit	Name	Attribute	Default	Description
7	GPIO4_FUNC_EN	RW	0	GPIO4 has an initial function before nRESET=1. This bit can disable the function of “GPIO2_FUNC_SEL” after nRESET=1. 0: disable 1: enable
6:3	GPIO4_FUNC_SEL	RWE	1000	0000 : General IO1 (as EXT_EN1_O output) 0001 : General IO2 (as EXT_EN2_O output) 0010 : nIRQ (output) 0011 : Sleep Mode (input) 0100 : Deeper Sleep Mode (input) 0101 : B1/B2 enable/disable (input) 1000 : Nothing (default) 1001 : SYSMON 1010 : SYSWARN 1011 : B3_DVS 1100 : EXT_PG1 (input) 1101 : EXT_PG2 (input)
2:1	GPIO4_INIT_STAT	R	00	00 : low 01 : high-Z 11 : high
0	GPIO4_GENERAL_CTRL	RW	0	If the function selection is as “General IO1/2”, these bits can control the voltage level of the General IO1/2. 00 : low level 01 : high level

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7.9.11 GPIO5_CFG

Address: 09h Reset: 10h

Bit	Name	Attribute	Default	Description
7	RSV	R	0	reserved
6:3	GPIO5_FUNC_SEL	RWE	0010	0000 : General IO1 (as EXT_EN1_O output) 0001 : General IO2 (as EXT_EN2_O output) 0010 : nIRQ (output) (default) 0011 : Sleep Mode (input) 0100 : Deeper Sleep Mode (input) 0101 : B1/B2 enable/disable (input) 0110 : PWRDIS (input) 0111 : EXT_EN1_I (input) 1000 : EXT_EN2_I (input) 1001 : SYSMON 1010 : SYSWARN 1011 : B3_DVS 1100 : EXT_PG1 (input) 1101 : EXT_PG2 (input)
2:1	RSV	R	00	reserved
0	GPIO5_GENERAL_CTRL	RW	0	If the function selection is as “General IO1/2”, these bits can control the voltage level of the General IO1/2. 00 : low level 01 : high level

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7.9.12 GPIO6_CFG

Address: 0Ah Reset: 40h

Bit	Name	Attribute	Default	Description
7	GPIO6_FUNC_EN	RW	0	GPIO6 has an initial function before nRESET=1. This bit can disable the function of “GPIO2_FUNC_SEL” after nRESET=1. 0: disable 1: enable
6:3	GPIO6_FUNC_SEL	RWE	1000	0000 : General IO1 (as EXT_EN1_O output) 0001 : General IO2 (as EXT_EN2_O output) 0010 : nIRQ (output) 0011 : Sleep Mode (input) 0100 : Deeper Sleep Mode (input) 0101 : B1/B2 enable/disable (input) 1000 : Nothing (default) 1001 : SYSMON 1010 : SYSWARN 1011 : DVS 1100 : EXT_PG1 (input) 1101 : EXT_PG2 (input)
2:1	GPIO6_INIT_STAT	R	00	00: low 01: high-Z 11:high
0	GPIO6_GENERAL_CTRL	RW	0	If the function selection is as “General IO1/2”, these bits can control the voltage level of the General IO1/2. 00 : low level 01 : high level

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7.9.13 GPIO7_CFG

Address: 0Bh Reset: 30h

Bit	Name	Attribute	Default	Description
7	RSV	R	0	reserved
6:3	GPIO7_FUNC_SEL	RWE	0110	0000 : General IO1 (as EXT_EN1_O output) 0001 : General IO2 (as EXT_EN2_O output) 0010 : nIRQ (output) 0011 : Sleep Mode (input) 0100 : Deeper Sleep Mode (input) 0101 : B1/B2 enable/disable (input) 0110 : PWRDIS (input) 0111 : EXT_EN1_I (input) 1000 : EXT_EN2_I (input) 1001 : SYSMON 1010 : SYSWARN 1011 : B3_DVS 1100 : EXT_PG1 (input) 1101 : EXT_PG2 (input)
2:1	RSV	R	00	reserved
0	GPIO7_GENERAL_CTRL	RW	0	If the function selection is as “General IO1/2”, these bits can control the voltage level of the General IO1/2. 00 : low level 01 : high level

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7.9.14 GPIO8_CFG

Address: 0Ch Reset: 20h

Bit	Name	Attribute	Default	Description
7	RSV	R	0	reserved
6:3	GPIO8_FUNC_SEL	RWE	0100	0000 : General IO1 (as EXT_EN1_O output) 0001 : General IO2 (as EXT_EN2_O output) 0010 : nIRQ (output) 0011 : Sleep Mode (input) 0100 : Deeper Sleep Mode (input) 0101 : B1/B2 enable/disable (input) 0110 : PWRDIS (input) 0111 : EXT_EN1_I (input) 1000 : EXT_EN2_I (input) 1001 : SYSMON 1010 : SYSWARN 1011 : B3_DVS 1100 : EXT_PG1 (input) 1101 : EXT_PG2 (input)
2:1	RSV	R	00	reserved
0	GPIO8_GENERAL_CTRL	RW	0	If the function selection is as “General IO1/2”, these bits can control the voltage level of the General IO1/2. 00 : low level 01 : high level

7.9.15 GPIO3_DLY_CFG0

Address: 0Dh Reset: 00h

Bit	Name	Attribute	Default	Description
7:2	B4_EXT_DLY	RWE	000000	000000 : 0ms 000001 : 0.25ms ... 111111 : 15.75ms
1:0	LD1_EXT_DLY[3:2]	RWE	00	0000 : 0ms 0001 : 0.25ms ... 1111 : 3.75ms

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7.9.16 GPIO3_DLY_CFG1

Address: 0Eh Reset: 00h

Bit	Name	Attribute	Default	Description
7:6	LD1_EXT_DLY[1:0]	RWE	00	0000 : 0ms (default) 0001 : 0.25ms ... 1111 : 3.75ms
5:0	LD2_EXT_DLY	RWE	000000	000000 : 0ms (default) 000001 : 0.25ms ... 111111 : 15.75ms

7.9.17 WARN_CFG0

Address: 0Fh Reset: 00h

Bit	Name	Attribute	Default	Description
7:4	syswarn_sel	RW	0000	Vth of the SYSWARN falling selection: 0000 : 2775mV 0001 : 2800mV ... 1111 : 3150mV
3:0	sysmon_sel	RW	0000	Vth of the SYSMON selection: 0000 : 2725mV 0001 : 2750mV ... 1111 : 3100mV

7.9.18 WARN_CFG1

Address: 10h Reset: 44h

Bit	Name	Attribute	Default	Description
7	RSV	R	0	reserved
6:5	pok_ov_sel	RWE	10	Vth of the AVIN OV WARNING signal selection: 00 : 3.50V 01 : 3.60V 10 : 3.70V 11 : 3.80V
4:3	RSV	R	00	reserved
2:1	vin_ov_sel	RWE	10	Vth of the AVIN OV fault signal selection: 00 : 3.70V 01 : 3.80V

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				10 : 3.90V 11 : 4.00V
0	RSV	R	0	reserved

7.9.19 nRESET_MASK_CFG0

Address: 11h Reset: DFh

Bit	Name	Attribute	Default	Description
7	B1_PBAD	RWE	1	Mask the nRESET signal to react the rail's PBAD event. 0: not mask 1: mask
6	B2_PBAD	RWE	1	
5	B3_PBAD	RWE	0	
4	B4_PBAD	RWE	1	
3	LDO1_PBAD	RWE	1	
2	LDO2_PBAD	RWE	1	
1	EXT1_PBAD	RWE	1	
0	EXT2_PBAD	RWE	1	

7.9.20 irq_MASK0

Address: 12h Reset: FFh

Bit	Name	Attribute	Default	Description
7	B1_irq_mask	RW	1	mask the rail's PBAD interrupt flag 0 : does not mask the interrupt flag of the event 1 : mask the interrupt flag of the event
6	B2_irq_mask	RW	1	
5	B3_irq_mask	RW	1	
4	B4_irq_mask	RW	1	
3	LDO1_irq_mask	RW	1	
2	LDO2_irq_mask	RW	1	
1	VSYSMON_UV	RW	1	Only mask the interrupt flag of the exception bit and the function will still work well. 0 : does not mask the interrupt flag of the event 1 : mask the interrupt flag of the event
0	VSYSWARN_UV	RW	1	

7.9.21 irq_MASK1

Address: 13h Reset: 7Fh

Bit	Name	Attribute	Default	Description
7	RSV	R	0	reserved
6	sleep_irq_mask	RW	1	irq mask when system is in sleep/deep sleep 1 : mask irq when system is in sleep/deep sleep 0 : not mask irq when system is in sleep/deep sleep
5	EXT1_irq_mask	RW	1	mask the rail's interrupt flag 0 : does not mask the interrupt flag of the event

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4	EXT2_irq_mask	RW	1	1 : mask the interrupt flag of the event
3	OT_WARN	RW	1	Only mask the interrupt flag of the exception bit and the function will still work well. 0 : does not mask the interrupt flag of the event 1 : mask the interrupt flag of the event
2	OT_PMIC	RW	1	
1	POK_OV	RW	1	
0	VIN_OV	RW	1	

7.9.22 EXT_EN1_O_CFG0

Address: 14h Reset: 07h

Bit	Name	Attribute	Default	Description
7	EXT1_PBAD	RC	0	This bit will be set to 1 when external power PBAD happens. This bit will be cleared after read.
6	EXT2_PBAD	RC	0	
5	RSV	R	0	reserved
4:0	EXT_EN1_O_TIME_SLOT	RWE	00111	EXT_EN1_O POWER ON sequence 00000 : Time Slot0 (0us) 00001 : Time Slot1 (250us) … 00111 : Time Slot7 (1750us) ... 11111 : Time Slot31 (7750us)

7.9.23 EXT_EN2_O_CFG0

Address: 15h Reset: 07h

Bit	Name	Attribute	Default	Description
7:5	RSV	R	000	reserved
4:0	EXT_EN2_O_TIME_SLOT	RWE	00111	EXT_EN2_O POWER ON sequence 00000 : Time Slot0 (0us) 00001 : Time Slot1 (250us) … 00111 : Time Slot7 (1750us) ... 11111 : Time Slot31 (7750us)

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7.9.24 EXT_EN1_O_CFG2

Address: 16h Reset: C0h

Bit	Name	Attribute	Default	Description
7:6	EXT_EN1_O_INPUT_SEL	RWE	11	EXT_EN1_O follows the below selected signal and issue the high level voltage signal with a delay time. 00 : Rails' POK 01 : EXT_EN1_I 10 : I2C Interface. (as General IO1/2) 11 : EXT_EN1_O_TIME_SLOT
5:3	EXT_EN1_POK_SEL	RWE	000	000 : B1 001 : B2 010 : B3 011 : B4 100 : L1 101 : L2 110 : nRESET 111 : VSYSMON
2:0	RSV	R	000	reserved

7.9.25 EXT_EN2_O_CFG2

Address: 17h Reset: C0h

Bit	Name	Attribute	Default	Description
7:6	EXT_EN2_O_INPUT_SEL	RWE	11	EXT_EN2_O follows the below selected signal and issue the high level voltage signal with a delay time. 00 : Rails' POK 01 : EXT_EN1_I 10 : I2C Interface. (as General IO1/2) 11 : EXT_EN1_O_TIME_SLOT
5:3	EXT_EN2_POK_SEL	RWE	000	000 : B1 001 : B2 010 : B3 011 : B4 100 : L1 101 : L2 110 : nRESET 111 : VSYSMON
2:0	RSV	R	000	reserved

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7.9.26 EXT_ENx_O_CFG1

Address: 18h Reset: 00h

Bit	Name	Attribute	Default	Description
7:4	EXT_EN2_O_DLY	RWE	0000	If the following signal is Rail's POK, EXT_EN2_I or Time_Slot, EXT_EN2_O will issue from low to high with below delay time. 0000 : 0ms 0001 : 0.25ms 0010 : 0.5ms 0011 : 0.75ms ... 1111 : 3.75ms
3:0	EXT_EN1_O_DLY	RWE	0000	If the following signal is Rail's POK, EXT_EN1_I or Time_Slot, EXT_EN1_O will issue from low to high with below delay time. 0000 : 0ms (default) 0001 : 0.25ms 0010 : 0.5ms 0011 : 0.75ms ... 1111 : 3.75ms

7.9.27 SST_CFG0

Address: 19h Reset: 55 h

Bit	Name	Attribute	Default	Description
7:6	B1_SST<1:0>	RWE	01	Soft-start time for B1 00 : 125us, 01 : 250us, 10 : 500us, 11 : 750us
5:4	B2_SST<1:0>	RWE	01	Soft-start time for B2 00 : 125us, 01 : 250us, 10 : 500us, 11 : 750us
3:2	B3_SST<1:0>	RWE	01	Soft-start time for B3 00 : 125us, 01 : 250us, 10 : 500us, 11 : 750us
1:0	B4_SST<1:0>	RWE	01	Soft-start time for B4 00 : 125us, 01 : 250us, 10 : 500us, 11 : 750us

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7.9.28 SST_CFG1

Address: 1Ah Reset: 00h

Bit	Name	Attribute	Default	Description
7	ldo1_sst_sel	RWE	0	Soft-start time for ldo1 0 : 250us, 1 : 500us
6	Ldo2_sst_sel	RWE	0	Soft-start time for ldo2 0 : 250us, 1 : 500us
5:0	RSV	R	000000	reserved

7.9.29 B1_CFG0

Address: 1Bh Reset: 4Ah

Bit	Name	Attribute	Default	Description
7:6	b1_imax	RWE	01	00 : 4A ,01 : 5A 10 : 6A ,11 : 7A
5	b1_disres	RWE	0	buck1 discharge resistance value 0: 4 ohm 1: 10 ohm
4	RSV	R	0	reserved
3:1	b1_freq	RWE	101	000 to 011 : 1MHz 100 : 1.5MHz 101 : 2MHz 110 : 2.5MHz 111 : 3MHz
0	RSV	R	0	reserved

7.9.30 B1_CFG1

Address: 1Ch Reset: A0h

Bit	Name	Attribute	Default	Description
7:2	b1_sel_reg	RWE	101000	000000: 1.7V 000001: 1.72V … 101000: 2.50V ... 111100: 2.90V
1:0	RSV	R	00	reserved

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7.9.31 B2_CFG0

Address: 1Dh Reset: 4Ah

Bit	Name	Attribute	Default	Description
7:6	B2_imax	RWE	01	00 : 2A ,01 : 3A 10 : 4A ,11 : 5A
5:4	RSV	R	00	reserved
3:1	B2_freq	RWE	101	000 to 011 : 1MHz 100 : 1.5MHz 101 : 2MHz 110 : 2.5MHz 111 : 3MHz
0	RSV	R	0	reserved

7.9.32 B2_CFG1

Address: 1E h Reset: 3C h

Bit	Name	Attribute	Default	Description
7:1	B2_sel_reg	RWE	0011110	0000000 : 0.9V 0000001 : 0.91V … 0011110 : 1.2V … 1101110 ~1111111 : 2.0V
0	RSV	R	0	reserved

7.9.33 B3_CFG0

Address: 1Fh Reset: 6Ah

Bit	Name	Attribute	Default	Description
7:6	B3_imax	RWE	01	00 : 4A ,01 : 5A 10 : 6A ,11 : 7A
5:4	b3_tstep	RWE	10	00 : DVID up:20mV/us , DVID down:5mV/us 01 : DVID up:15mV/us , DVID down:5mV/us 10 : DVID up:10mV/us , DVID down:5mV/us 11 : DVID up:5mV/us , DVID down:5mV/us
3:1	B3_freq	RWE	101	000 to 011 : 1MHz 100 : 1.5MHz 101 : 2MHz 110 : 2.5MHz 111 : 3MHz
0	B3_DVS_EN	RW	0	0: BUCK3 voltage will be configured as b3s_sel_reg

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				1: BUCK3 voltage will be configured as b3_sel_reg

7.9.34 B3_CFG1

Address: 20 h Reset: 3C h

Bit	Name	Attribute	Default	Description
7:1	B3_sel_reg	RWE	0011110	0000000 : 0.5V 0000001 : 0.51V … 0011110 : 0.8V … 1010000 ~1111111 : 1.3V
0	RSV	R	0	reserved

7.9.35 B3_CFG2

Address: 21 h Reset: 32 h

Bit	Name	Attribute	Default	Description
7:1	b3s_sel_reg	RWE	0011001	0000000 : 0.5V 0000001 : 0.51V … 0011001 : 0.69V … 1010000 ~1111111 : 1.3V
0	RSV	R	0	reserved

7.9.36 B4_CFG0

Address: 22h Reset: 4Ah

Bit	Name	Attribute	Default	Description
7:6	b4_imax	RWE	01	00 : 2A , 01 : 3A 10 : 4A , 11 : 5A
5	b4_ldo_imax	RWE	0	0: 400mA , 1: 500mA
4	RSV	R	0	reserved
3:1	b4_freq	RWE	101	000 to 011 : 1MHz 100 : 1.5MHz 101 : 2MHz 110 : 2.5MHz 111 : 3MHz
0	ldo1_ilimsel	RWE	0	ldo1 ilim select: ldo mode: 0 : 400mA; 1 : 500mA plsw mode: 0 : 400mA; 1 : 500mA nlsw mode: 0 : 600mA; 1 : 1200mA

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7.9.37 B4_CFG1

Address: 23 h Reset: 3C h

Bit	Name	Attribute	Default	Description
7:1	B4_sel_reg	RWE	0011110	0000000 : 0.9V 0000001 : 0.91V … 0011110 : 1.20V … 1101110 : 2.0V 1101110 ~1111111 : 2.0V
0	RSV	R	0	reserved

7.9.38 LDO1_CFG1

Address: 24 h Reset: 40 h

Bit	Name	Attribute	Default	Description
7:2	ldo1_sel	RWE	010000	000000: 1.0V 000001: 1.05V … 010000 : 1.80V … 100010 : 2.7V
1:0	RSV	R	00	reserved

7.9.39 LDO2_CFG1

Address: 25 h Reset: 40 h

Bit	Name	Attribute	Default	Description
7:2	ldo2_sel	RWE	0100000	000000: 1.0V 000001: 1.05V … 010000 : 1.80V (default) … 100010 : 2.7V
1	ldo2_ilimsel	RWE	0	ldo2 ilim select: ldo mode: 0 : 400mA; 1 : 500mA plsw mode: 0 : 400mA; 1 : 500mA
0	RSV	R	0	reserved

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7.9.40 DCDC_CFG0

Address: 26h Reset: FCh

Bit	Name	Attribute	Default	Description
7	B1_EN	RWE	1	0 : low level ENABLE signal 1 : high level ENABLE signal For nRESET = 0, if ENABLE keeps high level which is not from low to high, the rail will follow the sequence to ramp up. For nRESET = 1, if set ENABLE from low level to high level, the rail will ramp up immediately.
6	B2_EN	RWE	1	
5	B3_EN	RWE	1	
4	B4_EN	RWE	1	
3	LDO1_EN	RWE	1	
2	LDO2_EN	RWE	1	
1:0	RSV	R	00	reserved

7.9.41 SLP_CFG

Address: 27h Reset: 3Ch

Bit	Name	Attribute	Default	Description
7	B1_ALIVE_SLP	RWE	0	0 : When PMIC is in SLP mode (PS3.5 mode), turns off. 1 : When in PS3.5 mode, keeps alive and enter LPM
6	B2_ALIVE_SLP	RWE	0	
5	B3_ALIVE_SLP	RWE	1	
4	B4_ALIVE_SLP	RWE	1	
3	LDO1_ALIVE_SLP	RWE	1	
2	LDO2_ALIVE_SLP	RWE	1	
1	RSV	R	0	reserved
0	SLP_EN	RW	0	0 : PMIC is in normal mode, if DPSLP_EN is also 0. 1 : PMIC is in sleep mode and all rails follow the settings in this register function to ramp down or enter LPM.

7.9.42 DPSLP_CFG

Address: 28h Reset: 3Ch

Bit	Name	Attribute	Default	Description
7	B1_ALIVE_DPSLP	RWE	0	0 : When PMIC is in DPSLP mode (PS4 mode), turns off. 1 : When in PS4 mode, keeps alive and enter LPM
6	B2_ALIVE_DPSLP	RWE	0	
5	B3_ALIVE_DPSLP	RWE	1	
4	B4_ALIVE_DPSLP	RWE	1	
3	LDO1_ALIVE_DPSLP	RWE	1	0 : When PMIC is in DPSLP mode (PS4 mode), turns off. 1 : When in PS4 mode, keeps alive and enter LPM
2	LDO2_ALIVE_DPSLP	RWE	1	
1	RSV	R	0	reserved
0	DPSLP_EN	RW	0	0 : PMIC is in normal mode, if SLP_EN is also 0. 1 : PMIC is in deepsleep mode and all rails follow the settings in this register function to ramp down or enter LPM.

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7.9.43 DCDC_CFG1

Address: 29h Reset: 00h

Bit	Name	Attribute	Default	Description
7	B1_FPWM	RW	0	0 : PSKIP mode 1 : Forced PWM mod（fccm）
6	B2_FPWM	RW	0	
5	B3_FPWM	RW	0	
4	B4_FPWM	RW	0	
3:0	RSV	R	0000	reserved

7.9.44 DCDC_CFG2

Address: 2Ah Reset: FCh

Bit	Name	Attribute	Default	Description
7	B1_DISCH	RW	1	0 : disable discharged resistor path 1 : enable discharged resistor path The discharged resistor path will be connected from VOUT to ground with the rail's ENABLE = low level, if the setting of the rail's discharged resistor path enable signal is 1.
6	B2_DISCH	RW	1	
5	B3_DISCH	RW	1	
4	B4_DISCH	RW	1	
3	LDO1_DISCH	RW	1	
2	LDO2_DISCH	RW	1	
1:0	RSV	R	00	reserved

7.9.45 DCDC_CFG3

Address: 2Bh Reset: 00h

Bit	Name	Attribute	Default	Description
7	B1_LPM	RWE	0	active mode lpm select 0 : normal mode 1 : low power mode
6	B2_LPM	RWE	0	
5	B3_LPM	RWE	0	
4	B4_LPM	RWE	0	
3	LDO1_LPM	RWE	0	
2	LDO2_LPM	RWE	0	
1:0	RSV	R	00	reserved

7.9.46 REAL_STAT

Address: 30h Reset: 00h

Bit	Name	Attribute	Default	Description
7:2	RSV	R	000000	reserved
1	uvlo_i	R	0	Real Time bit. Indicates uvlo_i
0	uvlo_shut_i	R	0	Real Time bit. Indicates uvlo_shut_i

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7.9.47 PWRDIS_TIME_CFG0

Address: 39h Reset: 00h

Bit	Name	Attribute	Default	Description
7:5	PWRDIS_DLY	RWE	000	PMIC will enter power-off sequence with the delay time after the low-level detected PWRDIS signal. 000 : 0ms 001 : 0.5ms 010 : 1.0ms 011 : 2.0ms 100 : 4.0ms 101 : 8.0ms 110 : 16ms 111 : disable PWRDIS function
4:0	RSV	R	00000	reserved

7.9.48 EFUSE_PROT2

Address: 3Dh Reset: 00h

Bit	Name	Attribute	Default	Description
7:0	EFUSE_PROT_CODE2	RW	00000000	This register serves as the read/write password for the EFUSE_LOAD0 register. Access to EFUSE_LOAD0 is only permitted after writing the value 0xEA to this register itself. The contents of this register are automatically cleared upon successful modification of EFUSE_LOAD0.

7.9.49 EFUSE_LOAD0

Address: 3Eh Reset: 00h

Bit	Name	Attribute	Default	Description
7	EFUSE_PROT_CODE2	R	0	This bit indicates whether the correct password (0xEA) has been written to register 0x3D to enable EFUSE_LOAD0 register access: 1: EFUSE_LOAD0 is currently readable/writable 0: EFUSE_LOAD0 is currently inaccessible This bit is automatically cleared upon successful modification of the EFUSE_LOAD0 register.
6:2	RSV	R	00000	Reserved
1	DIS_STB_LOAD	RWE	0	0: auto load all efuse in STANDBY status when power up sequency need

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				1: disable auto load all efuse in STANDBY status, even if power up sequency need.
0	LOAD_ALL	RW	0	Set 1b to re-load all EFUSE values into all reg。

7.9.50 B1_TIME_CFG0

Address: 60h Reset: 00h

Bit	Name	Attribute	Default	Description
7:3	B1_WUP_ONDLY	RWE	00000	B1 wake up on delay time. B1 will turn on with the setting delay time when PMIC is in the wake up sequence. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms
2:0	B1_SLP_OFFDLY	RWE	000	B1 turns off delay time. B1 will turn off with the setting delay time when PMIC is in the sleep off sequence. 000 : 0ms 001 : 0.25ms … 100 : 1ms 101 : 2ms 110 : 4ms 111 : 8ms

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7.9.51 B2_TIME_CFG0

Address: 61h Reset: 18h

Bit	Name	Attribute	Default	Description
7:3	B2_WUP_ONDLY	RWE	00011	B2 wake up on delay time. B2 will turn on with the setting delay time when PMIC is in the wake up sequence. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms
2:0	B2_SLP_OFFDLY	RWE	000	B2 turns off delay time. B2 will turn off with the setting delay time when PMIC is in the sleep off sequence. 000 : 0ms 001 : 0.25ms … 100 : 1ms 101 : 2ms 110 : 4ms 111 : 8ms

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7.9.52 B3_TIME_CFG0

Address: 62h Reset: 00h

Bit	Name	Attribute	Default	Description
7:3	B3_WUP_ONDLY	RWE	00000	B3 wake up on delay time. B3 will turn on with the setting delay time when PMIC is in the wake up sequence. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms
2:0	B3_SLP_OFFDLY	RWE	000	B3 turns off delay time. B3 will turn off with the setting delay time when PMIC is in the sleep off sequence. 000 : 0ms 001 : 0.25ms … 100 : 1ms 101 : 2ms 110 : 4ms 111 : 8ms

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7.9.53 B4_TIME_CFG0

Address: 63h Reset: 18h

Bit	Name	Attribute	Default	Description
7:3	B4_WUP_ONDLY	RWE	00011	B4 wake up on delay time. B4 will turn on with the setting delay time when PMIC is in the wake up sequence. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms
2:0	B4_SLP_OFFDLY	RWE	000	B4 turns off delay time. B4 will turn off with the setting delay time when PMIC is in the sleep off sequence. 000 : 0ms 001 : 0.25ms … 100 : 1ms 101 : 2ms 110 : 4ms 111 : 8ms

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7.9.54 LDO1_TIME_CFG0

Address: 64h Reset: 00h

Bit	Name	Attribute	Default	Description
7:3	LDO1_WUP_ONDLY	RWE	00000	LDO1 wake up on delay time. LDO1 will turn on with the setting delay time when PMIC is in the wake up sequence. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms
2:0	LDO1_SLP_OFFDLY	RWE	000	LDO1 turns off delay time. LDO1 will turn off with the setting delay time when PMIC is in the sleep off sequence. 000 : 0ms 001 : 0.25ms … 100 : 1ms 101 : 2ms 110 : 4ms 111 : 8ms

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7.9.55 LDO2_TIME_CFG0

Address: 65h Reset: 00h

Bit	Name	Attribute	Default	Description
7:3	LDO2_WUP_ONDLY	RWE	00000	LDO2 wake up on delay time. LDO2 will turn on with the setting delay time when PMIC is in the wake up sequence. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms
2:0	LDO2_SLP_OFFDLY	RWE	000	LDO2 turns off delay time. LDO2 will turn off with the setting delay time when PMIC is in the sleep off sequence. 000 : 0ms 001 : 0.25ms … 100 : 1ms 101 : 2ms 110 : 4ms 111 : 8ms

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7.9.56 B1_TIME_CFG1

Address: 66h Reset: 08h

Bit	Name	Attribute	Default	Description
7:5	RSV	R	000	reserved
4:0	B1_ONDLY	RWE	01000	B1 turns on delay time. B1 will turn on with the setting delay time when PMIC is in the power up sequencee. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms

7.9.57 B2_TIME_CFG1

Address: 67h Reset: 02h

Bit	Name	Attribute	Default	Description
7:5	RSV	R	000	reserved
4:0	B2_ONDLY	RWE	00010	B2 turns on delay time. B2 will turn on with the setting delay time when PMIC is in the power up sequencee. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms

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				… 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms

7.9.58 B3_TIME_CFG1

Address: 68h Reset: 03h

Bit	Name	Attribute	Default	Description
7:5	RSV	R	000	reserved
4:0	B3_ONDLY	RWE	00011	B3 turns on delay time. B3 will turn on with the setting delay time when PMIC is in the power up sequencee. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms

7.9.59 B4_TIME_CFG1

Address: 69h Reset: 00h

Bit	Name	Attribute	Default	Description
7:5	RSV	R	000	reserved
4:0	B4_ONDLY	RWE	00000	B4 turns on delay time. B4 will turn on with the setting delay time when PMIC is in the power up sequencee. 00000 : 0ms 00001 : 0.25ms …

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				01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms

7.9.60 LDO1_TIME_CFG1

Address: 6Ah Reset: 00h

Bit	Name	Attribute	Default	Description
7:5	RSV	R	000	reserved
4:0	LDO1_ONDLY	RWE	00000	LDO1 turns on delay time. LDO1 will turn on with the setting delay time when PMIC is in the power up sequencee. 00000 : 0ms 00001 : 0.25ms … 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms

7.9.61 LDO2_TIME_CFG1

Address: 6Bh Reset: 08h

Bit	Name	Attribute	Default	Description
7:5	RSV	R	000	reserved
4:0	LDO2_ONDLY	RWE	01000	LDO1 turns on delay time. LDO1 will turn on with the setting delay time when PMIC is in the power up sequencee. 00000 : 0ms 00001 : 0.25ms

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				… 01000 : 2ms 01001 : 2.5ms … 10100 : 8ms 10101: 9ms 10110 : 10ms … 11100 : 16ms

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8 Application and Implementation

8.1 System Example

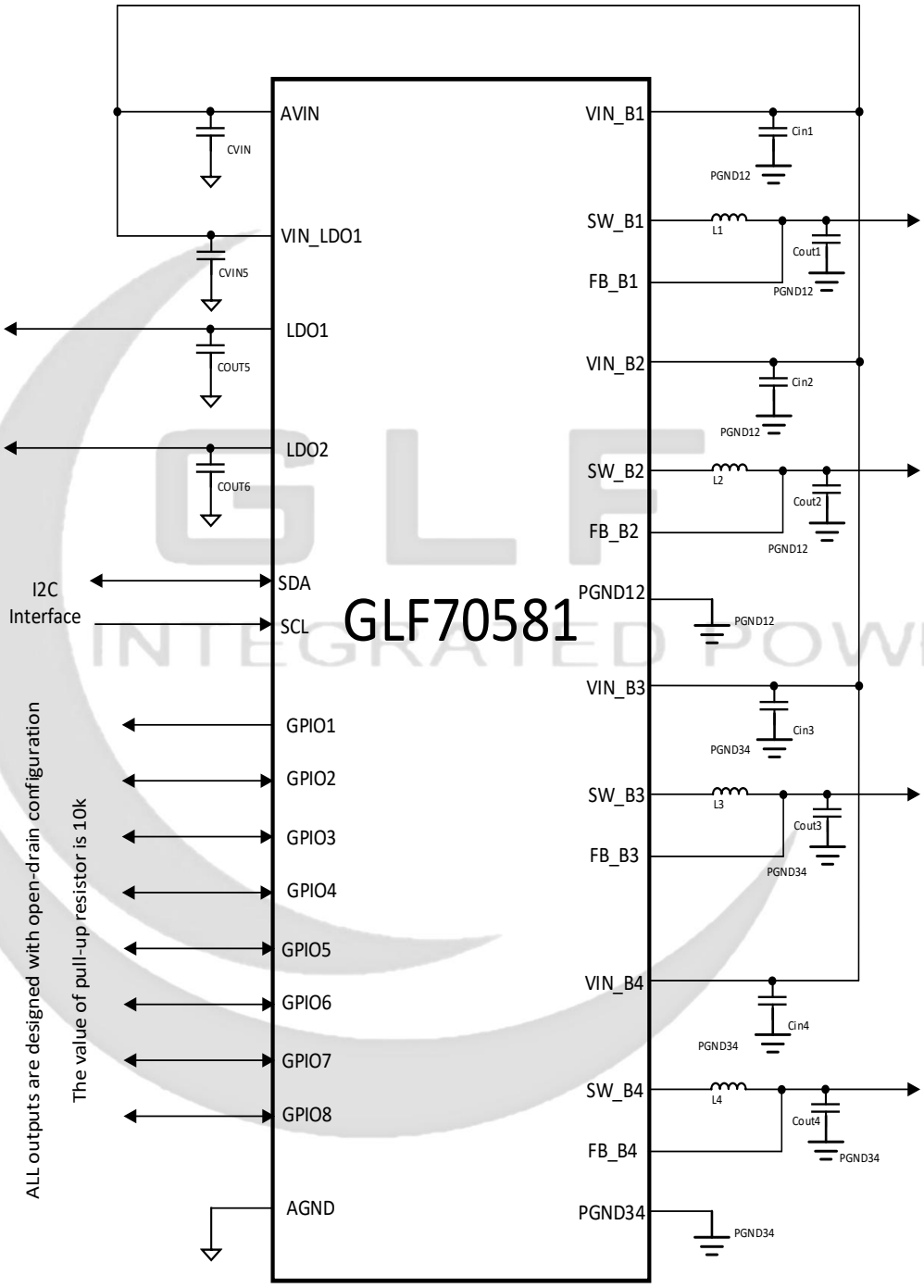

Figure 8-1. System Example

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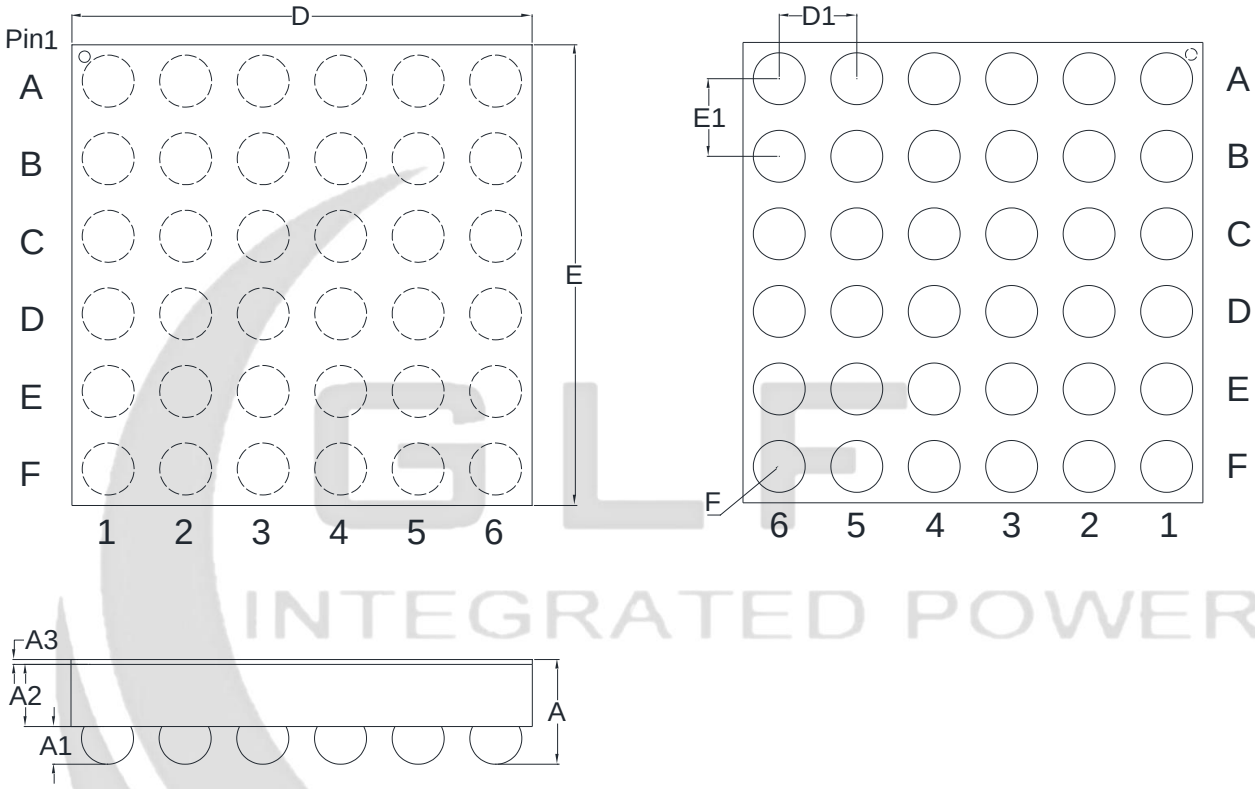
9 Package Outline and Layout

9.1 Package Outline



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.490	0.590	0.019	0.023
A1	0.170	0.220	0.007	0.009
A2	0.300	0.340	0.012	0.013
A3	0.020	0.030	0.001	0.001
D	2.350	2.400	0.093	0.094
E	2.350	2.400	0.093	0.094
D1	0.400 BSC.		0.016 BSC.	

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E1	0.400 BSC.		0.016 BSC.	
F	0.240	0.300	0.009	0.012

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9.2 Layout Example

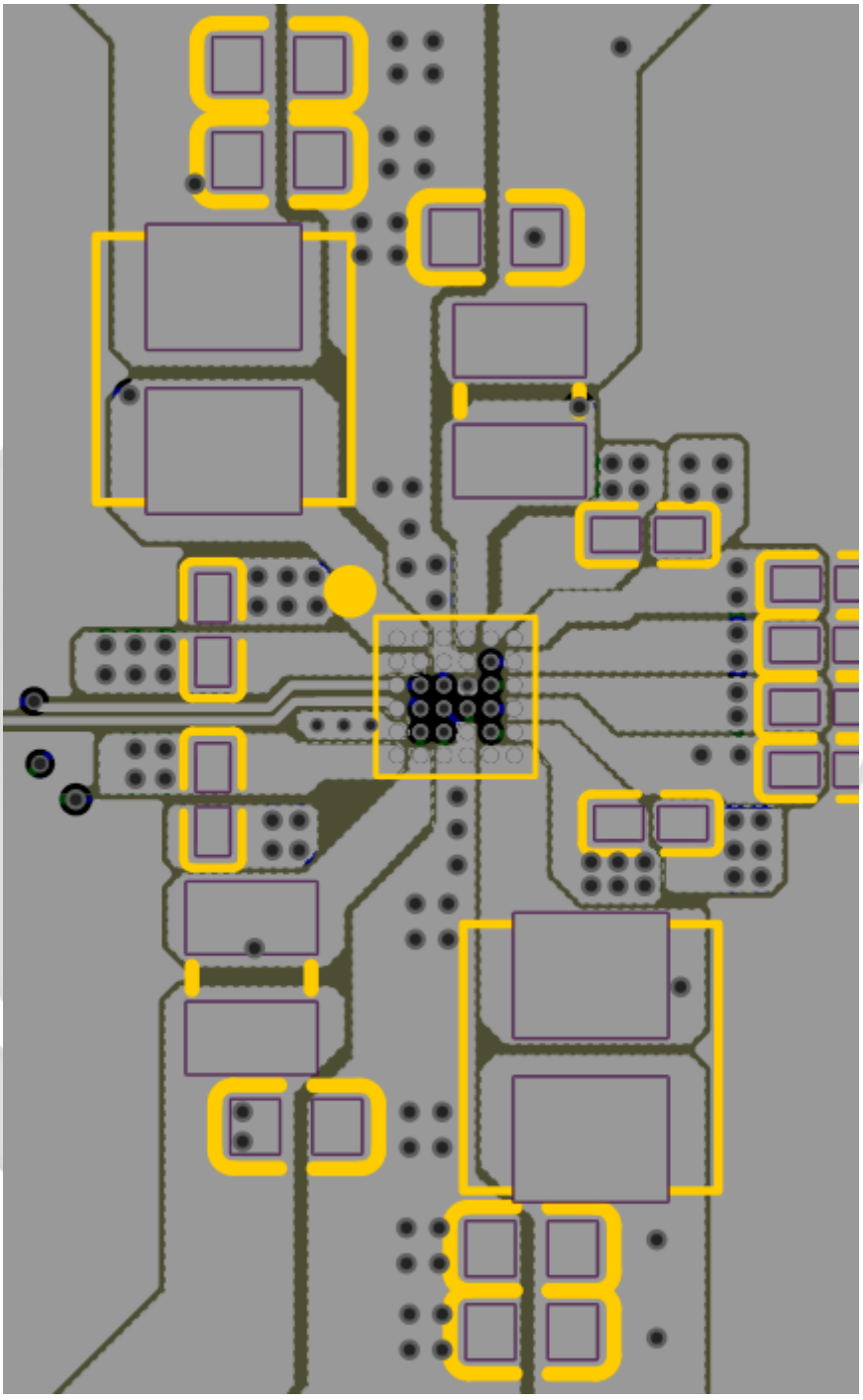

Figure 9-1. Layout Example

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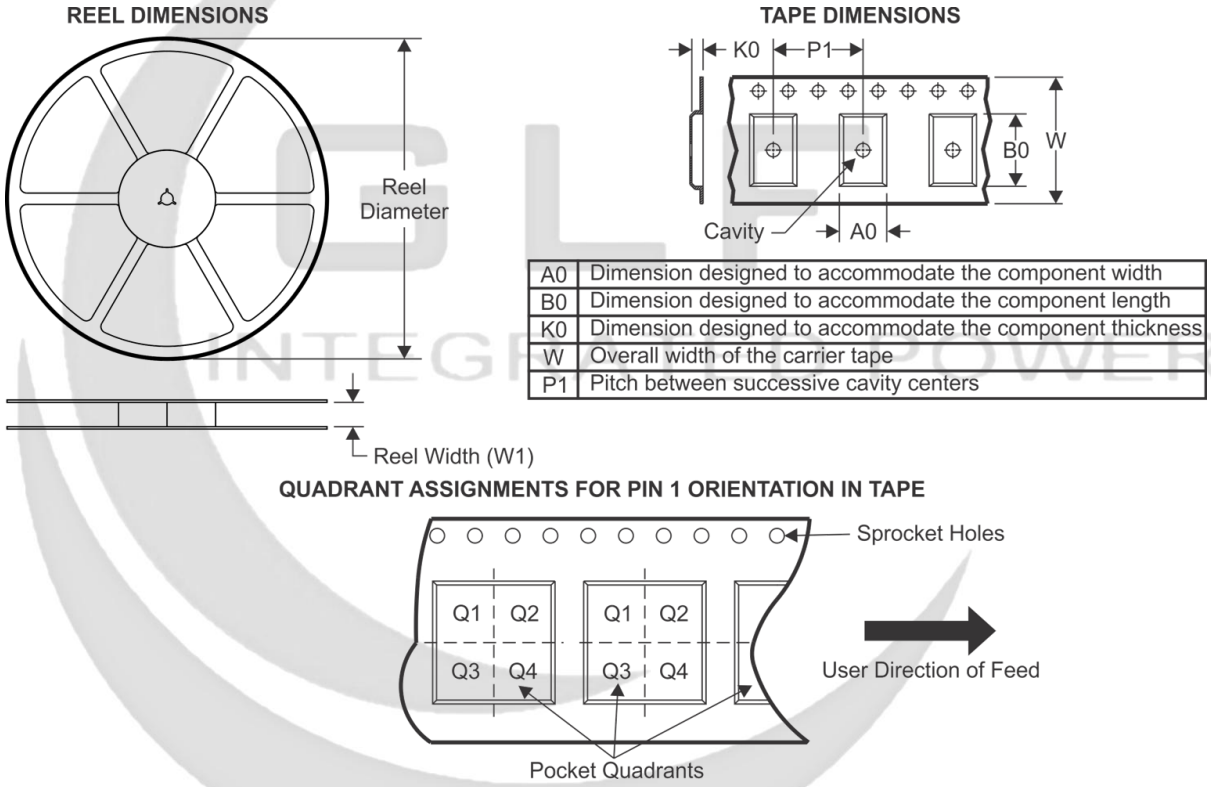
10 Packaging and Ordering Information

10.1 Order Information

Part Number	Part Number EFUSE Settings
GLF70581-S87	4*Buck+2*LDO PMIC used for SSD module and embedded system

10.2 Tape and Reel Information

(The following is an example)



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
GLF70581	CSP	S87	36	3000	178	9.5	2.55	2.55	0.68	4.0	8.0	Q1

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