GLF4007

Ultra-low I_Q, Asymmetrical Power Mux IC with Auto & Manual Input Selection

Preliminary Specification

DESCRIPTION

The GLF4007 is an integrated power multiplexer IC with dual independent power switches connected to a single output pin to enable seamless transition between two input sources. The GLF4007 features asymmetrical power FET characteristics. Channel 1 (VIN1) provides lower conduction resistance to support 4.0 A continuous current capability. The current rating of another channel (VIN2) is 3.0 A. It is an ideal solution for a power system with an internal back up power source.

The GLF4007 provides an automatic selection mode as well as a manual selection mode by the combination of the logic input pins of S1 and S2. The S1 input pin is used along with the S2 input pin to select the automatic switching function, select VIN1 only, select VIN2 only, or turn both switches off. In the automatic selection mode, the GLF4007 automatically select the higher input voltage source out of two input DC power supplies.

The GLF4007 prevents cross conduction current between two input sources. When VOUT is higher than VIN, the GLF4007 prevents the reverse current from the output to the input, no matter which input supply is applied.

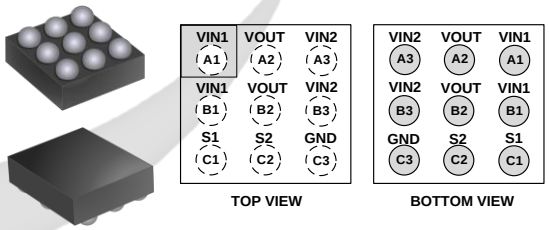
FEATURES

- Two-Input and Single-Output Power Multiplexer IC
- Auto and Manual Input Selection Mode
- Wide Input Range: 1.5 V to 5.5 V
- Low R_{ON}
  - Channel 1, 20 mΩ Typ at 5.5 V_{IN}
  - Channel 2, 30 mΩ Typ at 5.5 V_{IN}
- I_{OUT} Max
  - Channel 1 = 4.0 A at 2.0 V_{IN} to 5.5 V_{IN}
  - Channel 1 = 3.5 A at 1.5 V_{IN} to 2.0 V_{IN}
  - Channel 2 = 3.0 A at 1.5 V_{IN} to 5.5 V_{IN}
- Ultra-Low Supply Current at Operation
  - I_Q : 1.1 µA Typ at 5.5 V_{IN}
- Ultra-Low Shutdown Current
  - I_{SD} : 550 nA Typ at 5.5 V_{IN}
- Reverse Current Blocking Protection
- Operating Temperature Range: -40 °C to 85 °C

APPLICATIONS

- Doorbell
- Internet Protocol Camera
- Subsystem with Backup Power
- IoT Tracking System
- Communication / Network System

PACKAGE



1.27 mm x 1.27 mm x 0.55 mm WLCSP

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PRODUCT INFORMATION

Part Number	Top Mark	Channel 1 (VIN1)		Channel 2 (VIN2)		Package
		R_{ON1} at 5.5 V_{IN}	I_{OUT}	R_{ON2} at 5.5 V_{IN}	I_{OUT}	
GLF4007-S57	HP	20 mΩ	4.0 A	30 mΩ	3.0 A	1.27 mm x 1.27 mm 9 Bumps WLCSP

FUNCTIONAL BLOCK DIAGRAM

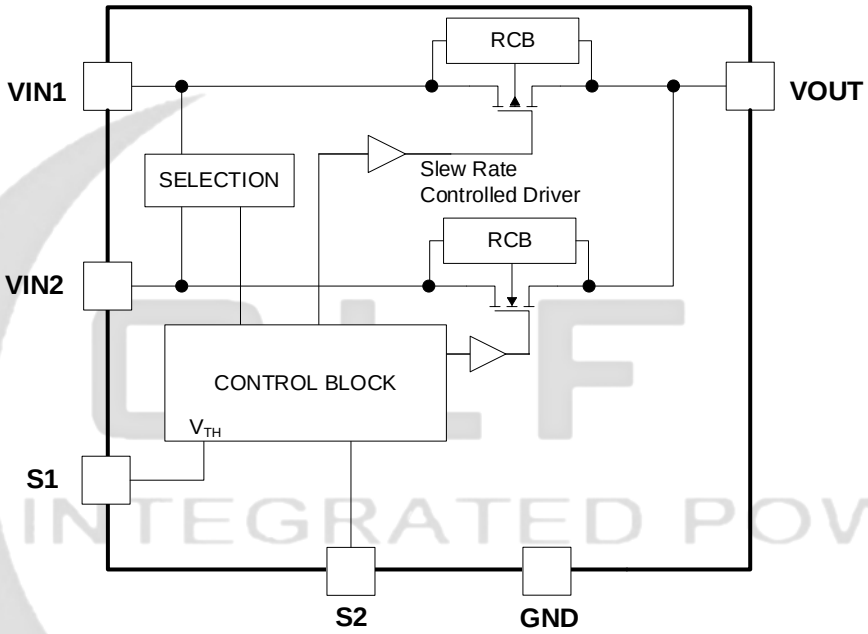

Figure 1. Functional Block Diagram

PIN CONFIGURATION

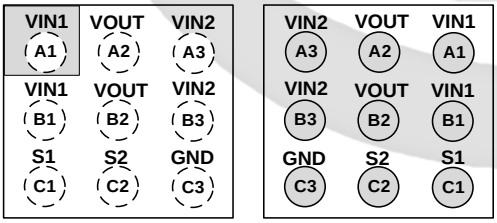

Figure 2. 1.27 mm x 1.27mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1, B1	VIN1	IC Input 1
A2, B2	VOUT	IC Output
A3, B3	VIN2	IC Input 2
C3	GND	Ground
C1	S1	Control logic input. Do not leave the S1 pin floating.
C2	S2	Control logic input. Do not leave the S2 pin floating.

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ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN1}, V_{IN2}, V_{OUT}	Each Pin Voltage Range to GND		- 0.3	6	V
V_{S1}, V_{S2}	Control Pin Voltage		- 0.3	6	V
I_{OUT}	Continuous Current through VIN1 at 2.0 V_{IN} to 5.5 V_{IN}			4.0	A
	Continuous Current through VIN1 at 1.5 V_{IN} to 2.0 V_{IN}			3.5	A
	Continuous Current through VIN2 at 1.5 V_{IN} to 5.5 V_{IN}			3.0	A
T_J	Maximum Junction Temperature			125	°C
T_{STG}	Storage Temperature		- 65	150	°C
T_A	Ambient Operating Temperature Range		- 40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	± 2		kV
		Charged Device Model, JESD22-C101	± 2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN1}, V_{IN2}	Input Voltage	1.5	5.5	V
V_{S1}, V_{S2}	Control Pin Voltage	0	5.5	V

ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = 1.5 V to 5.5 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ.	Max	Units
Basic Operation							
$I_{STBY_VIN1,2}$	VIN Unselect Channel Standby Current	V_{IN1} = 5.5 V, I_{OUT} = 0 mA, V_{S2} = V_{IN1}, V_{S1} = 0 V, V_{OUT} = V_{IN2} or V_{IN2} = 5.5 V, I_{OUT} = 0 mA, V_{S1} = V_{S2} = V_{IN2}, V_{OUT} = V_{IN1}	T_A = 25 °C		0.9	1.1	µA
			T_A = 85 °C		1.3		
$I_{Q_VIN1,2}$	VIN Quiescent Current	V_{IN1} = 5.5 V, I_{OUT} = 0 mA, V_{S1} = V_{S2} = V_{IN1}, V_{OUT} = V_{IN1} or V_{IN2} = 5.5 V, I_{OUT} = 0 mA, V_{S1} = V_{IN1}, V_{S2} = 0 V, V_{OUT} = V_{IN2}	T_A = 25 °C		1.1	1.6	
			T_A = 85 °C		1.6		
$I_{SD_VIN1,2}$	VIN Shutdown Current	$V_{IN1,2}$ = 5.5 V, V_{S2} = 0 V, V_{S1} = 5.5 V, V_{OUT} = High-Z	T_A = 25 °C		0.55	0.8	µA
			T_A = 85 °C		1.2		
I_{S1}, I_{S2}	S1 and S2 Pin Leakage	V_{S1} = V_{S2} = 5.5 V			2		nA

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{ON}	Channel 1 On-Resistance	V_{IN1} = 5.5 V, I_{OUT} = 200 mA	T_A = 25 °C		20	26	mΩ
			T_A = 85 °C		23		
		V_{IN1} = 3.3 V, I_{OUT} = 200 mA	T_A = 25 °C		24	31	
			T_A = 85 °C		28		
		V_{IN1} = 1.8 V, I_{OUT} = 200 mA	T_A = 25 °C		37	44	
			T_A = 85 °C		43		
		V_{IN1} = 1.5 V, I_{OUT} = 200 mA	T_A = 25 °C		46	54	
			T_A = 85 °C		52		
	Channel 2 On-Resistance	V_{IN2} = 5.5 V, I_{OUT} = 200 mA	T_A = 25 °C		30	40	
			T_A = 85 °C		35		
		V_{IN2} = 3.3 V, I_{OUT} = 200 mA	T_A = 25 °C		38	48	
			T_A = 85 °C		44		
		V_{IN2} = 1.8 V, I_{OUT} = 200 mA	T_A = 25 °C		61	72	
			T_A = 85 °C		70		
		V_{IN2} = 1.5 V, I_{OUT} = 200 mA	T_A = 25 °C		76	88	
			T_A = 85 °C		87		
V_{TH}	S1 Pin Threshold Voltage	V_{IN1} or V_{IN2} = 1.5 V to 5.5 V		0.8	1	1.2	V
		Hysteresis			50		mV
V_{IH}	S2 Input Logic High Voltage	V_{IN1} or V_{IN2} = 1.5 V to 5.5 V		1.2			V
V_{IL}	S2 Input Logic Low Voltage	V_{IN1} or V_{IN2} = 1.5 V to 5.5 V				0.3	
Reverse Current Blocking Protection							
t_{RCB}	RCB Response Time (1)	V_{OUT} > Selected V_{IN} + 1 V			2		µs
V_{RCB_TH}	RCB Protection Threshold	V_{OUT} - V_{IN}			60		mV
V_{RCB_RL}	RCB Protection Release	V_{IN} - V_{OUT}			44		mV
I_{RCB}	RCB activation current (1)				1.4		A
Switching Characteristics							
V_{TR}	Auto Input Selection Trigger (1)	V_{INX} - V_{INY}, In automatic selection mode			120		mV
t_{SW}	Switching Over time In Manual Mode (1)	V_{IN1} to V_{IN2}	V_{IN1} = 4.2 V, V_{IN2} = 3.6 V, C_{IN} = C_{OUT} = 10 µF, R_L = 10 Ω		36		µs
		V_{IN2} to V_{IN1}			18		
t_{dON}	Turn-On Delay time, Channel 1	V_{IN1} = 5 V	C_{IN} = C_{OUT} = 10 µF, R_L = 100 Ω		1100		
		V_{IN1} = 4.2 V			1130		
		V_{IN1} = 3.3 V			1133		
		V_{IN1} = 1.8 V			1207		
	Turn-On Delay time, Channel 2	V_{IN1} = 5 V			600		
		V_{IN1} = 4.2 V			606		
		V_{IN1} = 3.3 V			619		
		V_{IN1} = 1.8 V			639		
t_R	VOUT Rise Time, Channel 1	V_{IN1} = 5 V			1716		
		V_{IN1} = 4.2 V			1546		
		V_{IN1} = 3.3 V			1308		
		V_{IN1} = 1.8 V			910		
	VOUT Rise Time, Channel 2	V_{IN1} = 5 V			985		
		V_{IN1} = 4.2 V			863		
		V_{IN1} = 3.3 V			746		
		V_{IN1} = 1.8 V			517		

Note: 1. By design; characterized, not production tested.

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APPLICATION DIAGRAM

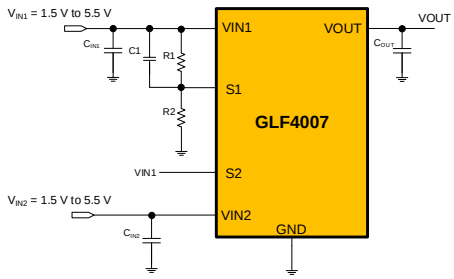

Figure 3. VIN1 Preference Selection Mode

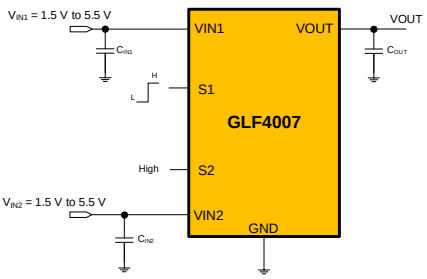

Figure 4. Manual Selection Mode by GPIO

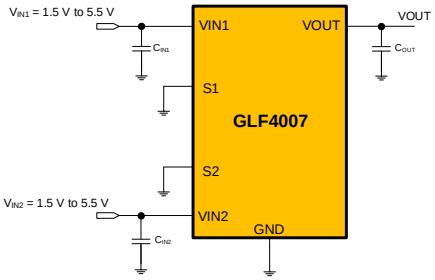

Figure 5. Auto Selection Mode

TRUTH TABLE AND TIMING DIAGRAM

Mode	S2	S1	VOUT	Function
Manual	High	> V_{TH}	VIN1	VIN1 is selected
	High	< V_{TH}	VIN2	VIN2 is selected
	Low	> V_{TH}	High-Z	Both channels are off
Auto	Low	< V_{TH}	Higher voltage between VIN1 and VIN2	Auto-Input selection

Note : V_{INX} or V_{INY} > 1.5 V (V_{IN_MIN}), High = V_{S2} > V_{IH}, Low = V_{S2} < V_{IL}

Table 1. Truth Table of Input Source Selection

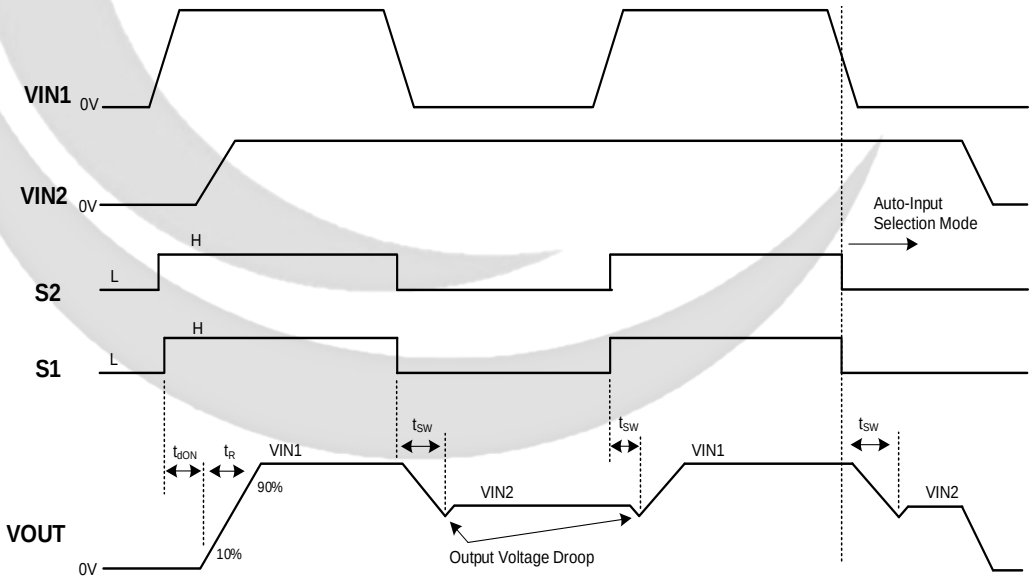

Figure 6. Timing Diagram, Manual Mode (Figure 3) with S2 tied to VIN1
High : V_{S2} > V_{IH}, V_{S1} > V_{TH} , Low : V_{S2} < V_{IL}, V_{S1} < V_{TH}

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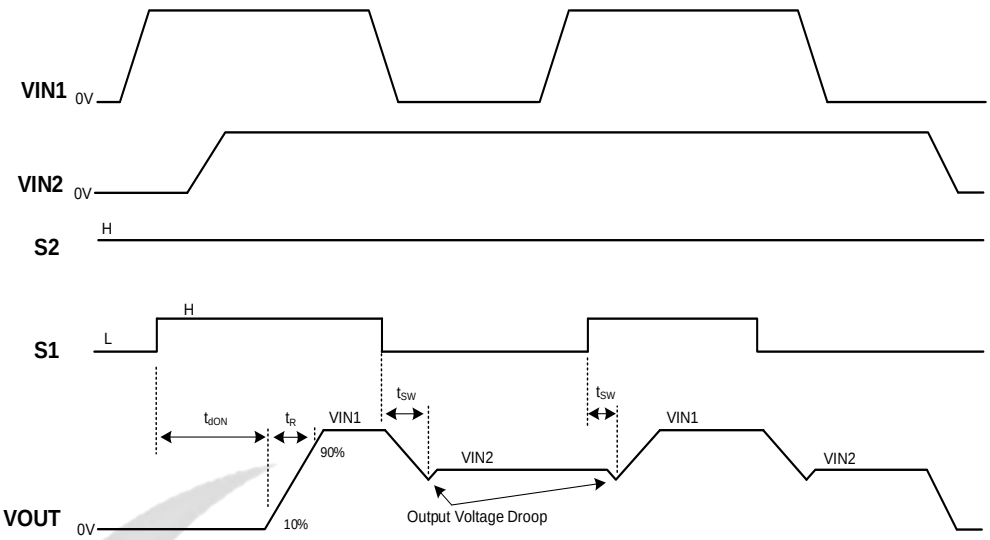

Figure 7. Timing Diagram, Manual Mode (Figure 4) with S1 controlled by GPIO
High : $V_{S2} > V_{IH}$, $V_{S1} > V_{TH}$, Low : $V_{S2} < V_{IL}$, $V_{S1} < V_{TH}$

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TYPICAL PERFORMANCE CHARACTERISTICS

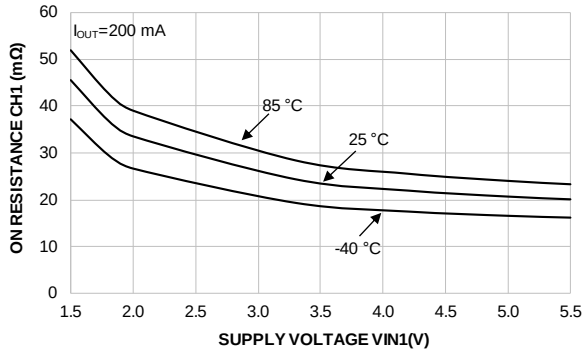

Figure 8. On-Resistance vs. Supply Voltage, Channel 1

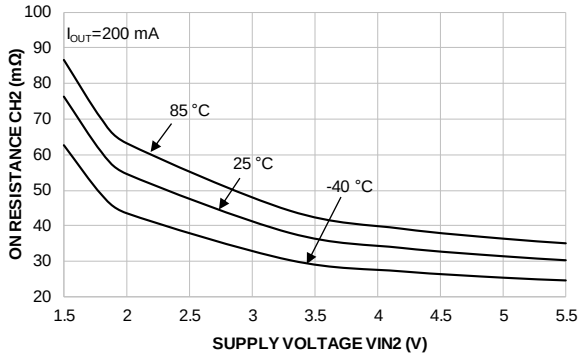

Figure 9. On-Resistance vs. Supply Voltage, Channel 2

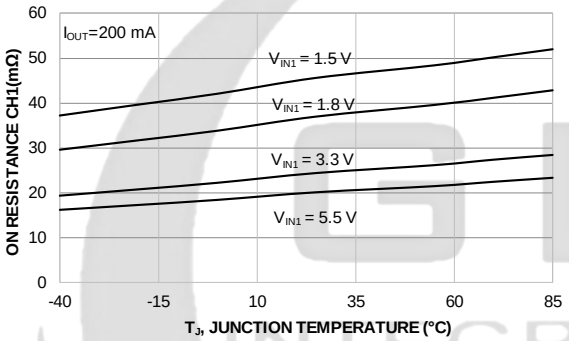

Figure 10. On-Resistance vs. Temperature, Channel 1

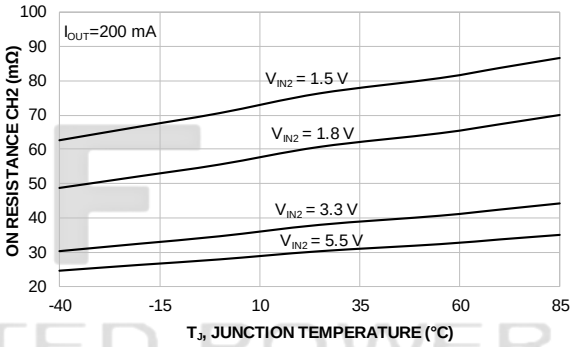

Figure 11. On-Resistance vs. Temperature, Channel 2

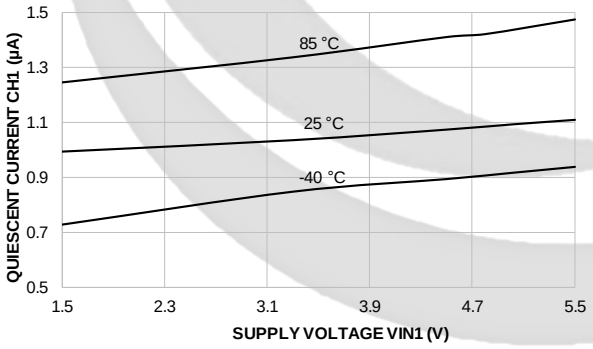

Figure 12. VIN1 Quiescent Current vs. Supply Voltage

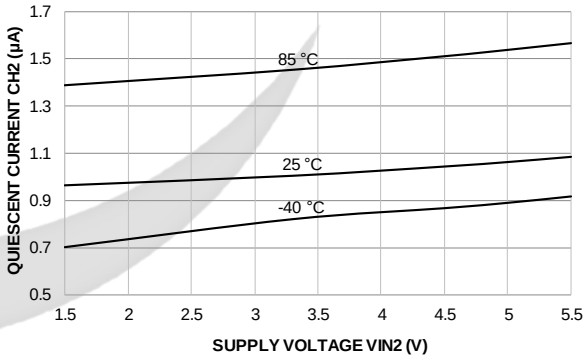

Figure 13. VIN2 Quiescent Current vs. Supply Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

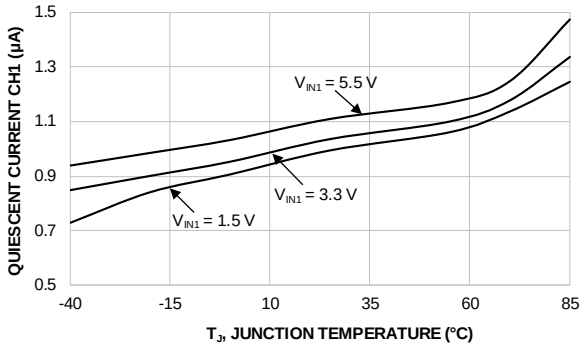

Figure 14. VIN1 Quiescent Current vs. Temperature

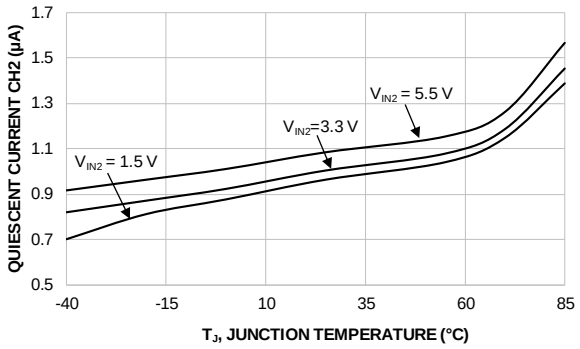

Figure 15. VIN2 Quiescent Current vs. Temperature

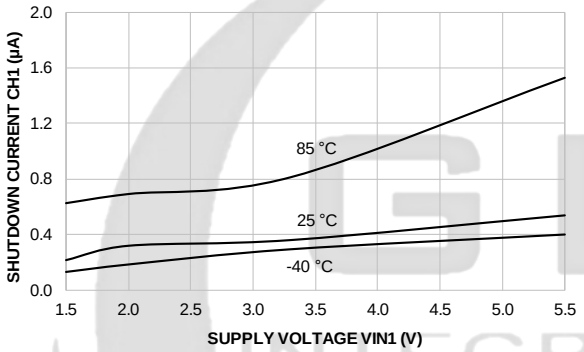

Figure 16. VIN1 Shutdown Current vs. Supply Voltage

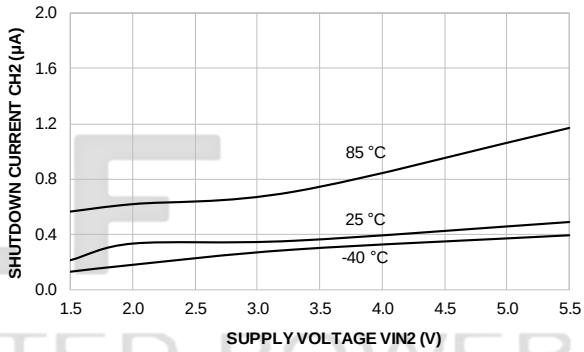

Figure 17. VIN2 Shutdown Current vs. Supply Voltage

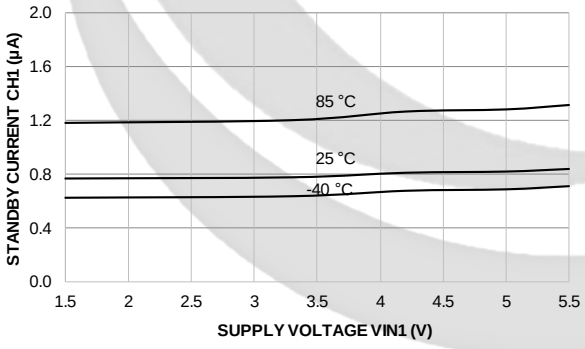

Figure 18. VIN1 Standby Current vs. Supply Voltage

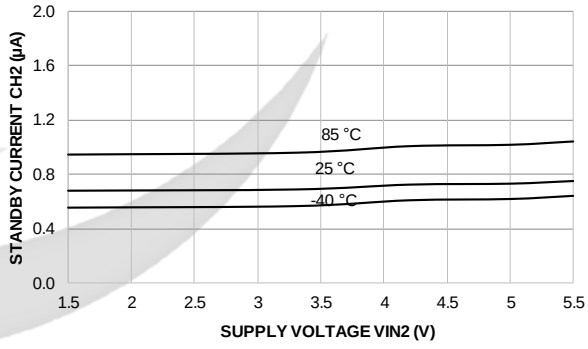

Figure 19. VIN2 Standby Current vs. Supply Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

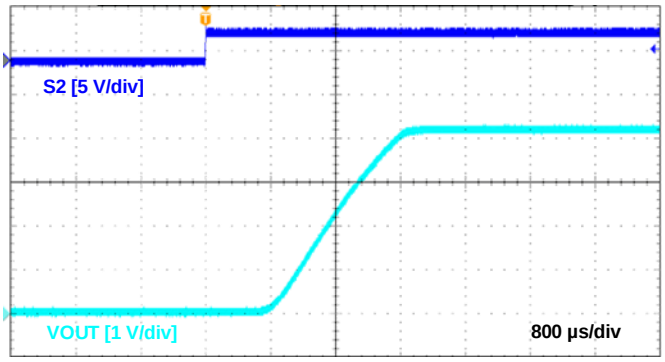

Figure 20. Turn-On Response, Channel 1
V_{IN1}=4.2 V, C_{IN}=C_{OUT} =10 µF, R_L=100 Ω, S2=High

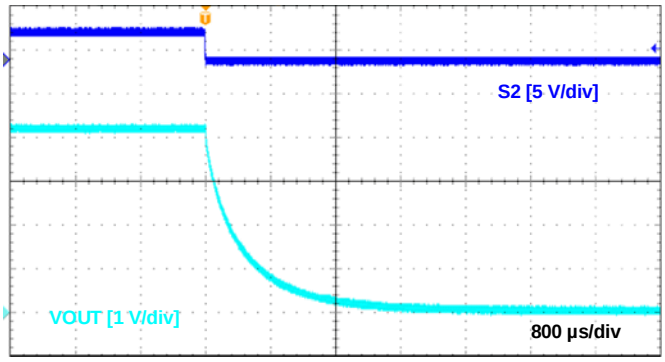

Figure 21. Turn-Off Response, Channel 1
V_{IN1}=4.2 V, C_{IN}=C_{OUT} =10 µF, R_L=100 Ω, S2=High

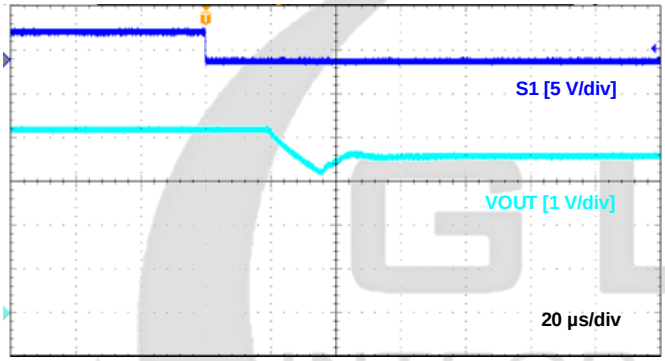

Figure 22. VOUT Switchover from 4.2 V to 3.6 V
V_{IN1}=4.2 V, V_{IN2}=3.6 V, C_{IN}=C_{OUT}=10 µF, R_L=10 Ω
S2 = VIN1, S1 controlled by GPIO

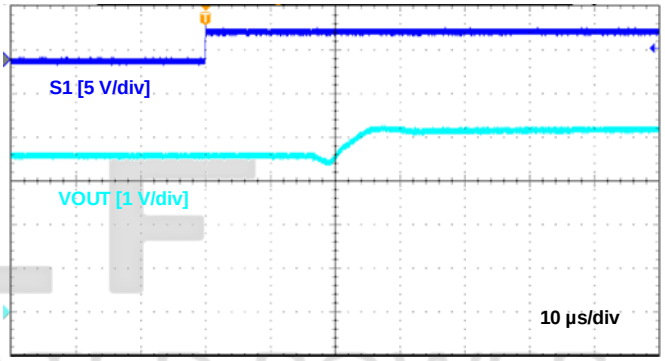

Figure 23. VOUT Switchover from 3.6 V to 4.2 V
V_{IN1}=4.2 V, V_{IN2}=3.6 V, C_{IN}=C_{OUT}=10 µF, R_L=10 Ω
S2 = VIN1, S1 controlled by GPIO

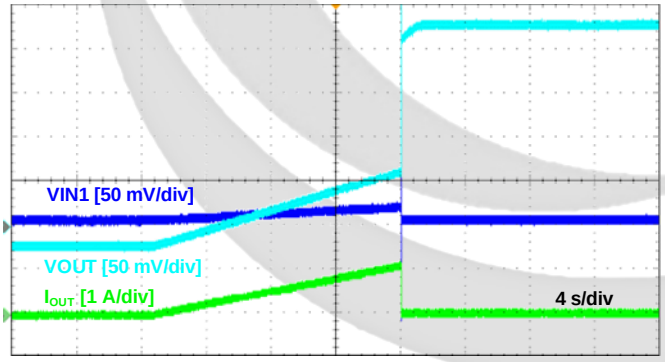

Figure 24. Reverse Current Blocking on Each VIN
V_{IN1} =3.3 V, V_{OUT}=3 V to 3.4 V, C_{IN}=C_{OUT}=10 µF

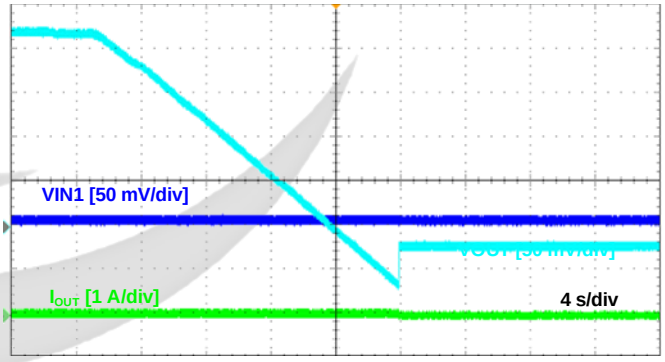

Figure 25. Reverse Current Blocking Release
V_{IN1} =3.3 V, V_{OUT}= 3.4 V to 3 V, C_{IN}=C_{OUT}=10 µF

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APPLICATION INFORMATION

The GLF4007 is a fully integrated power mux IC with the input voltage range from 1.5 V to 5.5 V. It has asymmetrical two channels and a fixed slew rate control to limit the inrush current during turn on. It also has very low on-resistance to reduce conduction loss. In the off state, it consumes very low leakage current to avoid unwanted standby current and save input power supply.

Input Source Selection

According to the state of S2 and S1 pins, the GLF4007 offers the automatic and manual selection mode. In each mode, the VOUT connects to one input source. Do not leave both S2 and S1 pins floating.

MODE	S2	S1	VOUT
Manual	High	> V_{TH}	VIN1
	High	< V_{TH}	VIN2
	Low	> V_{TH}	High-Z
Auto	Low	< V_{TH}	Higher voltage between VIN1 and VIN2

Table 2. Input Source Selection

In preference mode (refer to Figure 3), the S2 pin is connected to VIN1. The S1 pin is connected to the midpoint of a voltage divider formed by two resistors. The voltage at the S1 pin determines the operating state of the GLF4007. When VIN1 is applied and the voltage at the S1 pin is higher than the threshold voltage (V_{TH}), the VOUT is powered by VIN1. As VIN1 voltage drops, if the voltage at the S1 pin falls below V_{TH}, VOUT automatically switches over to VIN2.

For applications, where a General-Purpose Input/Output (GPIO) pin is used to select the input source (refer to Figure 4), the GPIO pin connects directly to the S1 pin, and the S2 pin is set high. When the GPIO pin is high, VIN1 is selected as the input. Conversely, when the GPIO pin is low, VIN2 is selected.

For applications, if both S1 & S2 are low (refer to Figure 5), the GLF4007 will choose a higher input voltage source to VOUT automatically.

Design Example for Switching-Over Trigger Voltage Calculation:

Parameter	Value
VIN1	4.5 V
VIN2	1 cell Lithium Thionyl Chloride Battery
Selection Mode	VIN1 Preference Selection

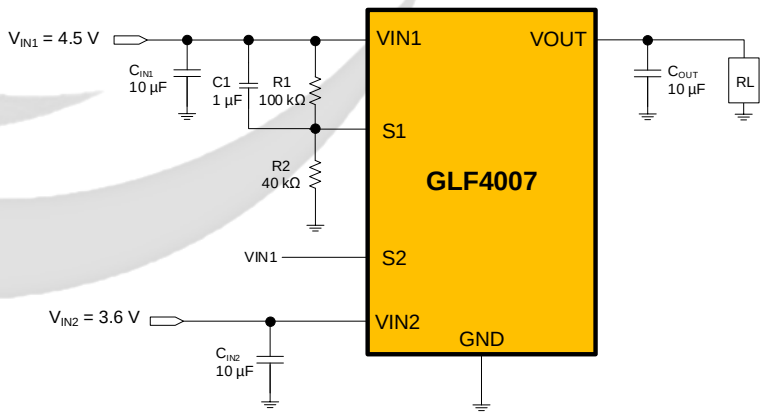

Figure 26. Design Example for V_{SW_TRG} Calculation

The value of the switching-over trigger voltage is determined by the following equation.

$$V_{SW_TRG} = V_{TH} \times (1 + R1 / R2)$$

Where, V_{SW_TRG} : Switching-over trigger voltage when VIN1 is unplugged.

V_{TH}: S1 pin threshold voltage

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For downstream systems requiring power supply switching with minimal output voltage drop, the GL4007 can reduces the voltage drop during transition from the primary input (VIN1) to the secondary input (VIN2) upon removal of VIN1. In this example, the switching trigger voltage is set to 3.5 V (when 4.5 V is removed) using resistors R1 (100 kΩ) and R2 (40 kΩ).

Output Voltage Drop at Switching Over

During the switching event, the output voltage drop is influenced by both the load resistance and the output capacitance. A lower load resistance at the switching point will result in a larger voltage drop. During switching events, the drop in output voltage is affected jointly by the load resistance and the output capacitance. Lower load resistance at the switching point leads to a greater voltage drop. To reduce voltage drop when a larger load current is required during the transition period, it is necessary to provide GLF4007 with a minimum 2.2 µF input capacitor and a minimum 10 µF output capacitor. However, it is strongly recommended to increase the output capacitor to 100 µF, which will significantly improve transient voltage drop during channel switching at load currents exceeding 1 A.

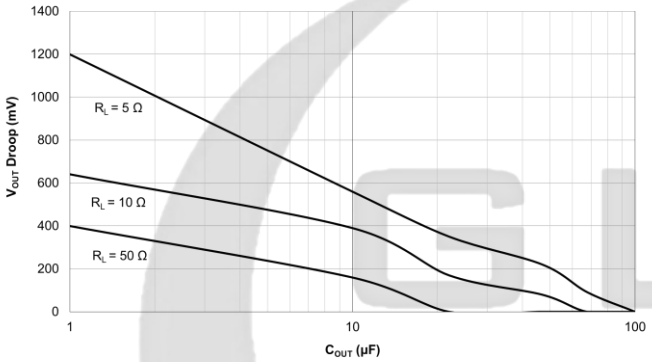

Figure 27. Output Voltage Droop at Switching Over from VIN1 (4.5 V) to VIN2 (3.3 V)

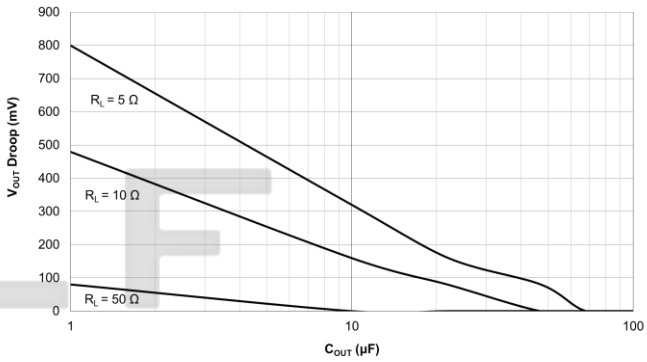

Figure 28. Output Voltage Droop at Switching Over from VIN2 (3.3 V) to VIN1 (4.5 V)

Reverse Current Blocking

The reverse current blocking protection will be enabled when either of the input voltage (VIN1 or VIN2) exceeds its minimum rating. The reverse current blocking protection triggers when the output voltage rises above an input voltage plus the reverse current blocking threshold (V_{RCB_TH}). The main FET immediately shuts off to prevent reverse current flow. It's important to note that some reverse current might exist before V_{RCB_TH} is reached. Normal operation resumes when the output voltage falls below the input minus the reverse current blocking release voltage (V_{RCB_RL}). An additional clamping component and a high output capacitance are recommended to safeguard against potential damage from high output voltage spikes.

Board Layout

All the external components should be placed to GLF4007 as close as possible. All traces should be as short as possible to minimize parasitic inductance. Wide traces of VIN, VOUT and GND can reduce parasitic effects under dynamic operations to improve thermal performance at high current loading.

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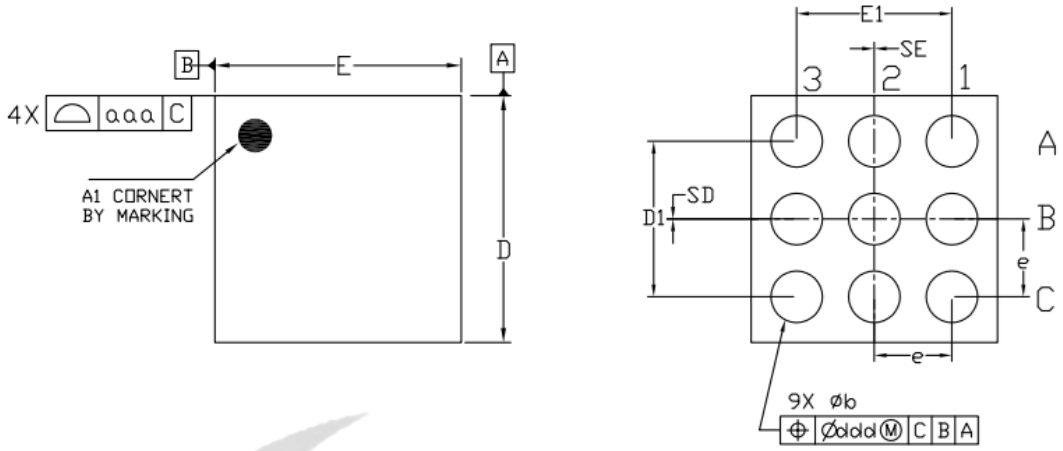
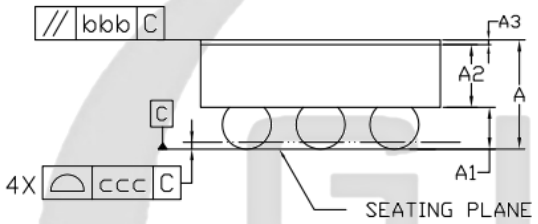
PACKAGE OUTLINE



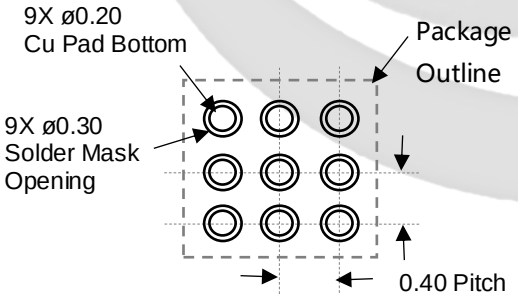


Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.175	0.200	0.225
A2	0.300	0.325	0.350
A3	0.020	0.025	0.030
D	1.255	1.270	1.285
E	1.255	1.270	1.285
D1	0.750	0.800	0.850
E1	0.750	0.800	0.850
b	0.215	0.265	0.315
e	0.400 BSC		
SD	0.000 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

Recommended Footprint



PACKAGING INFORMATION

Part Number	Package	Pins	Pitch	Top Mark	Moisture Sensitivity Level	Environmental Information
GLF4007-S57	1.27 mm x 1.27 mm x 0.55 mm WLCSP	9	0.4 mm	HP	MSL1	ROHS+HF

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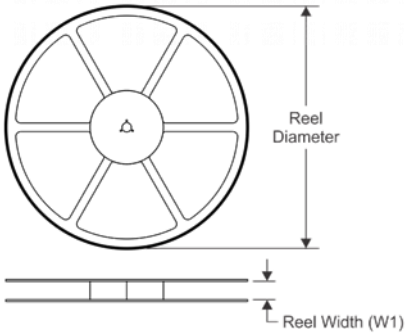
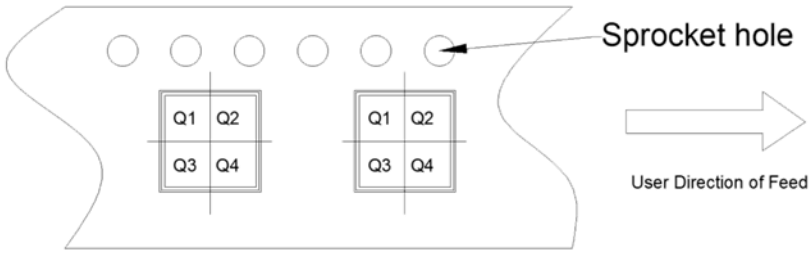
TAPE AND REEL INFORMATION

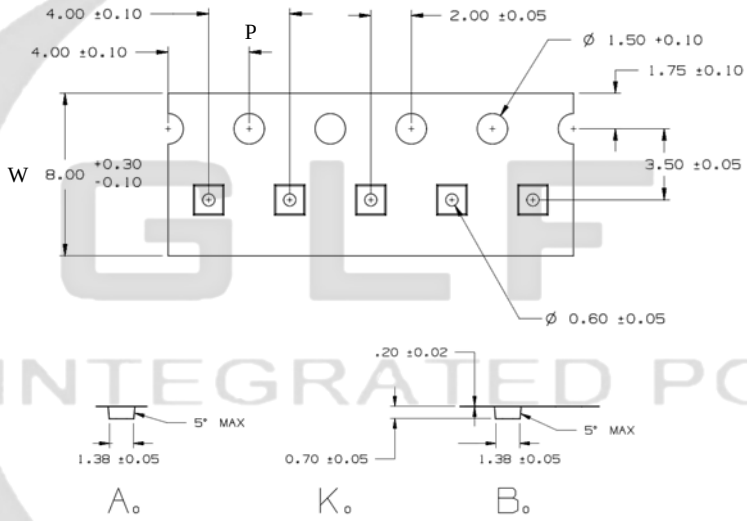
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF4007-S57	WLCSP	9	3000	180	9	1.38	1.38	0.78	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

K0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

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Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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