GLF4013

Ultra-low I_Q, Low Output Voltage Droop, 6 A Symmetrical Power Mux

Preliminary Specification

DESCRIPTION

The GLF4013 is an ultra-low I_Q integrated power multiplexer IC with dual independent power switches connected to a single output pin to enable seamless transition between two input sources. The GLF4013 features symmetrical power FET characteristics. Channel 1 (VIN1) and channel 2 (VIN2) provide ultra-low conduction resistance to support 6 A continuous current capability. It is an ideal solution for a power system with an internal back up power source.

The GLF4013 provides an automatic selection mode and a manual selection mode. The switching of these two modes is executed by combining the S1 and S2 pin settings. In the automatic input selection mode, the GLF4013 automatically selects a higher input voltage source between two input power sources.

The GLF4013 prevents cross conduction current between two input sources. When VOUT is higher than VIN, the GLF4013 prevents the reverse current from the output to the input, no matter which input supply is applied.

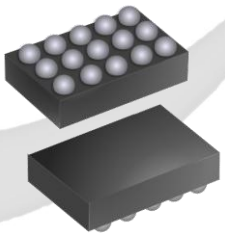
FEATURES

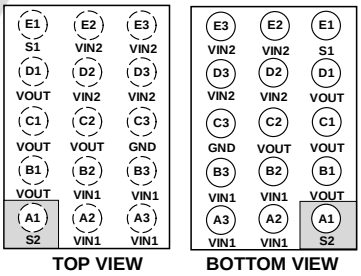
- Two-Input and Single-Output Power Multiplexer IC
- Auto & Manual Selection Mode
- Wide Input Range: 1.5 V to 5.5 V
- Low R_{ON}
  - 16 mΩ Typ at 5.5 V_{IN}
- I_{OUT} Max: 6 A Per Channel, VIN1 and VIN2
- Ultra-low Quiescent Current
  - I_Q : 1.4 μA Typ at 5.5 V_{IN}
- Low Shutdown Current
  - I_{SD} : 1.0 μA Typ at 5.5 V_{IN}
- Reverse Current Blocking Protection
- Thermal Shutdown Protection
- Wide Operating Temperature Range:
  - 40 °C to 105 °C

APPLICATIONS

- Smart Door Lock
- Subsystem with Backup Power
- Multi-channel Power Management
- Communication / Network System

PACKAGE





1.17 mm x 1.97 mm x 0.55 mm WLCSP

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PRODUCT INFORMATION

Part Number	Top Mark	R_{ON} (Typ.)	I_{OUT} (Max)	Package
GLF4013-SA7	ID	16 mΩ	6 A	1.17 mm x 1.97 mm x 0.55mm WLCSP

FUNCTIONAL BLOCK DIAGRAM

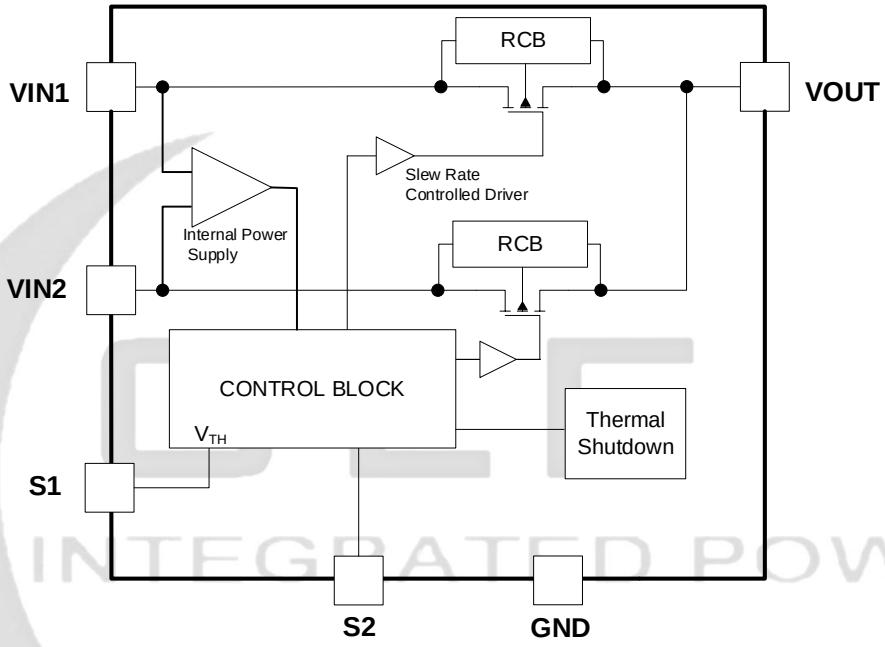

Figure 1. Functional Block Diagram

PIN CONFIGURATION

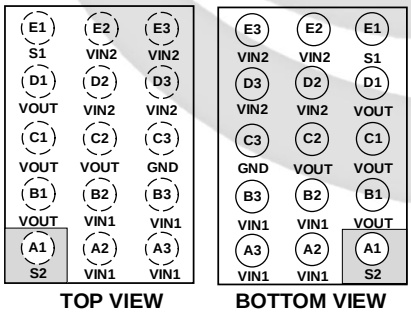

Figure 2. 1.17 mm x 1.97mm WLCSP

PIN DEFINITION

Pin #	Name	Description
B2, B3, A2, A3	VIN1	IC Input 1
B1, C1, C2, D1	VOUT	IC Output
D2, D3, E2, E3	VIN2	IC Input 2
C3	GND	Ground
E1	S1	Control logic pin. See table 1
A1	S2	Control logic pin. See table 1

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ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN1}, V_{IN2}, V_{OUT}	Each Pin Voltage Range to GND		- 0.3	6	V
V_{S1}, V_{S2}	Control Pin Voltage		- 0.3	6	V
I_{OUT}	Continuous Output Current	VIN1 or VIN2, higher input voltage at 2.5 V to 5.5 V Range		6	A
		VIN1 or VIN2, higher input voltage at 1.5 V to 2.5 V Range		4	A
T_J	Maximum Junction Temperature			150	°C
T_{STG}	Storage Junction Temperature		- 65	150	°C
T_A	Ambient Operating Temperature Range		- 40	105	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			60	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	± 4		kV
		Charged Device Model, JESD22-C101	± 2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN1}, V_{IN2}	Input Voltage	1.5	5.5	V
V_{S1}, V_{S2}	Control Pin Voltage	0	5.5	V

ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = 1.5 V to 5.5 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Basic Operation							
$I_{STBY_VIN1,2}$	VIN Unselect Channel Standby Current	V_{IN1} = 5.5 V, I_{OUT} = 0 mA, S2 = V_{IN1}, S1 = 0 V, VOUT= VIN2 or V_{IN2} = 5.5 V, I_{OUT} = 0 mA, S1 = V_{IN2}, S2 = 0 V, VOUT = VIN1	T_A = 25 °C		1.2	2	μA
			T_A = 85 °C (1)		1.4		
			T_A = 105 °C (1)		1.6		
$I_{Q_VIN1,2}$	VIN Quiescent Current	V_{IN1} = 5.5 V, I_{OUT} = 0 mA, S1 = V_{IN1}, S2 = 0 V, VOUT = VIN1 or V_{IN2} = 5.5 V, I_{OUT} = 0 mA, S2 = V_{IN2}, S1 = 0 V, VOUT = VIN2	T_A = 25 °C		1.4	2.2	
			T_A = 85 °C (1)		1.6		
			T_A = 105 °C (1)		2		
$I_{SD_VIN1,2}$	VIN Shutdown Current	$V_{IN1,2}$ = 5.5 V, V_{S2} =V_{S1} = 5.5 V, V_{OUT} = High-Z	T_A = 25 °C		1	1.5	
			T_A = 85 °C (1)		2		
			T_A = 105 °C (1)		3.6		
I_{S1}, I_{S2}	S1 and S2 Pin Leakage	V_{S1} = V_{S2} = 5.5 V			2		nA
R_{ON}	On-Resistance	$V_{IN1,2}$ = 5.5 V, I_{OUT} = 200 mA	T_A = 25 °C		16	22	mΩ
			T_A = 85 °C (1)		19		
			T_A = 105 °C (1)		20		
		$V_{IN1,2}$ = 3.3 V, I_{OUT} = 200 mA	T_A = 25 °C		21	28	
			T_A = 85 °C (1)		25		
			T_A = 105 °C (1)		26		

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ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN1} = V_{IN2} = 1.5 V to 5.5 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{ON}	On-Resistance	$V_{IN1,2}$ = 1.8 V, I_{OUT} = 200 mA	T_A = 25 °C		38	45	mΩ
			T_A = 85 °C (1)		44		
			T_A = 105 °C (1)		46		
		$V_{IN1,2}$ = 1.5 V, I_{OUT} = 200 mA	T_A = 25 °C		50	58	
			T_A = 85 °C (1)		56		
			T_A = 105 °C (1)		59		
V_{TH}	S1 Pin Threshold Voltage	$V_{IN1,2}$ = 1.5 V to 5.5 V		1.05	1.2	1.35	V
		Hysteresis			230		mV
V_{IH}	S2 Input Logic High Voltage	$V_{IN1,2}$ = 1.5 V to 5.5 V		1.2			V
V_{IL}	S2 Input Logic Low Voltage	$V_{IN1,2}$ = 1.5 V to 5.5 V				0.3	
Reverse Current Blocking Protection							
V_{RCB_TH}	RCB Protection Threshold	$V_{IN1,2}$ = 3.3 V, V_{OUT} - V_{IN}		0	20	50	mV
V_{RCB_RL}	RCB Protection Release	$V_{IN1,2}$ = 3.3 V, V_{IN} - V_{OUT}		0	20	50	mV
t_{RCB}	RCB Response Time (1)	V_{OUT} > Selected V_{IN} + 1 V			23		µs
I_{RCB}	RCB activation current (1)				0.7		A
TSD	Thermal Shutdown Protection Threshold (1)				150		°C
	Thermal Shutdown Release Hysteresis (1)				20		°C
Switching Characteristics							
V_{TR}	Auto Input Selection Trigger (1)	V_{INX} – V_{INY}, In automatic selection mode			230	300	mV
t_{CD}	Control Delay Time (1)	Delay Time between S1 and S2 in Manual Mode, See Figure 5		20			µs
t_{SW}	Switching Over time In Manual Mode (1)	VIN1 to VIN2	V_{IN1} = 3.3 V, V_{IN2} = 5.5 V C_{OUT} = 10 µF, R_L = 10 Ω		36		µs
		VIN2 to VIN1			18		
t_{dON}	Turn-On Delay time (1)	$V_{IN1,2}$ = 5 V	C_{OUT} = 10 µF, R_L = 150 Ω		330		µs
		$V_{IN1,2}$ = 4.2 V			340		
		$V_{IN1,2}$ = 3.3 V			350		
		$V_{IN1,2}$ = 1.5 V			380		
t_R	VOUT Rise Time (1)	$V_{IN1,2}$ = 5 V			430		
		$V_{IN1,2}$ = 4.2 V			380		
		$V_{IN1,2}$ = 3.3 V			320		
		$V_{IN1,2}$ = 1.5 V			210		
t_{dOFF}	VOUT Turn-Off Delay Time (1)	$V_{IN1,2}$ = 5 V			120		
		$V_{IN1,2}$ = 4.2 V			110		
		$V_{IN1,2}$ = 3.3 V			150		
		$V_{IN1,2}$ = 1.5 V			140		
t_F	VOUT Fall Time (1)	$V_{IN1,2}$ = 5 V			3.8		ms
		$V_{IN1,2}$ = 4.2 V			3.7		
		$V_{IN1,2}$ = 3.3 V			3.6		
		$V_{IN1,2}$ = 1.5 V			3.4		

Note: 1. By design; characterized, not production tested.

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APPLICATION DIAGRAM

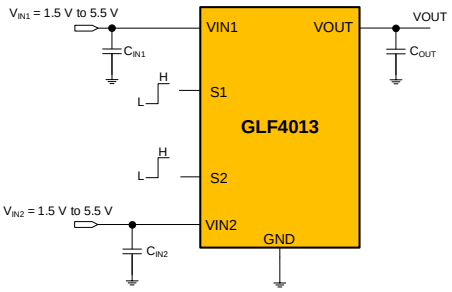

Figure 3. Manual Selection Mode by GPIO

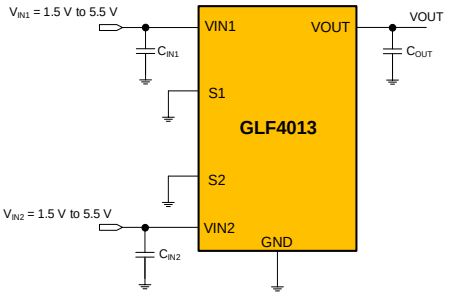

Figure 4. Auto Selection Mode

TRUTH TABLE AND TIMING DIAGRAM

Mode	S2	S1	Function
Manual (1),(2)	Low	> V_{TH}	VIN1 is selected
	High	< V_{TH}	VIN2 is selected
	High	> V_{TH}	Both channels are off
Auto (1),(3)	Low	< V_{TH}	Auto-Input selection

Note : (1) V_{INX} or V_{INY} > 1.5 V (V_{IN_MIN}), High = V_{S2} > V_{IH}, Low = V_{S2} < V_{IL}
(2) The operation timing of the S1 and S2 signals needs to follow Figure 5
(3) It is recommended to use the auto mode when V_{INX} - V_{INY} ≥ 500 mV.

Table 1. Truth Table of Input Source Selection

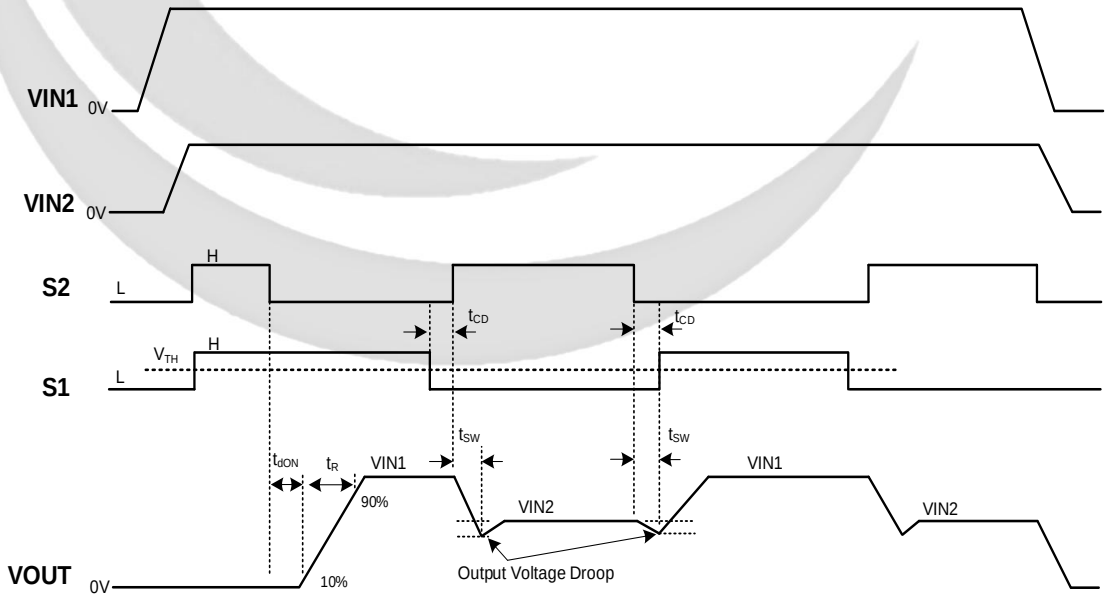

Figure 5. Timing Diagram, Manual Mode (Figure 3) with S1 and S2 controlled by GPIO
High: V_{S2} > V_{IH}, V_{S1} > V_{TH}, Low: V_{S2} < V_{IL}, V_{S1} < V_{TH}, when V_{IN1} > V_{IN2}

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TYPICAL PERFORMANCE CHARACTERISTICS

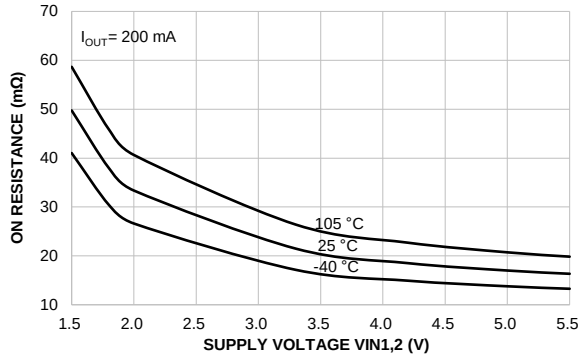

Figure 6. On-Resistance vs. Supply Voltage

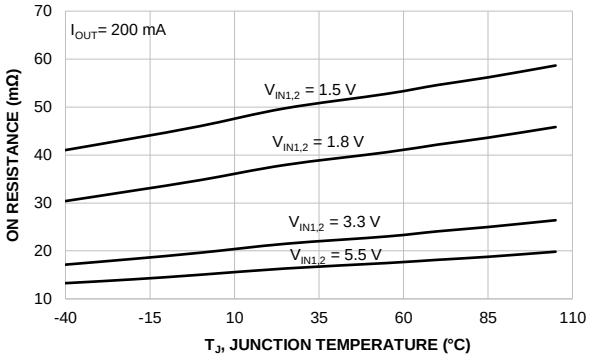

Figure 7. On-Resistance vs. Temperature

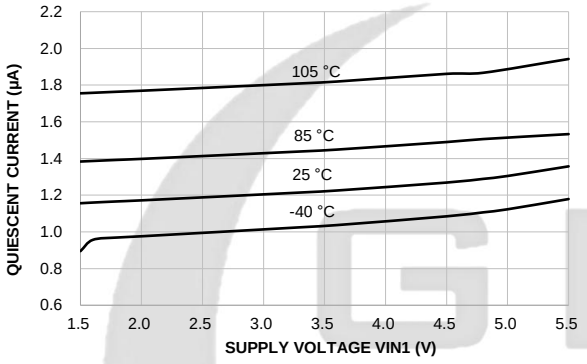

Figure 8. VIN1 Quiescent Current vs. Supply Voltage

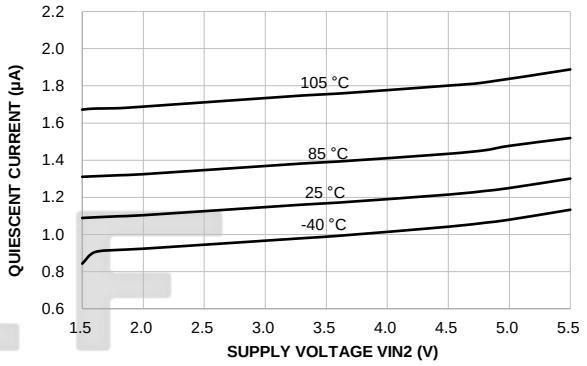

Figure 9. VIN2 Quiescent Current vs. Supply Voltage

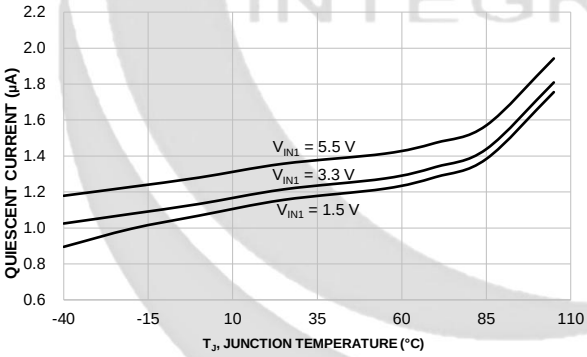

Figure 10. VIN1 Quiescent Current vs. Temperature

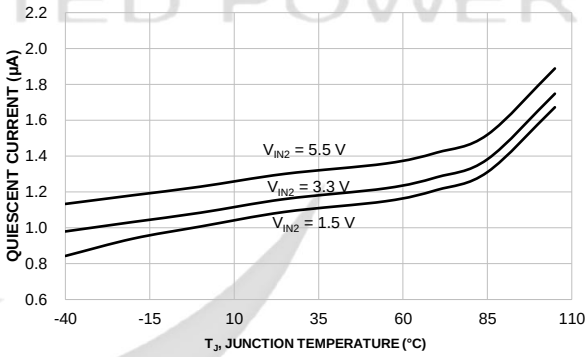

Figure 11. VIN2 Quiescent Current vs. Temperature

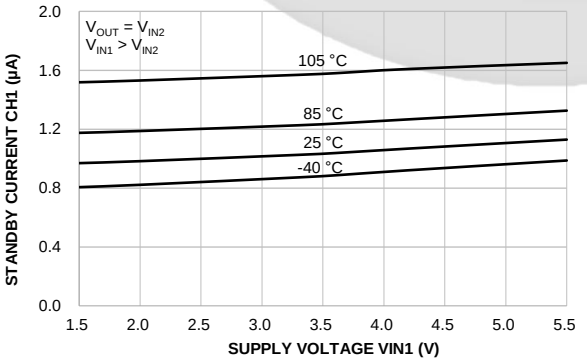

Figure 12. VIN1 Standby Current vs. Supply Voltage

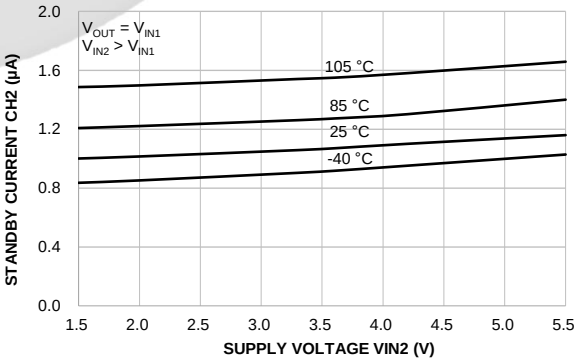

Figure 13. VIN2 Standby Current vs. Supply Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

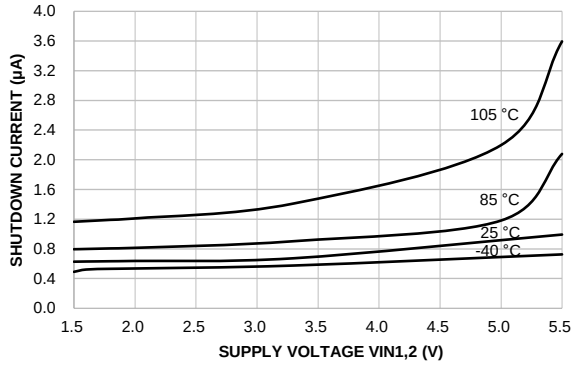

Figure 14. VIN Shutdown Current vs. Supply Voltage

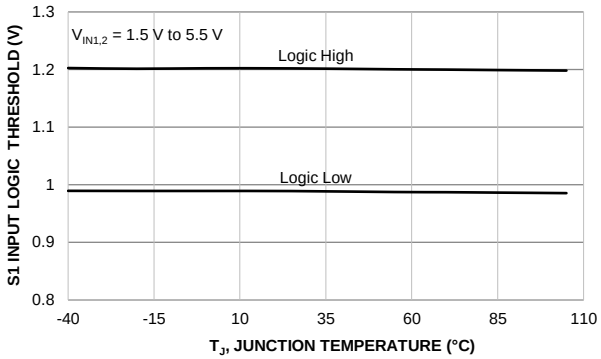

Figure 15. S1 Input Logic Threshold vs. Temperature

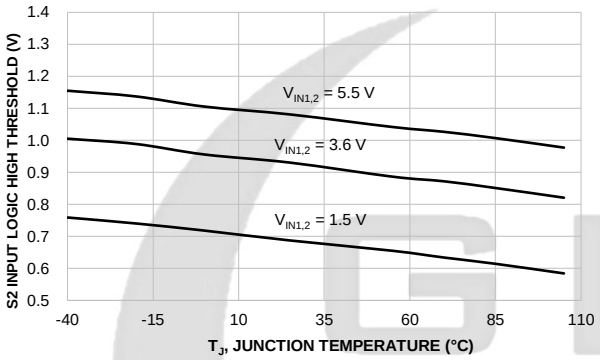

Figure 16. S2 Input Logic High Threshold vs. Temperature

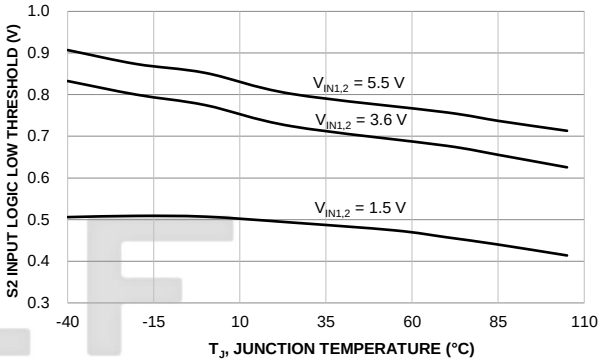

Figure 17. S2 Input Logic Low Threshold vs. Temperature

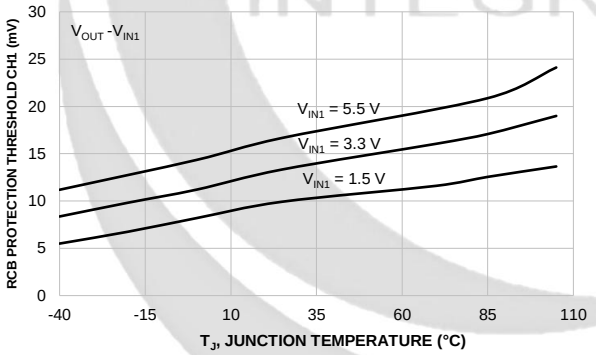

Figure 18. CH1 RCB Protection Threshold vs. Temperature

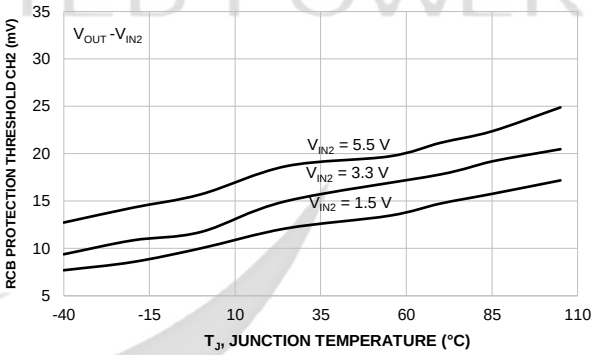

Figure 19. CH2 RCB Protection Threshold vs. Temperature

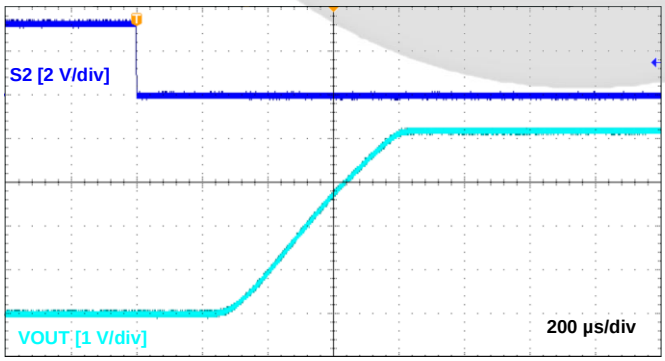

Figure 20. Turn-On Response, CH1
V_{IN1}=4.2 V, C_{IN}=C_{OUT} =10 µF, R_L=100 Ω

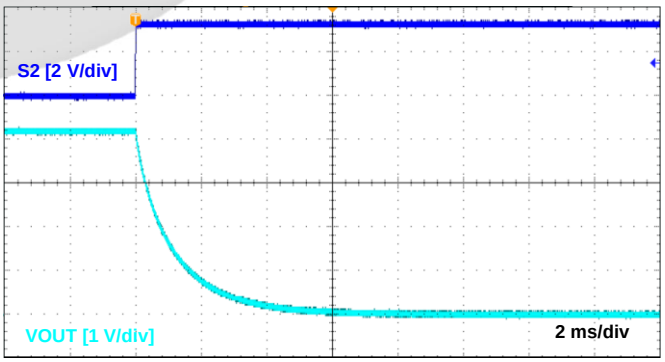

Figure 21. Turn-Off Response, CH1
V_{IN1}=4.2 V, C_{IN}=C_{OUT} =10 µF, R_L=100 Ω

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

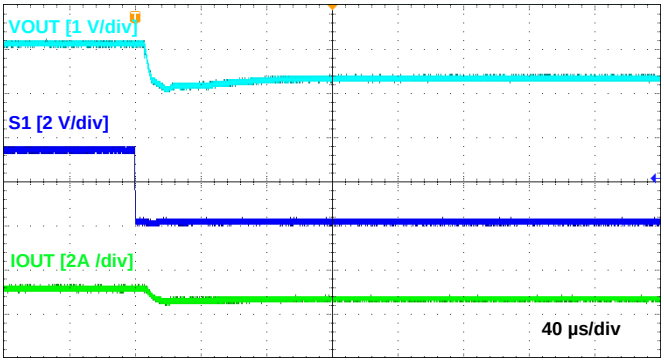


Figure 22. VOUT Switchover from 5.0 V to 4.2 V
V_{IN1}=5.0 V, V_{IN2}=4.2 V, C_{OUT}=47 µF, R_L=1.5 Ω

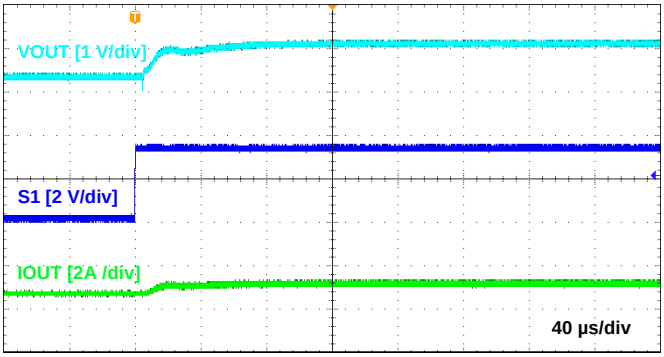
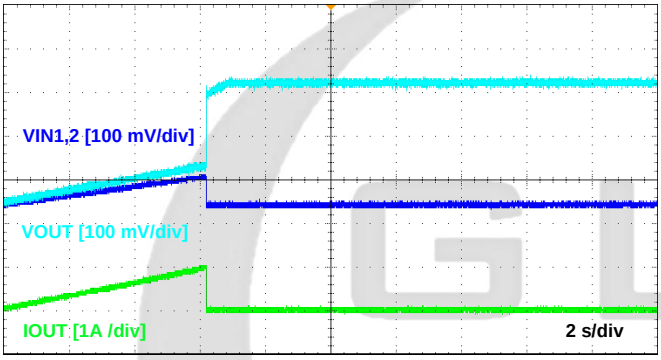
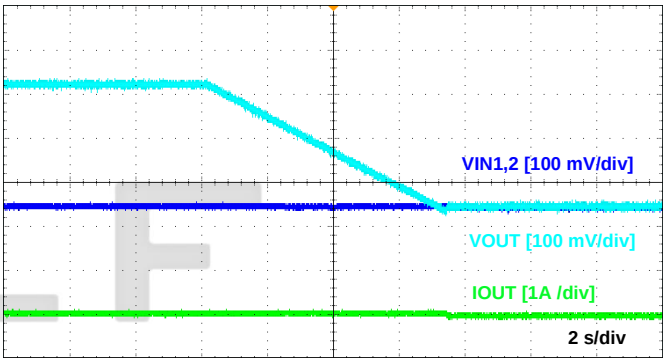


Figure 23. VOUT Switchover from 4.2 V to 5.0 V
V_{IN1}=5.0 V, V_{IN2}=4.2 V, C_{OUT}=47 µF, R_L=1.5 Ω



Fiqure 24. Reverse Current Blocking on Each Channel
$V_{IN1,2}$=3.3 V, V_{OUT}=3 V to 3.4 V, C_{IN}=C_{OUT}=10 µF



Fiqure 25. Reverse Current Blocking Release
$V_{IN1,2}$=3.3 V, V_{OUT}=3.4 V to 3 V, C_{IN}=C_{OUT}= 10 µF

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APPLICATION INFORMATION

The GLF4013 is a fully integrated power mux IC with the input voltage range from 1.5 V to 5.5 V. It has symmetrical two channels and a fixed slew rate control to limit the inrush current during turn on. It also has very low on-resistance to reduce conduction loss. In the off state, it consumes very low leakage current to avoid unwanted standby current and save input power supply.

Input Source Selection

According to the state of S2 and S1 pins, the GLF4013 offers the automatic and manual selection mode. In each mode, the VOUT connects to one input source. Do not leave both S2 and S1 pins floating.

Mode	S2	S1	Function
Manual	Low	> V_{TH}	VIN1 is selected
	High	< V_{TH}	VIN2 is selected
	High	> V_{TH}	Both channels are off
Auto	Low	< V_{TH}	Auto-Input selection

Table 2. Input Source Selection

For applications that use General Purpose Input/Output (GPIO) pins to select the input source (see Figure 3), the GPIO pins are directly connected to the S1 and S2 pins. When S1 is set to high and S2 is set to low, the device will select VIN1 as the output. When S1 is set to low and S2 is set to high, the device will select VIN2 as the output.

Note: The control delay time (t_{CD}) needs to be added between the S1 and S2 control signals to achieve lower switching Vdroop: for example, when the device switches from VIN1 to VIN2, S1 must first be set to low, and then after a 20μs (t_{CD}) delay, S2 is set to high. To switch back from VIN2 to VIN1, S2 must first be set to low, and then after a 20μs (t_{CD}) delay, S1 is set to high.

For applications, if both S1 & S2 are low (refer to Figure 4), the GLF4013 will choose a higher input voltage source to VOUT automatically. It is recommended to use V_{INX} - V_{INY} ≥ 500 mV for the auto mode, which will effectively prevent a series of problems caused by parasitic resistance in wires or PCB when the load current is high.

Output Voltage Droop at Switching Over

During switching events, the droop in output voltage is influenced by both the load current and the output capacitance. A higher load current at the switching point will result in a larger voltage droop. To reduce this droop when a large load current is required during the transition, it is recommended to use a large output capacitor. The Figure 26 shows the output voltage droop characteristics. A reminder: the minimum output voltage droop point will also be affected by the load transient capability of the input power supply.

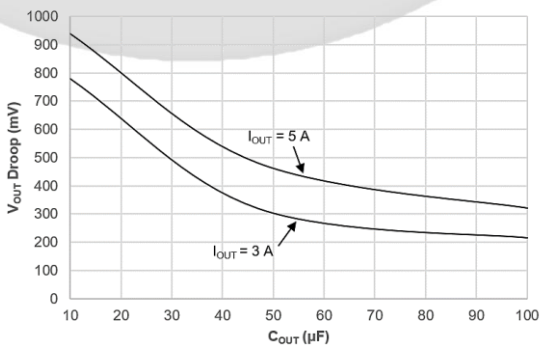

Figure 26. Output Voltage Droop at Switching Over from VIN1 (5.0 V) to VIN2 (3.3 V), Manual mode

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Thermal Shutdown Protection

The GLF4013 has a thermal shutdown protection. When the junction temperature exceeds TSD threshold, the device will turn off the internal main switch to protect itself from damage due to overheating. When the junction temperature drops below the TSD hysteresis, the device will return to normal operation.

Reverse Current Blocking

The reverse current blocking protection will be enabled when either of the input voltage (VIN1 or VIN2) exceeds its minimum rating. The reverse current blocking protection triggers when the output voltage rises above an input voltage plus the reverse current blocking threshold (V_{RCB_TH}). The main FET immediately shuts off to prevent reverse current flow. It's important to note that some reverse current might exist before V_{RCB_TH} is reached. Normal operation resumes when the output voltage falls below the input minus the reverse current blocking release voltage (V_{RCB_RL}). An additional clamping component and a high output capacitance are recommended to safeguard against potential damage from high output voltage spikes.

Board Layout

All the external components should be placed to GLF4013 as close as possible. All traces should be as short as possible to minimize parasitic inductance. Wide traces of VIN, VOUT and GND can reduce parasitic effects under dynamic operations to improve thermal performance at high current loading.

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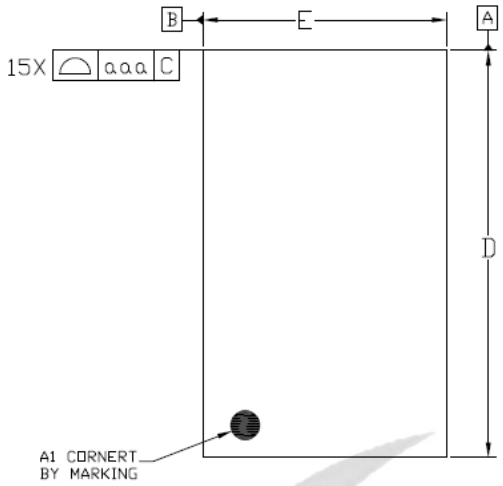
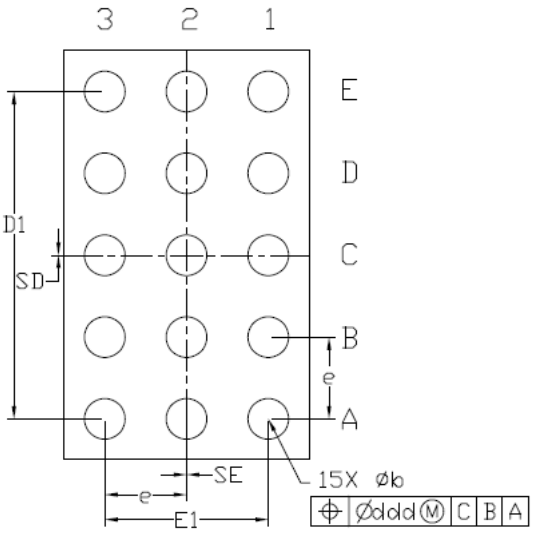
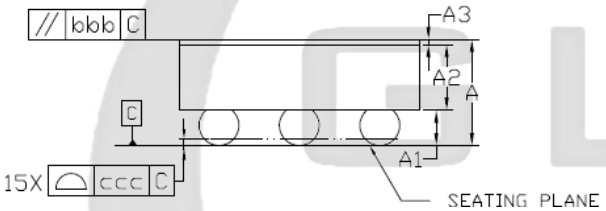
PACKAGE OUTLINE



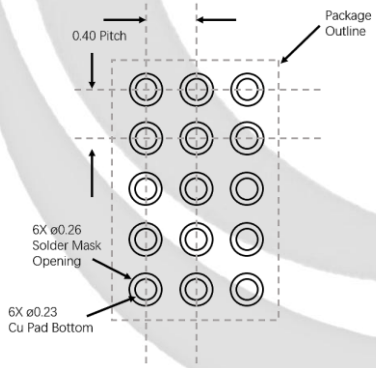
TOP VIEW



BOTTOM VIEW



Recommended Footprint



REF.	Dimensions Ref.		
	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.149	0.175	0.201
A2	0.325	0.350	0.375
A3	0.020	0.025	0.030
D	1.955	1.970	1.985
E	1.155	1.170	1.185
D1	1.550	1.600	1.650
E1	0.750	0.800	0.850
b	0.197	0.232	0.267
e	0.400 BSC		
SD	0.000 BSC		
SE	0.000 BSC		
Tol. of Form & Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

PACKAGING INFORMATION

Part Number	Package	Pins	Top Mark	Moisture Sensitivity Level	Environmental Information
GLF4013-SA7	WLCSP	15	ID	MSL1	ROHS+HF

Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

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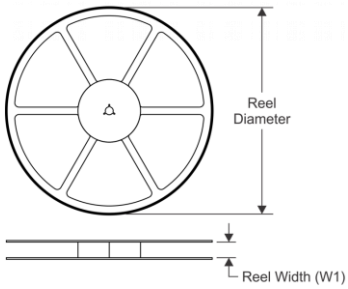
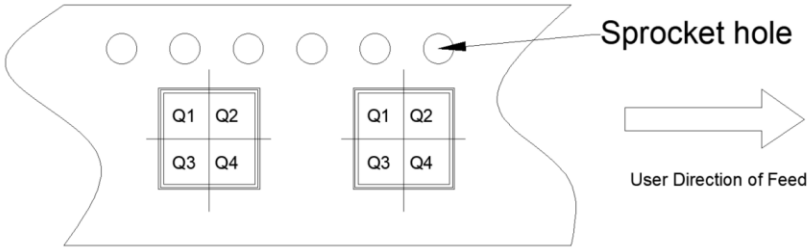
TAPE AND REEL INFORMATION

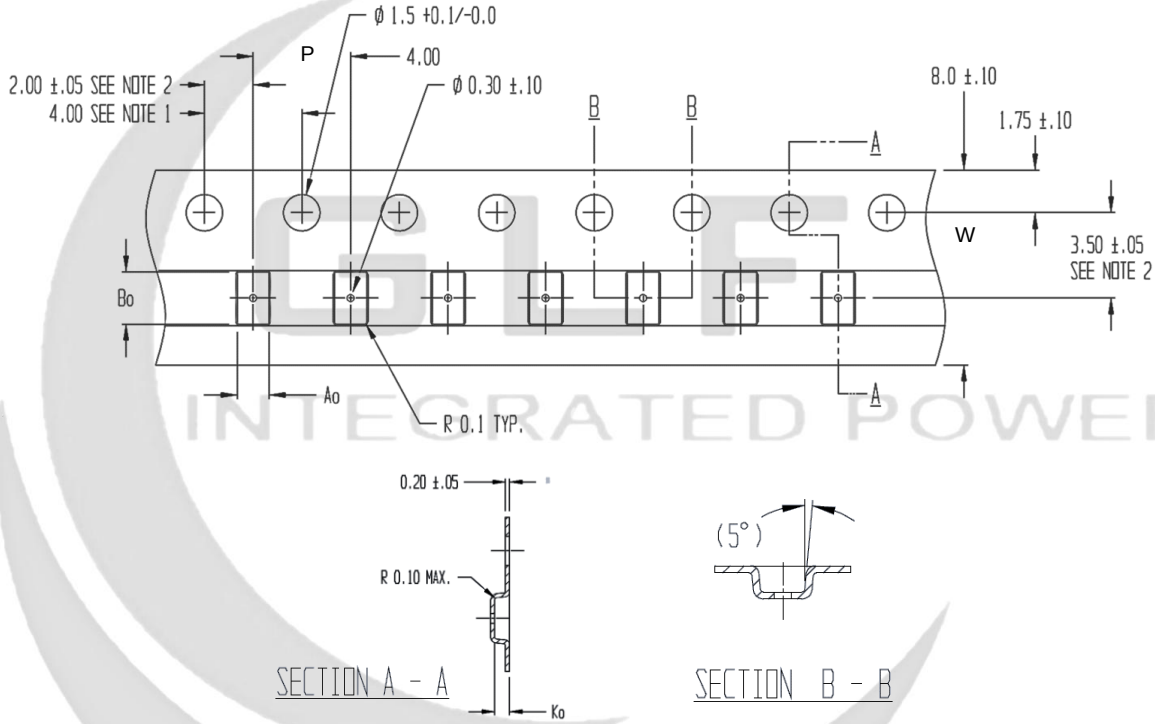
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF4013-SA7	WLCSP	15	3000	180	9	1.32	2.15	0.77	4	8	Q2

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

K0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

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SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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