GLF1595T, GLF1595LT

1 A Ultra-Low Input Voltage Power Load Switch

Preliminary Specification

DESCRIPTION

The GLF1595T and GLF1595LT are fully integrated 1 A load switches. The device is ideal for the mobile computing and data storage markets as a high-performance solution for load switch applications.

The GLF1595T and GLF1595LT support ultra-low VIN range applications, with an input supply voltage range of 0.1 V to 3.3 V and require an additional VBIAS power supply.

The GLF1595T and GLF1595LT are available in a ultra-thin wafer level chip scale package (WLCSP) measuring 0.67 mm x 1.02 mm x 0.35 mm with a 0.35 mm pitch. This allows the user to save board space.

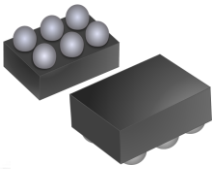
FEATURES

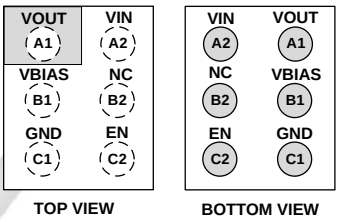
- Ultra-Low Input Voltage Range, V_{IN}:
  - 0.1 V to 3.3 V
- Supply Voltage Range, V_{BIAS}: V_{IN}+2 V to 5.5 V
- Ultra-Low Quiescent Current, I_{Q_BIAS}
  - 10 nA Typ. at V_{IN} = 0.1 V, V_{BIAS} = 2.1 V
  - 14 nA Typ. at V_{IN} = 3.3 V, V_{BIAS} = 5.5 V
- Shutdown Current, I_{SD_BIAS}
  - 14 nA Typ. at V_{BIAS} = 5.5 V
- Shutdown Current, I_{SD_VIN}
  - 7 nA Typ. at V_{IN} = 5.5 V
- Low On-Resistance, R_{ON}
  - 39 mΩ Typ. at V_{IN} = 0.1 V, V_{BIAS} = 2.1 V
  - 68 mΩ Typ. at V_{IN} = 3.3 V, V_{BIAS} = 5.5 V
- 1.0 A Maximum Continuous Output Current
- Reverse Current Blocking When Disabled
- Output Discharge Switch
- Operating Temperature Range
  - 40 °C to + 85 °C

APPLICATIONS

- Smart Doorbell
- Portable Devices
- Ultra-Low-Power AI System Devices
- Laptop, Solid State Drive (SSD)
- Set-Top Box

PACKAGE





0.67 mm x 1.02 mm x 0.35 mm Thin WLCSP

APPLICATION DIAGRAM

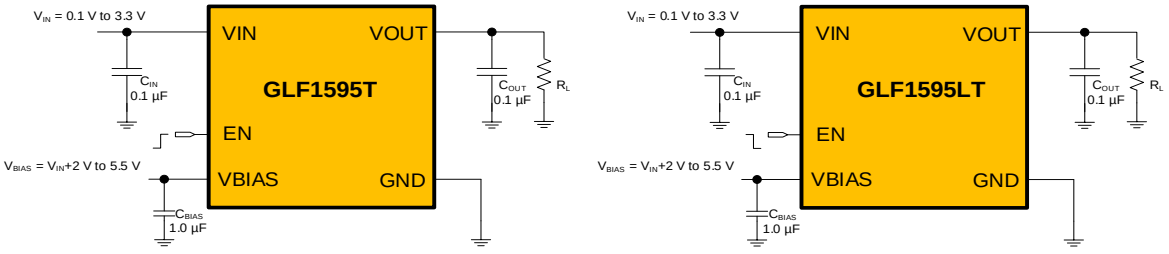


Figure 1. Application Diagram

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DEVICE ORDERING INFORMATION

Part Number	Top Mark	R_{ON} (Typ.) V_{IN}=0.1 V	Output Discharge (Typ.)	EN Activity	Package
GLF1595T-S97	HY	39 mΩ	150 Ω	High	0.67 mm x 1.02 mm x 0.35 mm Thin WLCSP
GLF1595LT-S97	JY			Low	

FUNCTIONAL BLOCK DIAGRAM

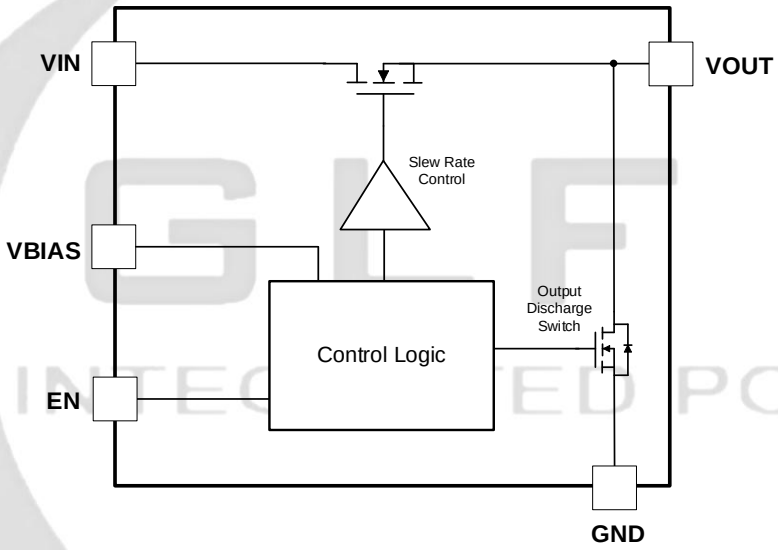

Figure 2. Functional Block Diagram

PIN CONFIGURATION

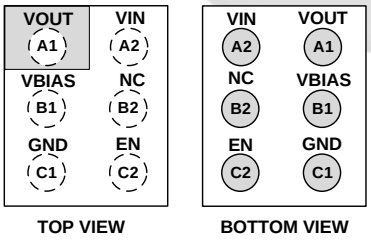

Figure 3. 0.67 mm x 1.02 mm x 0.35 mm

PIN DEFINITION

Pin #	Name	Description
A1	VOUT	Switch Output
A2	VIN	Switch Input.
B2	NC	No connection required. Keep floating or connect to GND
B1	VBIAS	Supply Voltage for IC
C1	GND	Ground
C2	EN	Enable control pin. Do not leave the EN pin floating

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ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{BIAS}, V_{EN}	Each Pin Voltage Range to GND		- 0.3	6	V
I_{OUT}	Maximum Continuous Output Current			1	A
T_{STG}	Storage Temperature		- 65	150	°C
T_J	Maximum Junction Temperature			150	°C
T_A	Operating Ambient Temperature Range		- 40	+ 85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			80	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	± 2		kV
		Charged Device Model, JESD22-C101	± 2		

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.1 V to 3.3 V, V_{BIAS} = V_{IN}+2 V, C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 0.1 µF, T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
I_{Q_BIAS}	V_{BIAS} Quiescent Current	V_{BIAS} = 2.1 V, EN = Enable, I_{OUT} = 0 mA	V_{IN} = 0.1 V		10		nA
			V_{IN} = 0.1 V, T_A = 85 °C (2)		165		
		V_{BIAS} = 3.3 V, EN = Enable, I_{OUT} = 0 mA	V_{IN} = 0 V to 1.3 V		11		
			V_{IN} = 0 V to 1.3 V, T_A = 85 °C (2)		177		
		V_{BIAS} = 5.5 V, EN = Enable, I_{OUT} = 0 mA	V_{IN} = 0 V to 3.3 V		14		
			V_{IN} = 0 V to 3.3 V, T_A = 85 °C (2)		216		
I_{SD_BIAS}	V_{BIAS} Shutdown Current	V_{BIAS} = 2.1 V, V_{EN} = GND (GLF1595T), V_{EN} = V_{BIAS} (GLF1595LT)			9		nA
		V_{BIAS} = 3.3 V, V_{EN} = GND (GLF1595T), V_{EN} = V_{BIAS} (GLF1595LT)			10		
		V_{BIAS} = 5.5 V, V_{EN} = GND (GLF1595T), V_{EN} = V_{BIAS} (GLF1595LT)	T_A = 25 °C		14		
			T_A = 85 °C (2)		210		
I_{SD_VIN}	V_{IN} Shutdown Current	V_{IN} = 0.1 V, EN = Disable, V_{BIAS} = V_{IN}+2 V to 5.5 V			1		nA
		V_{IN} = 3.3 V, EN = Disable, V_{BIAS} = V_{IN}+2 V to 5.5 V			4		
		V_{IN} = 5.5 V, EN = Disable, V_{BIAS} = 5.5 V	T_A = 25 °C		7		
			T_A = 85 °C (2)		235		
I_{Q_VIN}	V_{IN} Quiescent Current	V_{IN} = 0.1 V, EN = Enable, V_{BIAS} = V_{IN}+2 V to 5.5 V			1		nA
		V_{IN} = 1.0 V, EN = Enable, V_{BIAS} = V_{IN}+2 V to 5.5 V			4		
		V_{IN} = 3.3 V, EN = Enable, V_{BIAS} = 5.5 V	T_A = 25 °C		7		
			T_A = 85 °C (2)		42		
R_{ON}	On-Resistance	V_{IN} = 0.1 V, I_{OUT} = 200 mA	V_{BIAS} = 2.1 V, T_A = 25 °C		39		mΩ
			V_{BIAS} = 2.1 V, T_A = 85 °C (2)		50		
		V_{IN} = 1.5 V, I_{OUT} = 200 mA	V_{BIAS} = 3.5 V, T_A = 25 °C		29	45	
			V_{BIAS} = 3.5 V, T_A = 85 °C (2)		35		
		V_{IN} = 3.3 V, I_{OUT} = 200 mA	V_{BIAS} = 5.5 V, T_A = 25 °C		68	52	mΩ
			V_{BIAS} = 5.5 V, T_A = 85 °C (2)		135		

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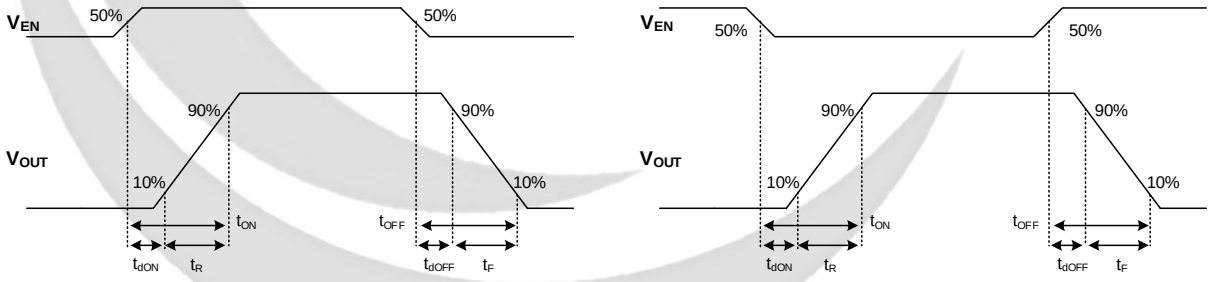
ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 0.1 V to 3.3 V, V_{BIAS} = V_{IN}+2 V, C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 0.1 µF, T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{DSC}	Output Discharge Resistance	V_{BIAS} = 2.1 V to 5.5 V, V_{EN} = GND (GLF1595T), V_{EN} = V_{BIAS} (GLF1595LT), I_{FORCE} = 10 mA	100	150	200	Ω
I_{EN}	EN Pin Leakage	V_{EN} = 5.5 V		1		nA
VIH	EN Input Logic High Voltage	VBIAS = 2.1 V to 5.5 V	1			V
VIL	EN Input Logic Low Voltage	VBIAS = 2.1 V to 5.5 V			0.2	
Switching Characteristics (1), (2)						
t_{dON}	Turn-On Delay	V_{IN} = 0.6 V, V_{BIAS} = 3.3 V, R_{OUT} = 150 Ω, C_{OUT} = 0.1 µF		170		µs
t_R	V_{OUT} Rise Time			210		
t_{dOFF}	Turn-Off Delay			1.2		
t_F	V_{OUT} Fall Time			14		
t_{dON}	Turn-On Delay	V_{IN} = 1.2 V, V_{BIAS} = 3.3 V, R_{OUT} = 150 Ω, C_{OUT} = 0.1 µF		190		
t_R	V_{OUT} Rise Time			450		
t_{dOFF}	Turn-Off Delay			1		
t_F	V_{OUT} Fall Time			13		
t_{dON}	Turn-On Delay	V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, R_{OUT} = 150 Ω, C_{OUT} = 0.1 µF		200		
t_R	V_{OUT} Rise Time			960		
t_{dOFF}	Turn-Off Delay			1		
t_F	V_{OUT} Fall Time			14		

Notes: 1. t_{ON} = t_{dON} + t_R, t_{OFF} = t_{dOFF} + t_F
2. By design; characterized, not production tested



GLF1595T **GLF1595LT**

Figure 4. Timing Diagram

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TYPICAL PERFORMANCE CHARACTERISTICS

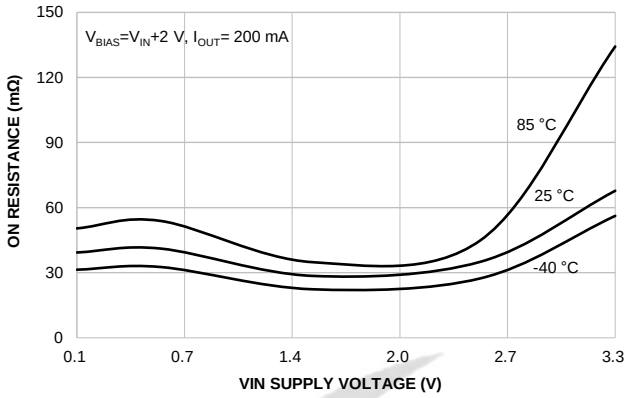

Figure 5. On-Resistance vs. VIN Supply Voltage

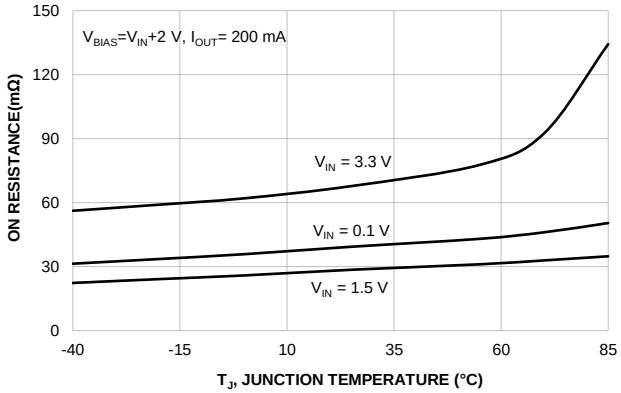

Figure 6. On-Resistance vs. Temperature

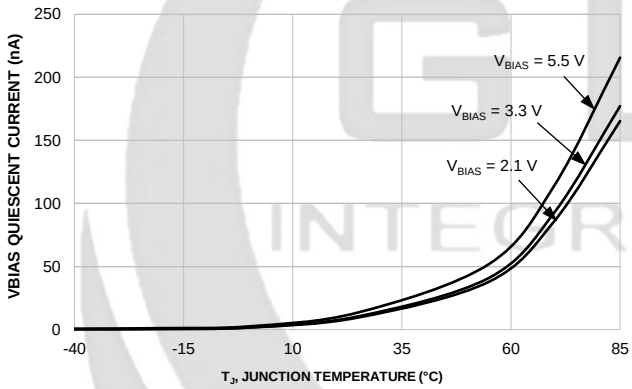

Figure 7. VBIAS Quiescent Current vs. Temperature

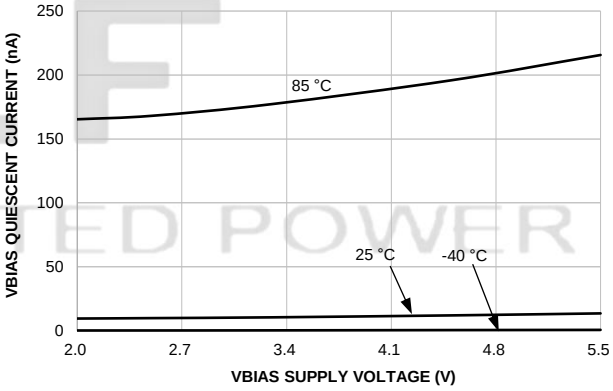

Figure 8. VBIAS Quiescent Current vs. VBIAS

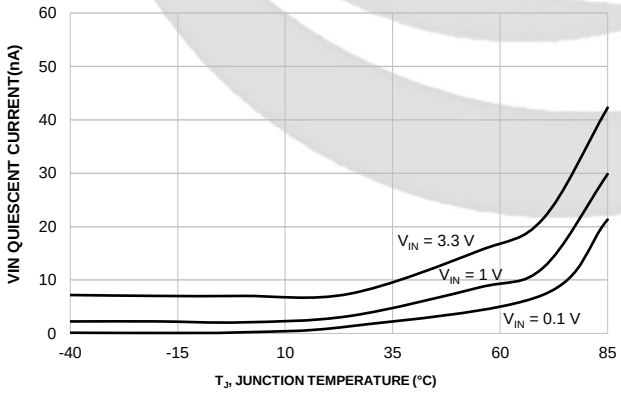

Figure 9. VIN Quiescent Current vs. Temperature

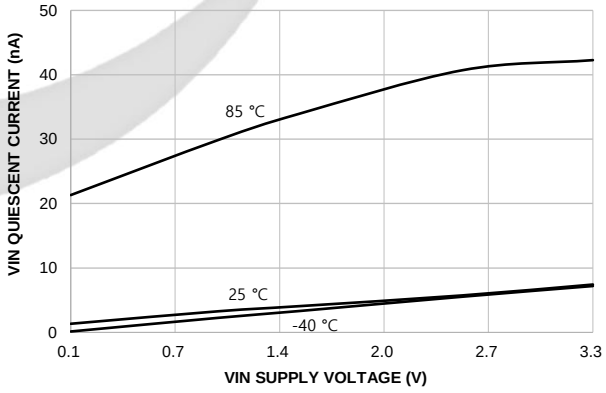

Figure 10. VIN Quiescent Current vs. VIN Supply Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

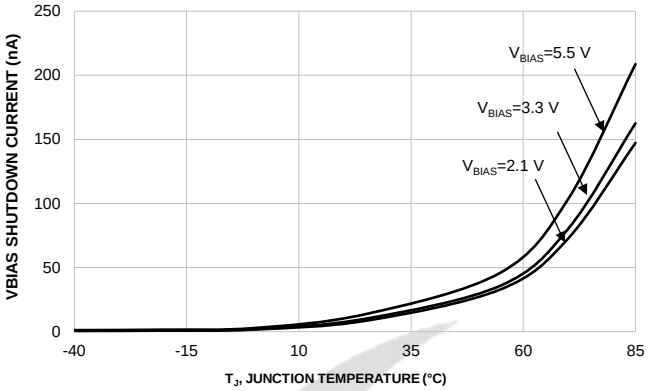

Figure 11. VBIAS Shutdown Current vs. Temperature

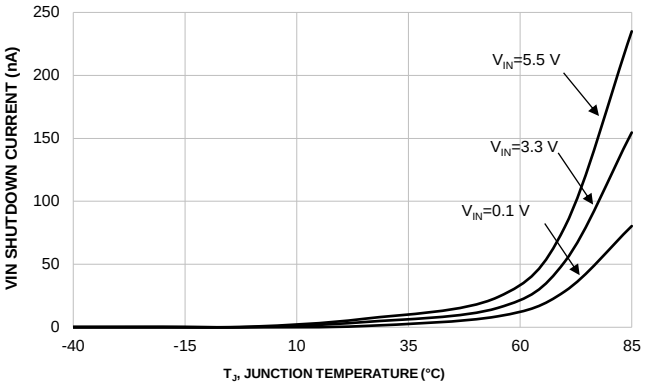

Figure 12. VIN Shutdown Current vs. Temperature

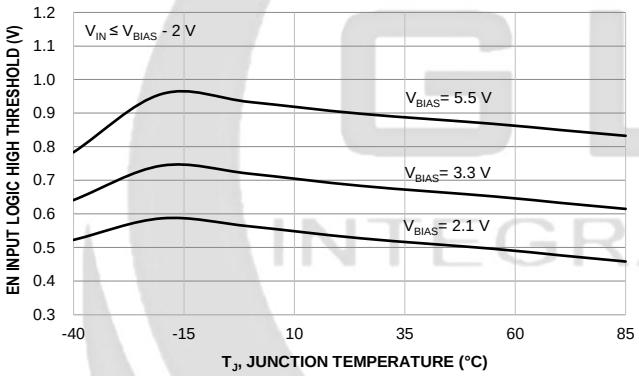

Figure 13. EN Input Logic High Threshold vs. Temperature

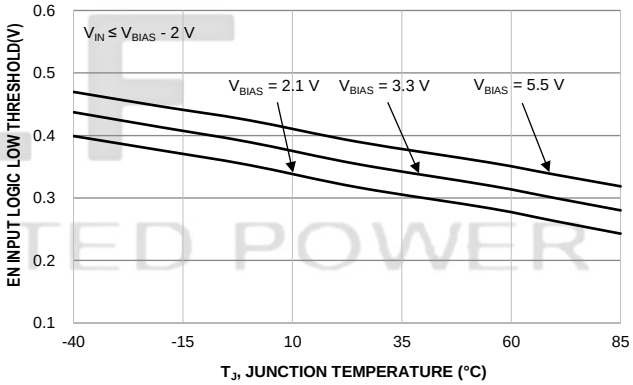

Figure14. EN Input Logic Low Threshold vs. Temperature

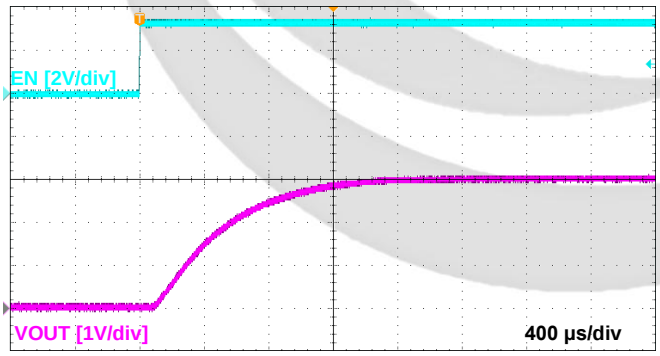

Figure 19. Turn-On Response
V_{IN}=3V, V_{BIAS}= 5 V, C_{OUT}=0.1 µF, R_L=150 Ω, GLF1595T

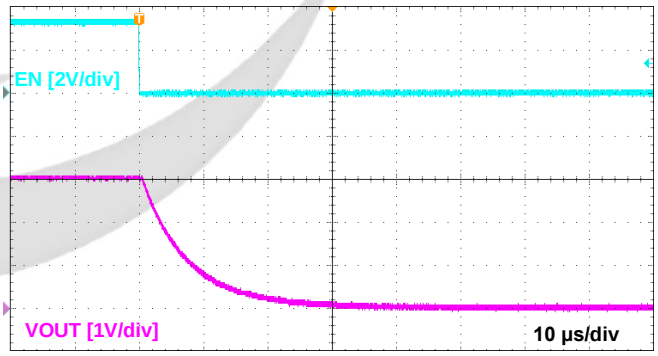

Figure 20. Turn-Off Response
V_{IN}=3V, V_{BIAS}=5 V, C_{OUT}=0.1 µF, R_L=150 Ω, GLF1595T

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

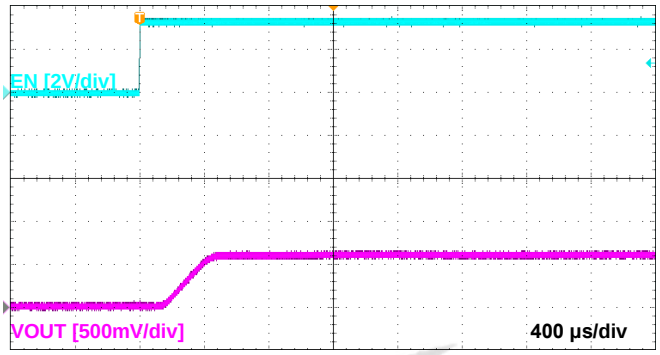

Figure 21. Turn-On Response
V_{IN}=0.6 V, V_{BIAS}= 3.3 V, C_{OUT}=0.1 µF, R_L=150 Ω, GLF1595T

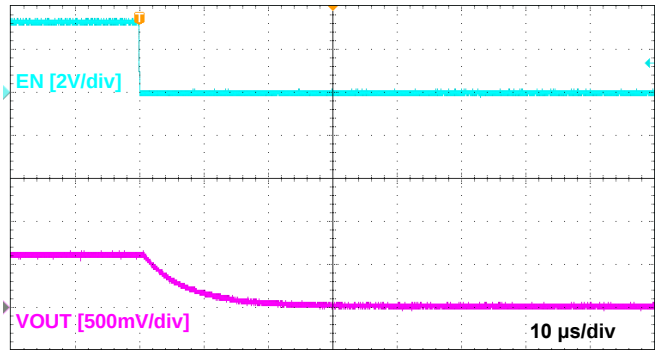

Figure 22. Turn-Off Response
V_{IN}=0.6 V, V_{BIAS}= 3.3 V, C_{OUT}=0.1 µF, R_L=150 Ω, GLF1595T

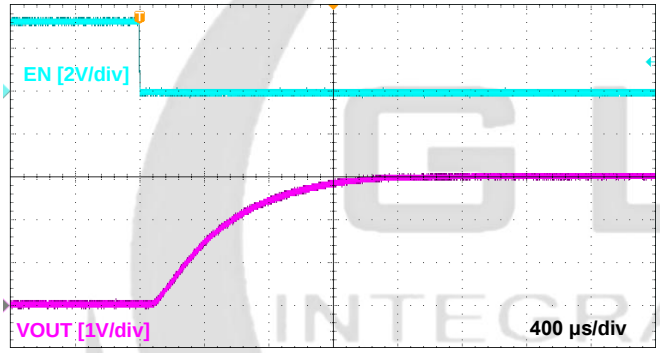

Figure 23. Turn-On Response
V_{IN}=3V, V_{BIAS}= 5 V, C_{OUT}=0.1 µF, R_L=150 Ω, GLF1595LT

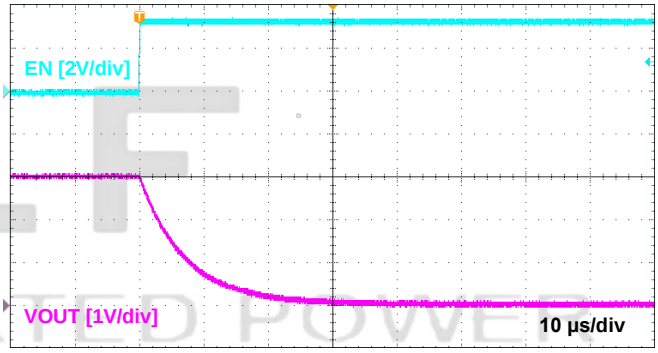

Figure 24. Turn-Off Response
V_{IN}=3V, V_{BIAS}=5 V, C_{OUT}=0.1 µF, R_L=150 Ω, GLF1595LT

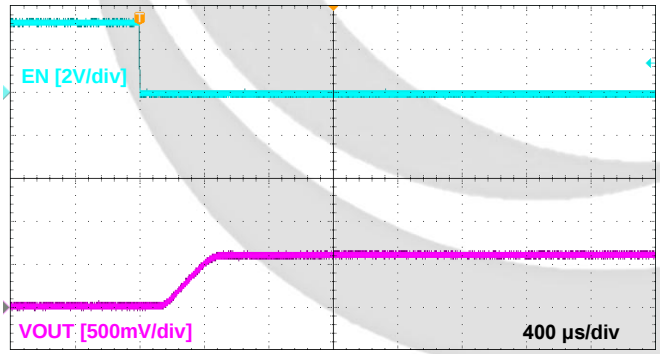

Figure 25. Turn-On Response
V_{IN}=0.6 V, V_{BIAS}= 3.3 V, C_{OUT}=0.1 µF, R_L=150 Ω, GLF1595LT

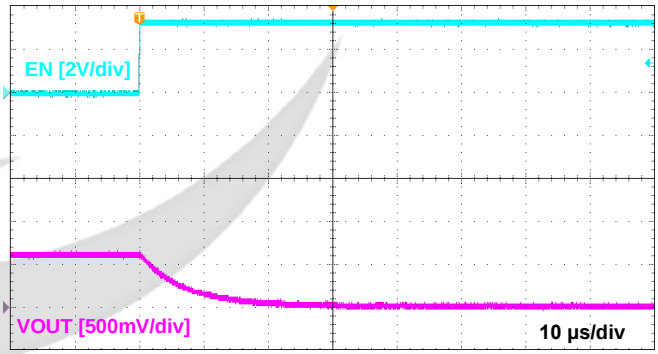

Figure 26. Turn-Off Response
V_{IN}=0.6 V, V_{BIAS}= 3.3 V, C_{OUT}=0.1 µF, R_L=150 Ω, GLF1595LT

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APPLICATION INFORMATION

The GLF1595T and GLF1595LT are ultra-efficient integrated 1 A load switches with Low input voltage. The device is capable of operating over a wide input range from 0.1 V_{IN} to 3.3 V_{IN} with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power supply.

Input and Output Capacitor

A minimum 0.1 µF input capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop. Also, a minimum 0.1 µF output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pin.

EN pin

The GLF1595T can be activated by EN pin high and the GLF1595LT can be activated by EN pin low. Note: The EN pin does not have an internal pull-up or pull-down resistor, so do not leave the EN pin floating

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will be better to reduce parasitic effects at dynamic operations and improve thermal performance at high load current.

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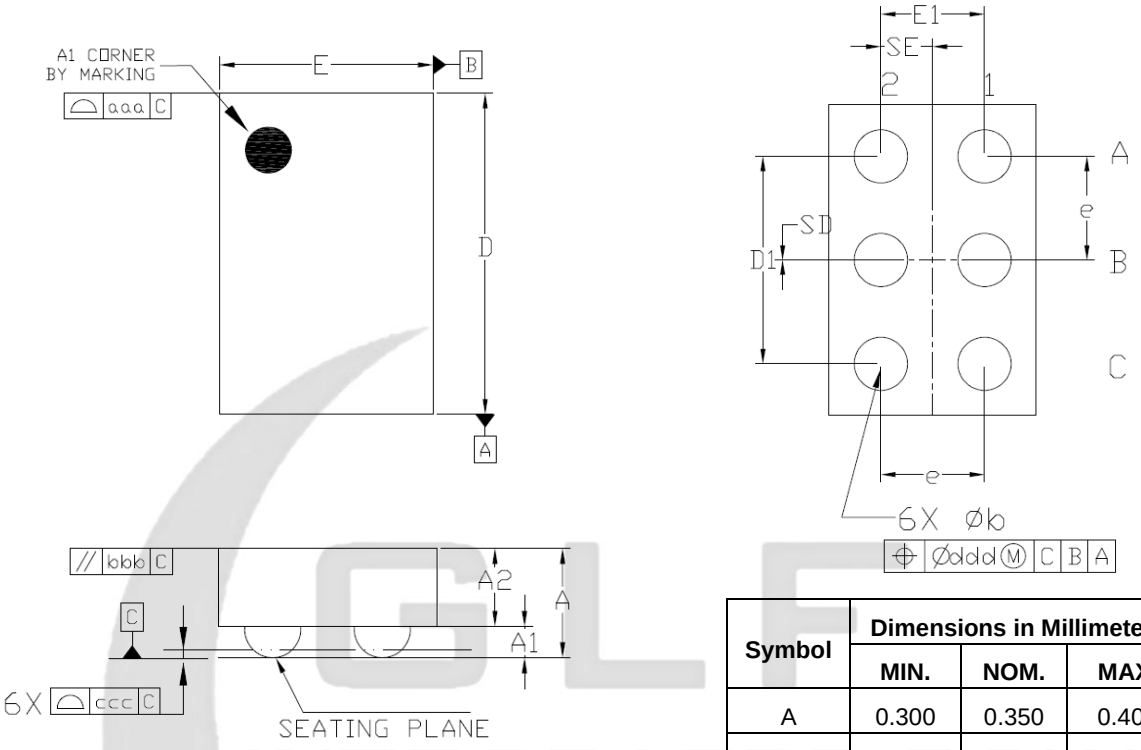
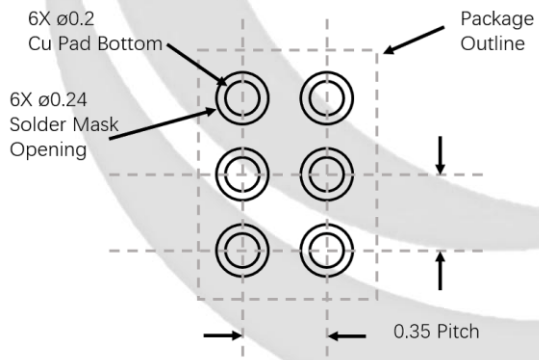
PACKAGE OUTLINE



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	0.300	0.350	0.400
A1	0.075	0.100	0.125
A2	0.225	0.250	0.275
D	1.005	1.020	1.035
E	0.655	0.670	0.685
D1	0.650	0.700	0.750
E1	0.300	0.350	0.400
b	0.175	0.210	0.245
e	0.350 BSC		
SD	0.000 BSC		
SE	0.175 BSC		
Tol. of Form & Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint



Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14,5M-1994

PACKAGING INFORMATION

Part Number	Package	Pins	Top Mark	Moisture Sensitivity Level	Environmental Information
GLF1595T-S97	Thin WLCSP	6	HY	MSL1	ROHS+HF
GLF1595LT-S97			JY		

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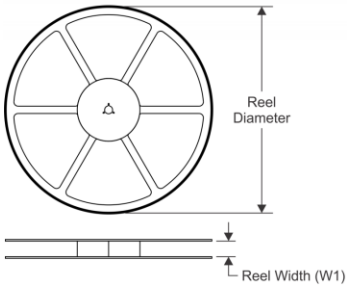
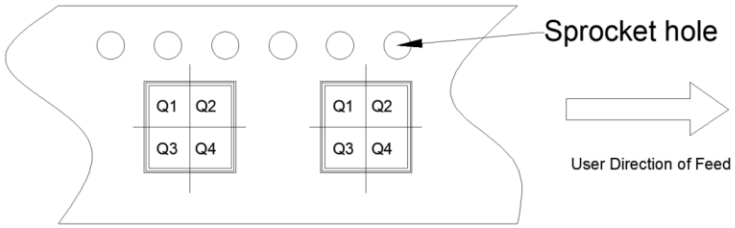
TAPE AND REEL INFORMATION

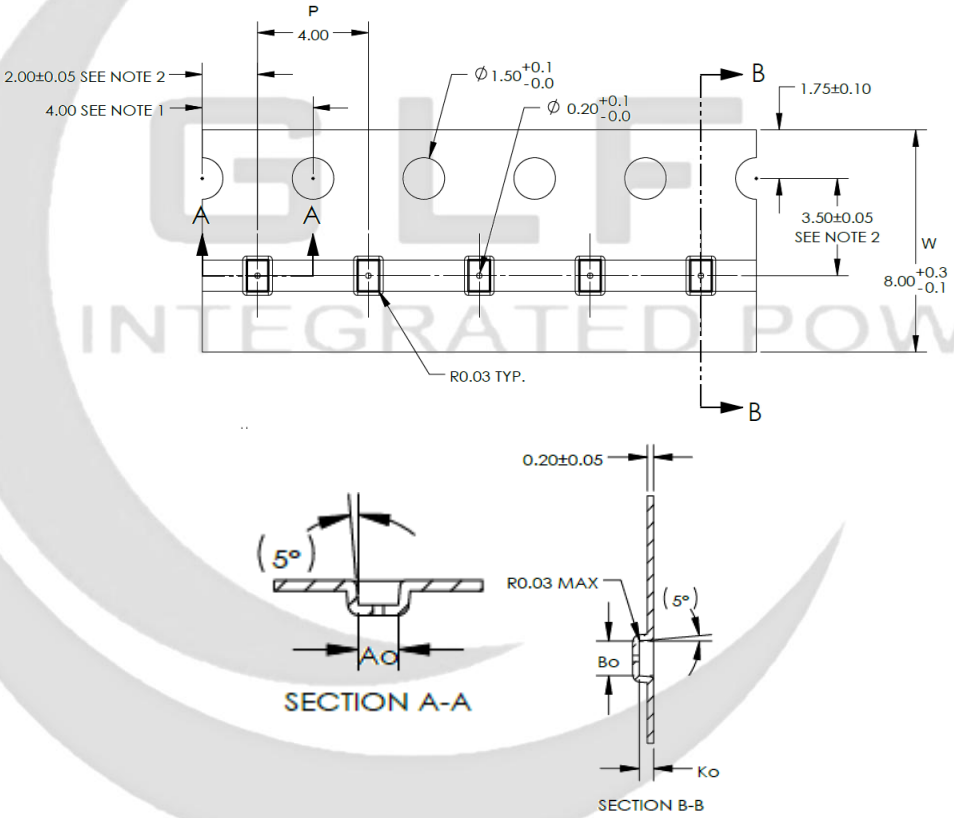
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF1595T-S97	WLCSP	6	4000	180	9	0.77	1.12	0.47	4	8	Q1
GLF1595LT-S97											

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

K0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

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SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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