

DESCRIPTION

The GLF71300H and GLF71301H are an ultra-efficiency, 2.0 A rated, Load Switch with integrated slew rate control. The best in class efficiency makes it an ideal choice for use in IoT, mobile, and wearable electronics.

The GLF71300H and GLF71301H support the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF71300H and GLF71301H slew rate control specifically limits inrush current during turn-on to minimize voltage droop.

The GLF71300H and GLF71301H support an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

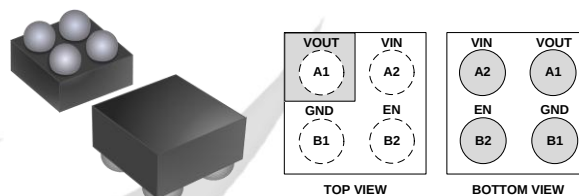
FEATURES

- Ultra-Low I_Q : 1 nA Typ at 5.5 V_{IN}
- Ultra-Low I_{SD}: 19 nA Typ at 5.5 V_{IN}
- Low R_{ON} : 34 mΩ Typ at 5.5 V_{IN}
- I_{OUT} Max : 2.0 A
- Wide Input Range: 1.1 V to 5.5 V
6 V_{ABS} Max
- Controlled Rise Time: 430 μs at 3.3V_{IN}
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- Wide Operating Temperature Range:
- 40 °C to 105 °C
- Ultra-Small: 0.77 mm x 0.77 mm

APPLICATIONS

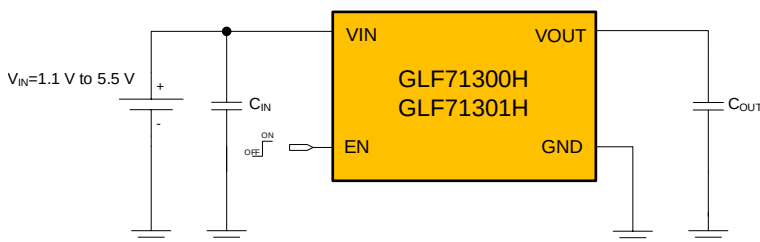
- Wearables
- Data Storage, SSD
- Mobile Devices
- Low Power Subsystems

PACKAGE



0.77 mm x 0.77 mm x 0.46 mm WLCSP

APPLICATION DIAGRAM



GLF71300H, GLF71301H

GLF Nano-Current Consumed, I_QSmart™ Power Load Switch with Slew Rate Control
INTEGRATED POWER

DEVICE INFORMATION

Part Number	Top Mark	V _{out} Rise Time at 3.3V _{in} (Typ)	R _{ON} (Typ) at 5.5 V	Output Discharge	EN Activity	Package
GLF71300H	h	430 μs	34 mΩ	NA	High	0.77 mm x 0.77 mm x 0.46 mm WLCSP
GLF71301H	P			85 Ω		

FUNCTIONAL BLOCK DIAGRAM

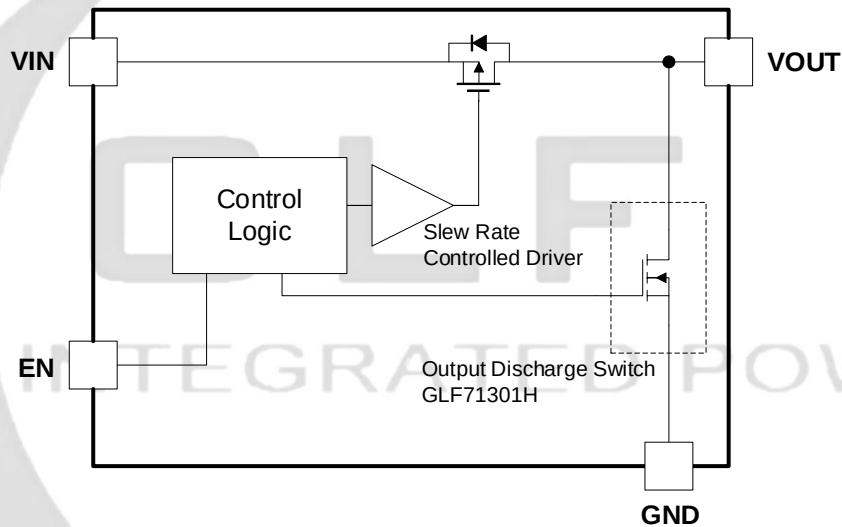


Figure 1. Functional Block Diagram

PIN CONFIGURATION

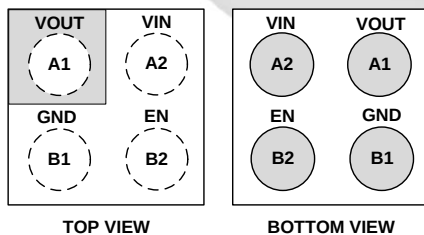


Figure 2. 0.77 mm x 0.77 mm x 0.46 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	V _{OUT}	Switch Output
A2	V _{IN}	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch. The EN pin has an internal pull-down resistor

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND	- 0.3	6	V
I_{OUT}	Maximum Continuous Switch Current		2	A
T_{STG}	Storage Temperature	- 65	150	°C
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	- 40	105	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (board dependent)		110	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6	kV
		Charged Device Model, JESD22-C101	2	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.1	5.5	V
T_A	Ambient Operating Temperature	- 40	105	°C

ELECTRICAL CHARACTERISTICS

Values are at $V_{IN} = 3.3\text{ V}$ and $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
I _Q	Quiescent Current ⁽¹⁾	EN = Enable, V _{IN} = 5.5 V, I _{OUT} = 0 mA			1		nA
		EN = Enable, V _{IN} = 5.5 V, I _{OUT} = 0 mA, Ta = 85 °C ⁽⁴⁾			12		
		EN = Enable, V _{IN} = 5.5 V, I _{OUT} = 0 mA, Ta = 105 °C ⁽⁴⁾			28		
I _{SD}	Shutdown Current	EN = Disable, I _{OUT} = 0 mA, V _{IN} = 1.1 V			3		nA
		EN = Disable, I _{OUT} = 0 mA, V _{IN} = 1.8 V			4		
		EN = Disable, I _{OUT} = 0 mA, V _{IN} = 3.3 V			6		
		EN = Disable, I _{OUT} = 0 mA, V _{IN} = 4.5 V			9		
		EN = Disable, I _{OUT} = 0 mA, V _{IN} = 5.5 V			19	50	
		EN = Disable, I _{OUT} = 0 mA, V _{IN} = 5.5 V, Ta = 55 °C ⁽⁴⁾			110		
		EN = Disable, I _{OUT} = 0 mA, V _{IN} = 5.5 V, Ta = 85 °C ⁽⁴⁾			600		
		EN = Disable, I _{OUT} = 0 mA, V _{IN} = 5.5 V, Ta = 105 °C ⁽⁴⁾			1300		
R _{ON}	On-Resistance	V _{IN} = 5.5 V, I _{OUT} = 500 mA	Ta = 25 °C		34	47	mΩ
			Ta = 85 °C ⁽⁴⁾		40		
			Ta = 105 °C ⁽⁴⁾		42		
		V _{IN} = 3.3 V, I _{OUT} = 500 mA	Ta = 25 °C		42	56	
			Ta = 85 °C ⁽⁴⁾		50		
			Ta = 105 °C ⁽⁴⁾		53		
		V _{IN} = 1.8 V, I _{OUT} = 300 mA	Ta = 25 °C		68		
		V _{IN} = 1.2 V, I _{OUT} = 100 mA	Ta = 25 °C		125		
		V _{IN} = 1.1 V, I _{OUT} = 100 mA	Ta = 25 °C		155		

ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{DSC}	Output Discharge Resistance	EN = Disable , $I_{FORCE} = 10\text{ mA}$, GLF71301H Only	70	85	100	Ω
V_{IH}	EN Input Logic High Voltage	$V_{IN} = 1.1\text{ V to }1.8\text{ V}$	0.9			V
		$V_{IN} = 1.8\text{ V to }5.5\text{ V}$	1.2			V
V_{IL}	EN Input Logic Low Voltage	$V_{IN} = 1.1\text{ V to }1.8\text{ V}$			0.3	V
		$V_{IN} = 1.8\text{ V to }5.5\text{ V}$			0.4	V
R_{EN}	EN Internal resistance	Internal Pull-down Resistance	7	10.1	13	$M\Omega$
I_{EN}	EN Current	$V_{EN} = 5.5\text{ V}$			0.8	μA

Switching Characteristics (2), (3), (4)

t_{dON}	Turn-On Delay	$R_L=150\ \Omega$, $C_{OUT}=0.1\ \mu\text{F}$		275		μs
t_R	V_{OUT} Rise Time			430		
t_{dOFF}	Turn-Off Delay	$R_L=150\ \Omega$, $C_{OUT}=0.1\ \mu\text{F}$, GLF71300H		1.9		
t_F	V_{OUT} Fall Time			29		
t_{dOFF}	Turn-Off Delay	$R_L=150\ \Omega$, $C_{OUT}=0.1\ \mu\text{F}$, GLF71301H		0.85		
t_F	V_{OUT} Fall Time			10.5		

Notes:

1. I_Q does not include the EN pin current through the pull-down resistor R_{PD} .
2. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$
3. Output discharge path is enabled during off.
4. By design; characterized, not production tested.

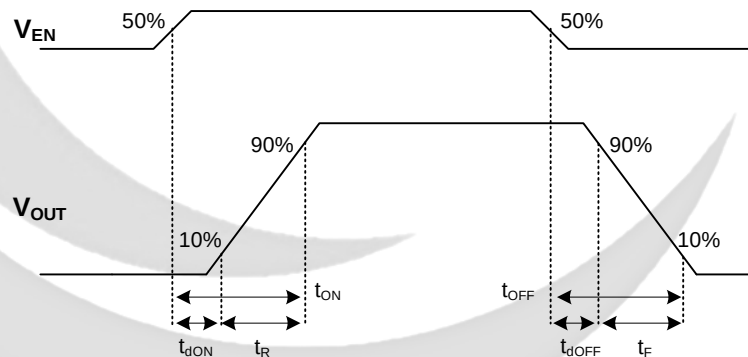
TIMING DIAGRAM


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

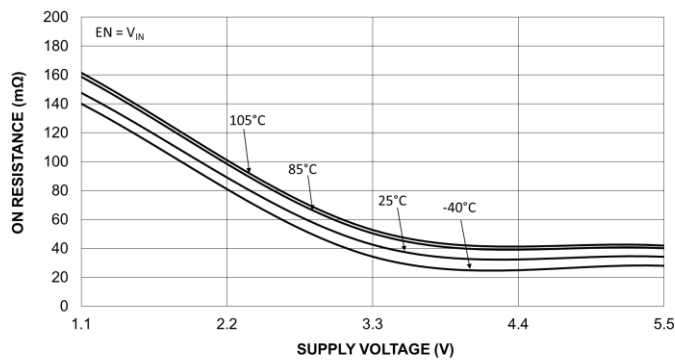


Figure 4. On-Resistance vs. Supply Voltage

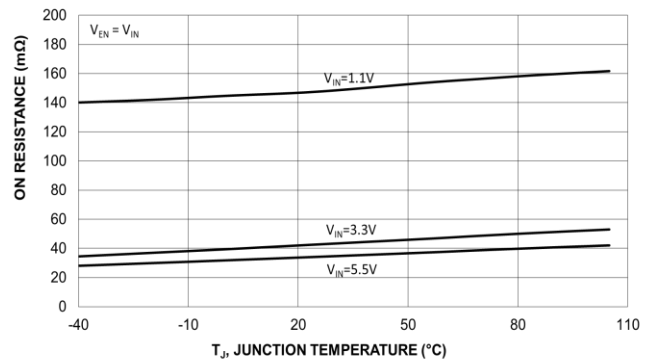


Figure 5. On-Resistance vs. Temperature

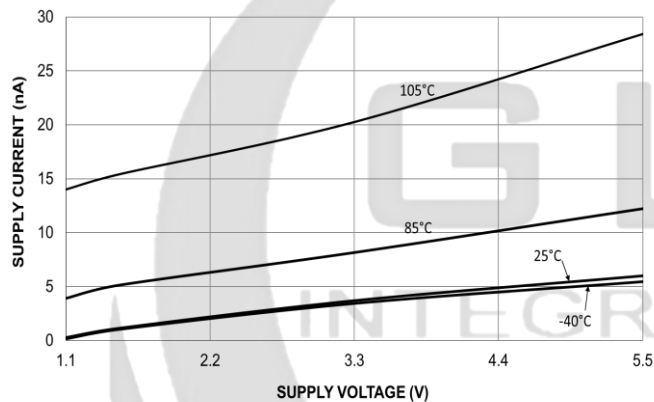


Figure 6. Quiescent Current vs. Supply Voltage

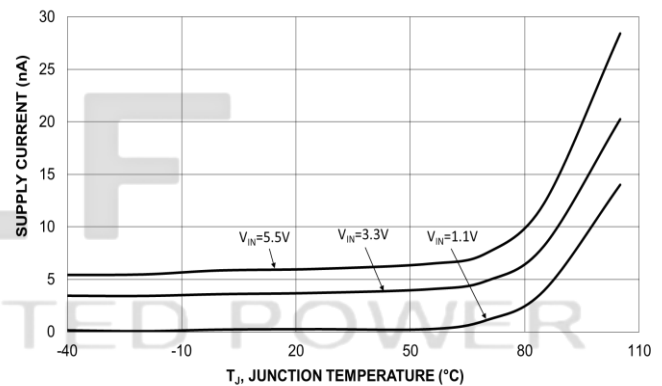


Figure 7. Quiescent Current vs. Temperature

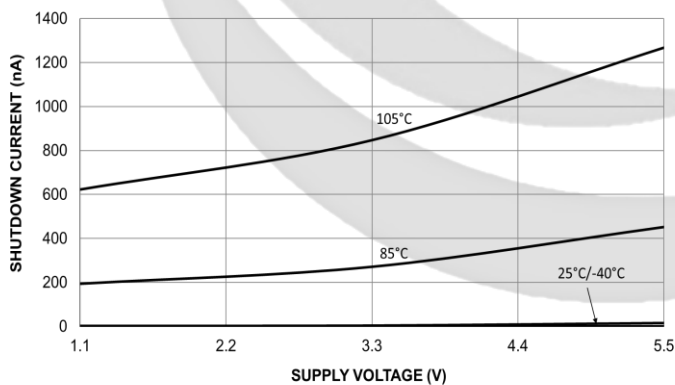


Figure 8. Shutdown Current vs. Supply Voltage

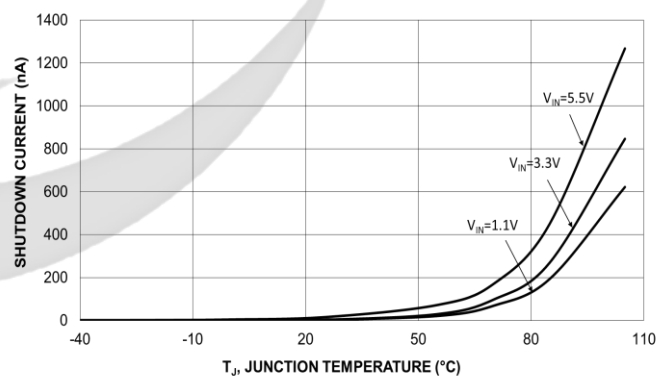


Figure 9. Shutdown Current vs. Temperature

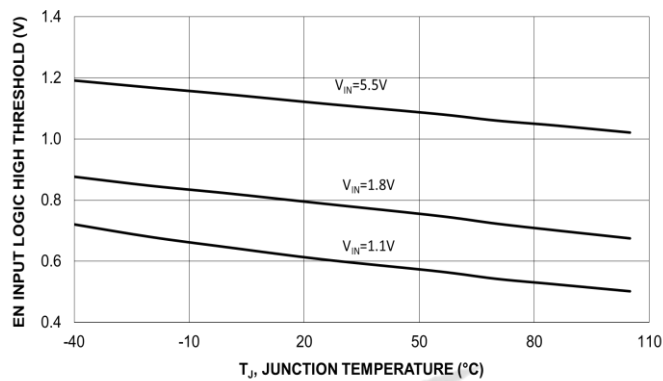
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)


Figure 10. EN Input Logic High Threshold Vs. Temperature

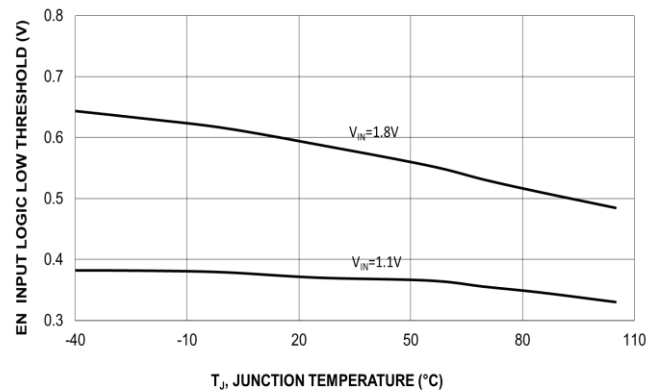


Figure 11. EN Input Logic Low Threshold Vs. Temperature

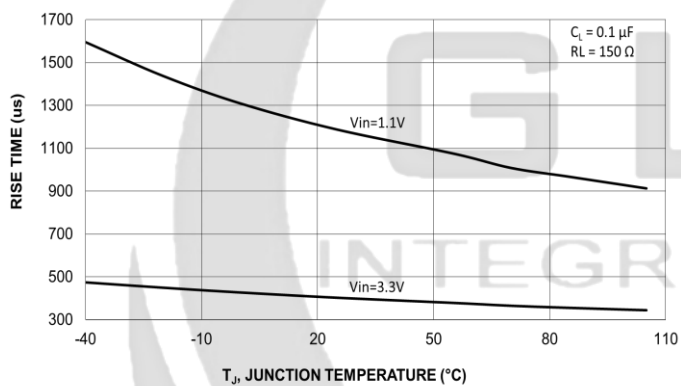
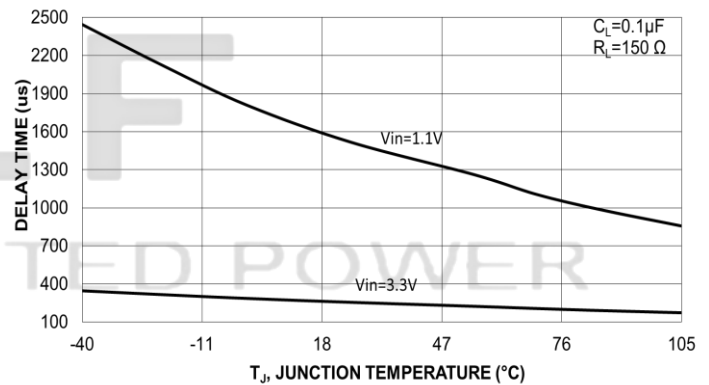

 Figure 12. V_{OUT} Rise Time vs. Temperature


Figure 13. Turn-On Delay Time vs. Temperature

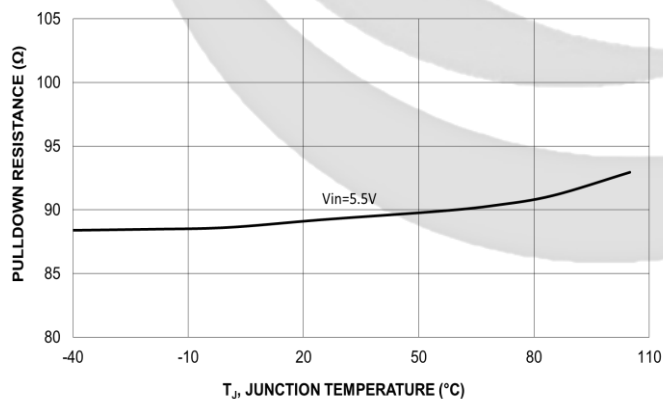


Figure 14. Pull-down Resistance (GLF71301H) vs. Temperature

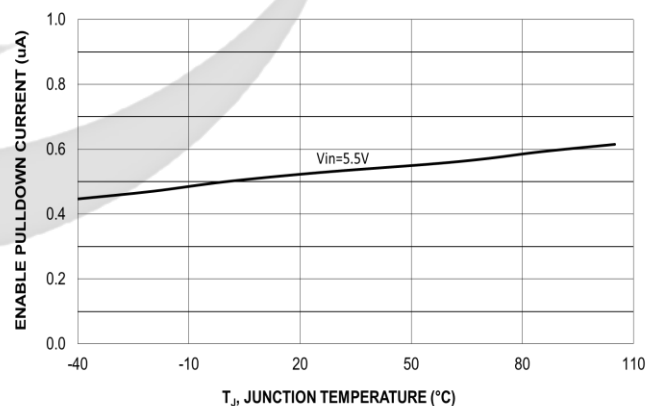


Figure 15. Enable Input Current vs. Temperature

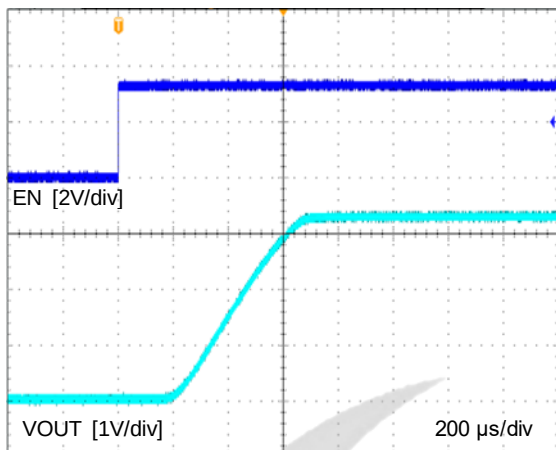
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)


Figure 16. Turn-On Response, GLF71300H
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=0.1\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

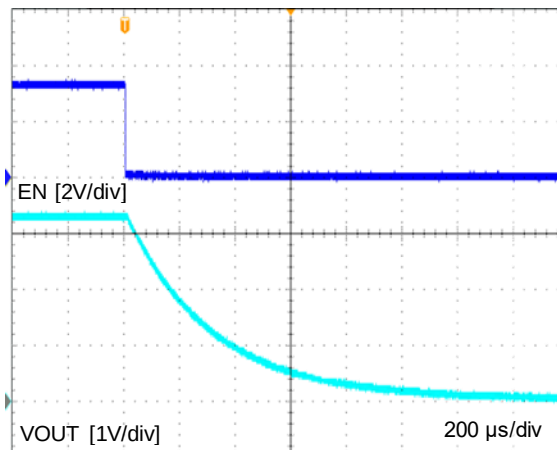


Figure 17. Turn-Off Response, GLF71300H
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=0.1\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

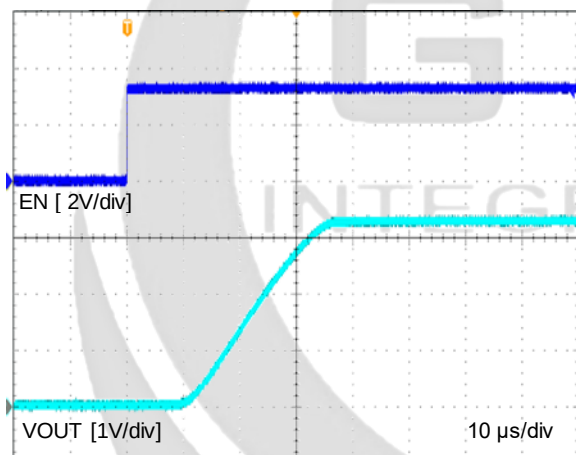


Figure 18. Turn-On Response, GLF71301H
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=0.1\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

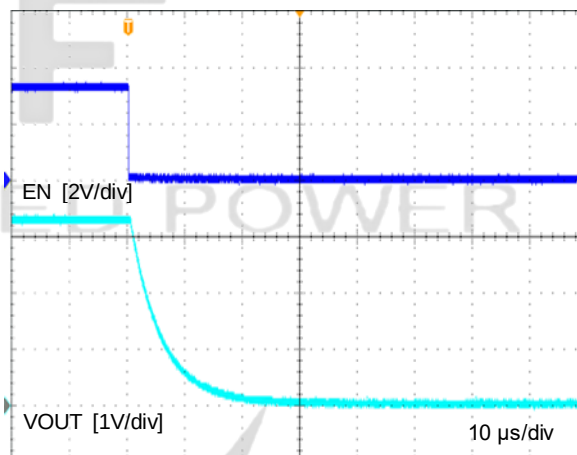


Figure 19. Turn-Off Response, GLF71301H
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=0.1\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

APPLICATION INFORMATION

The GLF71300H and GLF71301H are integrated 2.0 A, Ultra-Efficient I_QSmart™ Load Switch devices with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.77 mm x 0.77 mm x 0.46 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.4 mm pitch for manufacturability.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin the moment when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

EN pin

The GLF71300H and GLF71301H can be activated by EN pin high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

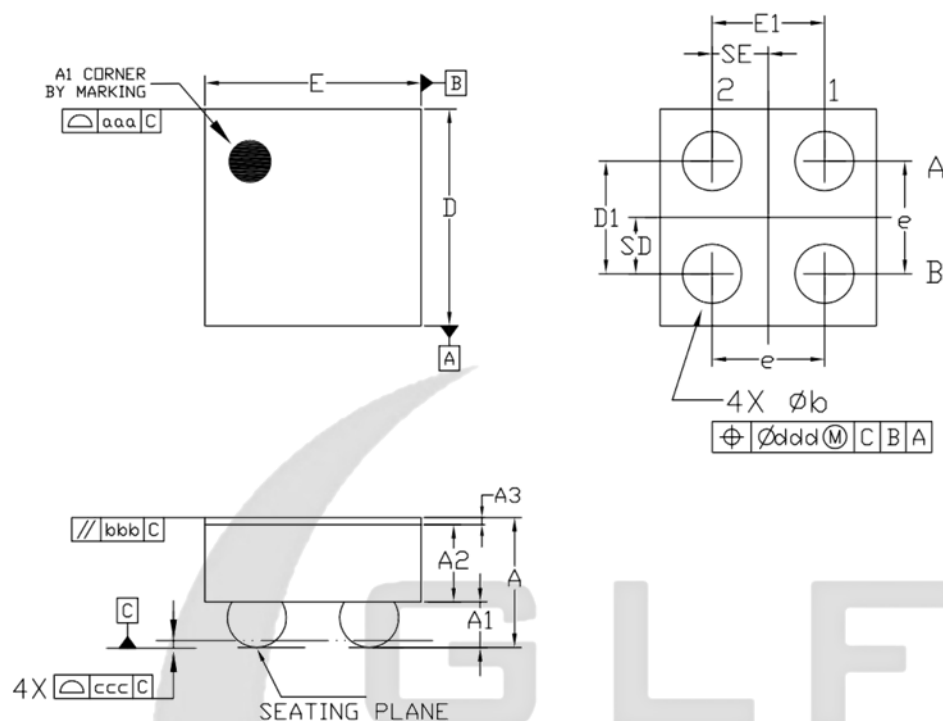
Output Discharge Function

The GLF71301H has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for V_{IN}, V_{OUT}, and GND will help reduce voltage drops and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

PACKAGE OUTLINE

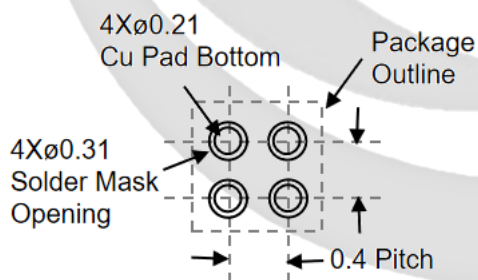


Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.410	0.460	0.510
A1	0.135	0.160	0.185
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	0.755	0.770	0.785
E	0.755	0.770	0.785
D1	0.350	0.400	0.450
E1	0.350	0.400	0.450
b	0.170	0.210	0.250
e	0.400 BSC		
SD	0.200 BSC		
SE	0.200 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint

Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

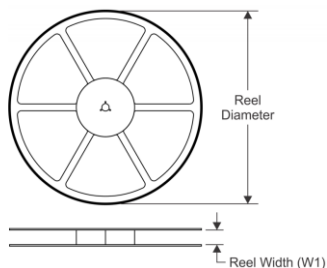


PACKAGING INFORMATION

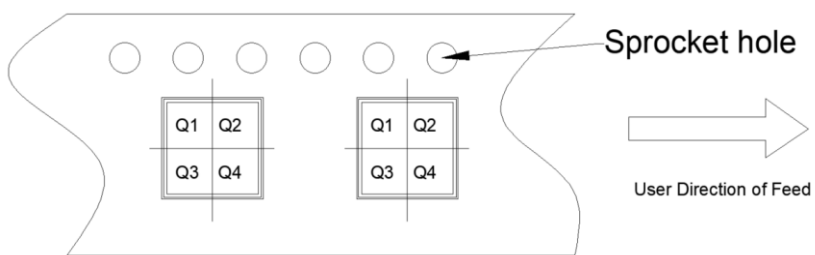
Part Number	Package	Pins	Pitch	Top Mark	Moisture Sensitivity Level	Environmental Information
GLF71300H	0.77 mm x 0.77 mm x 0.46 mm WLCSP	4	0.4 mm	h	MSL1	ROHS+HF
GLF71301H				P		

TAPE AND REEL INFORMATION

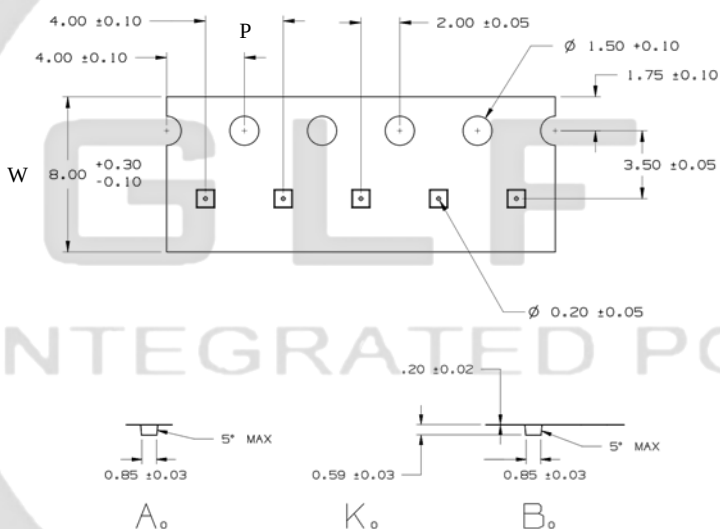
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF71300H	WLCSP	4	4000	180	9	0.85	0.85	0.59	4	8	Q1
GLF71301H											

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

K0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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