GLF70106

I2C Controlled 3A Buck Switch Charger with NVDC Power Path Management and OTG Output

Product Specification

Description

The GLF70106 is a highly integrated 3A switch-mode buck charger for single-cell Li-Ion and Li-polymer batteries, operating with an input voltage range of 4.0-13.5V and 1.5MHz switching frequency. It features NVDC system power path management, which separates the system load and charge current. Additionally, it supports system power-on even with a depleted battery.

The GLF70106 can support up to 3A charging current. It initate and conplete charging cycle without host control. The charging profile can be configured through I2C. The step of charge voltage is low to 10mV and the step of charge current is 20mA.

The GLF70106 is compatible with the BC1.2 and can automatically set the input current limit based on the input sources type.

The GLF70106 integrates an OTG function with 2.4A output capability, which can deliver power from the battery to other devices through a USB port.

The GLF70106 reverse operation supports Bypass Mode, which connects battery directly to the PMID pin via BATFET and HSFET. This mode enables extreme efficiency when powering external accessories and maximizes battery runtime.

Integrated high accuracy 12-bit ADC for voltage, current, NTC, die temperature monitoring.

The GLF70106 is available in packages of QFN2.5x3-18.

Applications

Smart watch/band and other wearable device
Mobile phone, tablet
Portable devices and accessory

Features

- 2.5uA quiescent current in standby mode
- 0.3uA quiescent current in ship mode
- High-efficiency switch-mode buck charger
  - Charging current up to 3A
  - >91.5% charge efficiency at 2A@5V
  - >90% charge efficiency at 2A@9V
- High accuracy charging profile
  - ±0.4% charge voltage regulation
  - ±5% charge current regulation@1.5A
  - Low termination current to 10mA
- Support USB On-The-Go (OTG) mode
  - Adjustable output from 4.6V to 9.52V
  - Up to 2.4A output
  - Soft-start up to 500uF capacitive load
  - Support reverse boost on PMID output
  - Bypass mode on PMID output for extreme efficiency
- NVDC power path management
  - Support 4.0V to 13.5V input voltage operation
  - Instant-On works with deeply discharged battery
  - Programmable input current limit (IINDPM) and input voltage limit (VINDPM)
- Safety and protection
  - Protection includes VBUS OVP, battery OVP/OCP, boost OVP/OCP
  - Charging safety timer
  - Thermal regulation and thermal shutdown
  - IEC62368-1 CB Certificate

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Typical Application Circuit

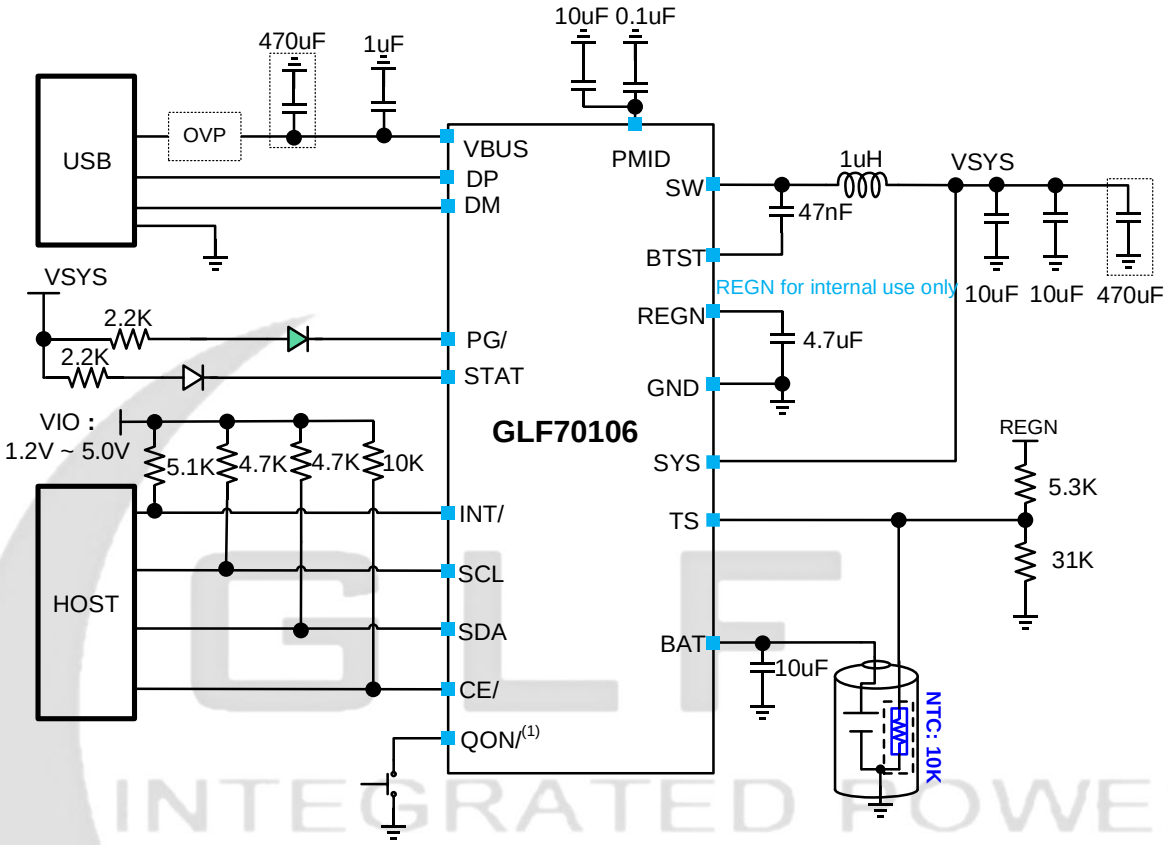


Figure 0-1. Typical Application Circuit

Note: (1)QON/ has internal pull-up

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Pin Configuration and Functions

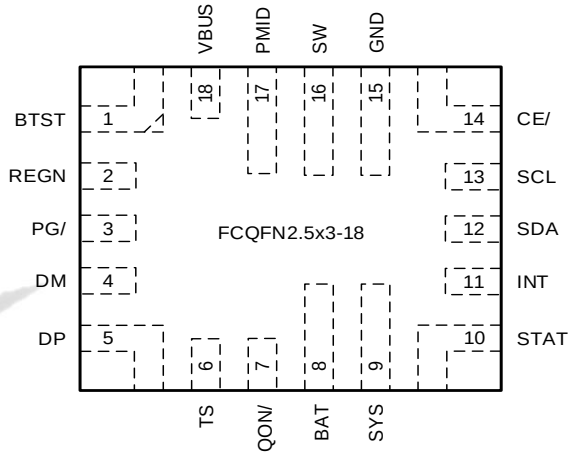


Figure 0-1. QFN2.5x3-18 Pin Configuration

Name	No.	IO	Description
BTST	1	P	High-side driver positive supply connects a 47nF capacitor between BTST and SW.
REGN	2	P	Internal LDO output. Connect a 4.7uF capacitor from REGN to GND.
PG/	3	DO	Open Drain Active Low Power Good Indicator – Connect to the pull up rail via 10-kΩ resistor. LOW indicates an input source of $V_{VBUS_PRESENT}$ < VBUS < V_{BUSOV}. Failing poor source detection or triggering the sleep comparator (VBUS < VBAT + V_{SLEEP}) also causes PG/ to transition HIGH.
DM	4	AIO	Negative line of the USB data line pair. Used for BC1.2 detection.
DP	5	AIO	Positive line of the USB data line pair. Used for BC1.2 detection.
TS	6	AI	Temperature qualification voltage input. Program temperature window with a resistor divider from REGN to TS to GND.
QON/	7	DI	BATFET enables / resets control input. Ship mode will be exited at a logic low pulse with a duration of t_{SHIP_MODE}. SYS (full system reset) will be reset at a logic low pulse with a duration of t_{QON_RST}.
BAT	8	P	Battery positive terminal pin uses a 10uF capacitor between BAT and GND.
SYS	9	P	Converter output pin connects two 10uF capacitors between SYS and GND.
STAT	10	DO	Open-drain output indicates charger status. Low: Charge in progress. HiZ: Charge complete or charger in SLEEP mode. Blink at 1Hz: Charge suspend (fault).
INT/	11	DO	Open-drain output. The INT/ pin sends an active low, 256-uS pulse to reports charger status update or fault.
SDA	12	DIO	I2C interface data.
SCL	13	DI	I2C interface clock.
CE/	14	DI	Charge enable pin. Enable charging when this pin is driven low & CHG_EN bit is set to 1.CE/ pin can be floating because it has an integrated about 4.8M pull down resistor.
PGND	15	P	Power ground.
SW	16	P	Switching node connects to output inductor.
PMID	17	P	The drain of the RBFET and the drain of HSFET.
VBUS	18	P	Charger input. Place at least 1uF capacitor from VBUS to GND.

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Specifications

Absolute Maximum Ratings (1)

	Min	Max	Unit
VBUS voltage	-2	30	V
PMID voltage	-0.3	30	V
BTST to SW voltage	-0.3	7	V
SW voltage	-0.3	22	V
Other pin voltage	-0.3	7	V
Storage temperature	-65	150	℃
Junction temperature	-40	150	℃

Recommended Operating Conditions (2)

Recommended Operating Conditions					
Parameter	**Description**	**Min**	**Nom**	**Max**	**Unit**
VBUS	Input voltage	4.0		13.5	V
VBAT	Battery voltage			4.65	V
IBUS	Input current			3.2	A
IBAT	Fast charging current			3.03	A
IBAT	RMS discharge current			9	A
TA	Ambient temperature	-40		85	°C
L	Inductor value	0.68	1	2.5	uH
CVBUS	VBUS capacitance(without de-rating)	1			uF
CPMID	PMID capacitance(without de-rating)	10			uF
CSYS	SYS capacitance(without de-rating)	10		500	uF
CBAT	BAT capacitance(without de-rating)	10			uF
CREGN	REGN capacitance(without de-rating)	4.7			uF

Note:

(1)Stress beyond absolute maximum rating may cause permanent damage to device.

(2)The device is not guaranteed to function outside of its operating conditions.

ESD Ratings

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), Mil-Std-883H Method 3015.8, all pins	±2000	V
		Charged device model (CDM), JS-002-2018, all pins	±500	V

Thermal Information

Thermal Metric		GLF70106	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	℃/W

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Electrical Characteristics

V_{BUS}=4.0 to 13.5V, V_{BAT}=3.8V, T_J=25℃, L=1μH for typical values (unless otherwise noted)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENT						
I_{Q_BAT}	Standby quiescent current	V_{BAT} = 3.7V, BATFET enabled, VBUS floating	2.0	2.5	6	μA
I_{SHIP_BAT}	Ship mode quiescent current	V_{BAT} = 3.7V, BATFET and I2C disabled	0.25	0.35	1	μA
I_{ADC_BAT}	ADC current in standby mode	V_{BAT} = 3.7V, BATFET and ADC enable		580	800	μA
I_{BYPASS}	Bypass mode quiescent current	V_{BAT} = 3.7V, EN_OTG_BYPASS		480	650	uA
I_{BUS}	Input current in buck mode	V_{BUS} = 5V, charge disabled, I_{SYS} = 0A	1.0	1.5	2.5	mA
I_{HIZ_VBUS}	Quiescent input current in HIZ mode	V_{BUS} = 5V, HIZ mode	25	33	50	μA
	Quiescent input current in HIZ mode	V_{BUS} = 12V, HIZ mode	200	215	350	μA
I_{BST}	Quiescent current in boost mode	V_{BAT}=4V, V_{BUS}=5V, boost mode enabled, not include NTC	1.0	1.2	2.5	mA
VBUS / VBAT SUPPLY						
V_{BUS_OP}	VBUS operating range		4.0		13.5	V
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery,			3.3	3.7	V
V_{VBUS_UVLO}	VBUS falling to turnoff I2C, no battery			3	3.3	V
$V_{VBUS_PRESENT}$	VBUS to enable REGN,VBUS rising			4.0	4.15	V
	Hys			150		mV
V_{SLEEP}	Enter Sleep mode threshold	VBUS falling, VBUS - VBAT, VBAT =4V	15	90	110	mV
V_{SLEEPZ}	Exit Sleep mode threshold	VBUS rising, VBUS - VBAT, VBAT =4V	115	220	340	mV
V_{BUSOV}	VBUS over voltage rising threshold to turn off switching	VBUS rising, OVP[1:0]=11	5.8	6.0	6.2	V
		VBUS rising, OVP[1:0]=10	6.1	6.4	6.75	V
		VBUS rising, OVP[1:0]=01	10.45	11	11.55	V
		VBUS rising, OVP[1:0]=00(default)	13.5	14.2	14.85	V
	VBUS over voltage falling threshold to resume switching	VBUS falling, OVP[1:0]=11	5.2	5.6	5.8	V
		VBUS falling, OVP[1:0]=10	5.8	6.2	6.45	V
		VBUS falling, OVP[1:0]=01	10	10.7	11.1	V
		VBUS falling, OVP[1:0]=00	13	13.9	14.5	V

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Electrical Characteristics(continued)

VBUS=4.0 to 13.5V, VBAT=3.8V, TJ=25℃, L=1μH for typical values (unless otherwise noted)

V_{BAT_UVLOZ}	BAT voltage for active I2C and turn on BATFET, no VBUS VBAT falling threshold		2.0	2.1	2.2	V
V_{BAT_UVLOZ}	BAT voltage for active I2C and turn on BATFET, no VBUS VBAT rising threshold		2.2	2.3	2.4	V
POWER-PATH MANAGEMENT						
$V_{SYS_MIN_ACC}$	Typical minimum system regulation voltage	VBAT=3.2V < VSYS_MIN = 3.5V, ISYS= 0A	3.5	3.75		V
V_{SYS_OVP}	System over voltage threshold	VREG = 4.35V, Charge disabled, ISYS=0A		4.7		V
		BATFET is in LDO mode, VSYS_MIN = 3.5V		4		V
R_{ON_RBFET}	T_J=25℃	PIN to PIN		30		mΩ
R_{ON_HSFET}	T_J=25℃	PIN to PIN		49		mΩ
R_{ON_LSFET}	T_J=25℃	PIN to PIN		41		mΩ
R_{ON_BATFET}	T_J=25℃	PIN to PIN		26		mΩ
V_{BATFET_FWD}	BATFET forward voltage in supplement mode	BAT discharge current 1A,		30		mV
$I_{SYS_OCP_Q4}$	BATFET over current	BATFET_OCP =0(Default)	8			A
		BATFET_OCP =1	12			A
BATTERY CHARGER						
$V_{BAT_REG_RANGE}$	Typical charge voltage regulation range		3.5		4.65	V
$V_{BAT_REG_STEP}$	Typical charge voltage step	4.3V < VBAT_REG < 4.52V		10		mV
$V_{BAT_REG_ACC}$	Charge voltage accuracy	VBAT_REG = 3.5V~4.65V, TJ = 25°C	-0.3		0.3	%
$V_{BAT_REG_ACC}$	Charge voltage accuracy	VBAT_REG = 3.5V~4.65V, TJ = -10°C ~ 85°C	-0.4		0.4	%
I_{CHG_RANGE}	Typical charge current regulation range	ICHG_SCALE=0(default)	20		2020	mA
		ICHG_SCALE=1	30		3030	mA
I_{CHG_STEP}	Typical charge current regulation step	ICHG_SCALE=0: 20mA to 1300mA		20		mA
		ICHG_SCALE=0: 1300mA to 2020mA		60		mA
		ICHG_SCALE=1: 30mA to 1950mA		30		mA
		ICHG_SCALE=1: 1950mA to 3030mA		90		mA

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Electrical Characteristics(continued)

VBUS=4.0 to 13.5V, VBAT=3.8V, TJ=25℃, L=1μH for typical values (unless otherwise noted)

I_{CHG_ACC}	Fast charge current regulation accuracy	ICHG = 30mA, VBAT = 3.1V or 3.8V,TJ = 0°C - 85°C	20	30	40	mA
		ICHG = 0.24A, VBAT = 3.1V or 3.8V,TJ = 0°C - 85°C	0.216	0.24	0.264	A
		ICHG = 0.72A, VBAT = 3.1V or 3.8V,TJ = 0°C - 85°C	0.682	0.72	0.76	A
		ICHG = 1.38A, VBAT = 3.1V or 3.8V,TJ = 0°C - 85°C	1.292	1.36	1.428	A
I_{PRECHG_RANGE}	Typical pre-charge current range	ICHG_SCALE=0	10		240	mA
		ICHG_SCALE=1	15		300	mA
I_{PRECHG_STEP}	Typical pre-charge current step	CHG_SCALE=0		20		mA
		ICHG_SCALE=1		30		mA
I_{PRECHG_ACC}	Precharge current accuracy	VBAT = 2.6V, IPRECHG = 10mA	5	10	15	mA
		VBAT = 2.6V, IPRECHG = 20mA	16	20	24	mA
		VBAT = 2.6V, IPRECHG = 120mA	108	120	132	mA
		VBAT = 2.6V, IPRECHG = 240mA	216	240	264	mA
I_{TERM_RANGE}	Typical termination current range	ICHG_SCALE=0	10		240	mA
		ICHG_SCALE=1	15		360	mA
I_{TERM_STEP}	Typical termination current Step	ICHG_SCALE=0		20		mA
		ICHG_SCALE=1		30		mA
I_{TERM_ACC}	Termination current accuracy	ITERM=10mA, TJ = 0°C - 85°C	5	10	15	mA
		ITERM=20mA, TJ = 0°C - 85°C	16	20	24	mA
		ITERM=40mA, TJ = 0°C - 85°C	32	40	48	mA
		ITERM=60~80mA , TJ = 0°C - 85°C	-10		10	%
		ITERM=100~140mA , TJ = 0°C - 85°C	-10		10	%
		ITERM=140~240mA, TJ = 0°C - 85°C	-5		5	%
V_{PRE_CHG}	Pre charge to fast charge threshold	VBAT rising(default)	2.9	3.0	3.1	V
		VBAT rising, 3.1V set	3.0	3.1	3.2	V
V_{BAT_SHORTZ}	Battery short voltage threshold	VBAT rising	2.0	2.15	2.3	V
V_{BAT_SHORT}		VBAT falling	1.8	2.0	2.2	V
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < VBAT_SHORTZ	20	25	30	mA
		VBAT < VBAT_SHORTZ	1	5	10	mA
V_{RECHG}	Battery recharge threshold	VRECHG=0, VBAT falling (default)	120	150	170	mV
		VRECHG=1, VBAT falling	216	240	275	mV
I_{SYS_LOAD}	VSYS PIN discharge load current VSYS=4.0V			250		Ω
I_{BAT_LOAD}	VBAT PIN discharge load VBAT=4.0V			250		Ω

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Electrical Characteristics(continued)

VBUS=4.0 to 13.5V, VBAT=3.8V, TJ=25℃, L=1μH for typical values (unless otherwise noted)

I_{PMID_LOAD}	PMID PIN discharge load PMID=5.0V			600		Ω
R_{CE}	CE/ PIN Pull Down Resistor			4.8		MΩ
BATTERY OVER-VOLTAGE PROTECTION						
V_{BAT_OVP}	VBAT rising threshold, As percentage of VBAT_REG		103	104	105	%
	VBAT falling threshold, As percentage of VBAT_REG		101	102	103	%
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		3.9		5.4	V
V_{INDPM_STEP}	Typical input voltage regulation step			100		mV
V_{INDPM_ACC}	VINDPM regulation accuracy		4.365	4.5	4.635	V
V_{INDPM_TRACK}	VINDPM threshold to track VBAT	VBAT = 4.35V, VINDPM_BAT_TRACK = VBAT+200mV	4.45	4.55	4.74	V
I_{INDPM_RANGE}	IINDPM regulation range		0.1		3.2	A
I_{INDPM_STEP}	IINDPM regulation step			100		mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500mA (TJ=0°C - 85°C)	450	465	500	mA
		IINDPM = 900mA (TJ=0°C - 85°C)	750	835	900	mA
		IINDPM = 1500mA (TJ=0°C - 85°C)	1300	1390	1500	mA
DP/DM DETECTION						
V_{DP/DM_2P8}	DP/DM comparator threshold for non-standard adapter		2.4	2.8	3.5	V
V_{DP/DM_2P0}	DP/DM comparator threshold for non-standard adapter		1.6	2.0	2.4	V
V_{DP/DM_1P2}	DP/DM comparator threshold for non-standard adapter		0.8	1.2	1.6	V
THERMAL REGULATION AND THERMAL SHUTDOWN						
THERMAL_REG	Thermal regulation accuracy	THERMAL_REG = 0, 90°C		101	110	°C
		THERMAL_REG = 1, 110°C		115	125	°C
T_{SHUT}	Thermal Shutdown Rising threshold			150		°C
	Thermal Shutdown Falling threshold			115		°C
THERMISTOR COMPARATOR (CHARGE MODE)						
Vcold	TS cold threshold	Percentage to REGN (0°C w/103AT) Rising Below 0°C	72.97	73.37	73.77	%
		Percentage to REGN (0°C w/103AT) Falling	71.49	71.89	72.29	%
		Percentage to REGN (-5°C w/103AT) Rising	75	75.4	75.8	%
		Percentage to REGN (-5°C w/103AT) Falling	74	74.4	74.8	%

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Electrical Characteristics(continued)

VBUS=4.0 to 13.5V, VBAT=3.8V, TJ=25℃, L=1μH for typical values (unless otherwise noted)

Vcool	TS cool threshold	Percentage to REGN (5°C w/103AT) Rising	70.35	70.75	71.15	%
		Percentage to REGN (5°C w/103AT) Falling	68.8	69.2	69.6	%
		Percentage to REGN (10°C w/103AT) Rising	67.85	68.25	68.65	%
		Percentage to REGN (10°C w/103AT) Falling	66.55	66.95	67.35	%
		Percentage to REGN (15°C w/103AT) Rising	64.85	65.25	65.65	%
		Percentage to REGN (15°C w/103AT) Falling	63.8	64.2	64.6	%
		Percentage to REGN (20°C w/103AT) Rising	61.85	62.25	62.65	%
		Percentage to REGN (20°C w/103AT) Falling	60.8	61.2	61.6	%
Vwarm	TS warm threshold	Percentage to REGN (40°C w/103AT) Rising, Above 40°C	47.85	48.25	48.65	%
		Percentage to REGN (40°C w/103AT) Falling	48.9	49.3	49.7	%
		Percentage to REGN (45°C w/103AT) Rising. Above 45°C	44.35	44.75	45.15	%
		Percentage to REGN (45°C w/103AT) Falling	45.4	45.8	46.2	%
		Percentage to REGN (50°C w/103AT) Rising. Above 50°C	40.3	40.7	41.1	%
		Percentage to REGN (50°C w/103AT) Falling	41.4	41.8	42.2	%
		Percentage to REGN (55°C w/103AT) Rising. Above 55°C	37.3	37.7	38.1	%
		Percentage to REGN (55°C w/103AT) Falling	38.6	39	39.4	%
Vhot	TS hot threshold	Percentage to REGN (50°C w/103AT) Rising. Above 50°C	40.3	40.7	41.1	%
		Percentage to REGN (50°C w/103AT) Falling	41.4	41.8	42.2	%

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Electrical Characteristics(continued)

VBUS=4.0 to 13.5V, VBAT=3.8V, TJ=25℃, L=1μH for typical values (unless otherwise noted)

		Percentage to REGN (60°C w/103AT) Rising. Above 60°C	33.8	34.2	34.6	%
		Percentage to REGN (60°C w/103AT) Falling	35.1	35.5	35.9	%
THERMISTOR COMPARATOR (BOOST MODE)						
Vbst_cold	TS pin voltage cold threshold in boost mode	As Percentage to REGN (–20°C w/103AT) Rising Below –20°C	79.6	80	80.4	%
		As Percentage to REGN (–20°C w/103AT) Falling	78.3	78.7	79.1	%
		As Percentage to REGN (–10°C w/103AT) Rising. Below –10°C	76.7	77.1	77.5	%
		As Percentage to REGN (–10°C w/103AT) Falling	75	75.4	75.8	%
Vbst_hot	TS pin voltage hot threshold in boost mode	As Percentage to REGN, (65°C w/103AT) Rising. Above 65°C	30.8	31.2	31.6	%
		As Percentage to REGN, (65°C w/103AT) Falling	32.1	32.5	32.9	%
		As Percentage to REGN, (60°C w/103AT) Rising. Above 60°C	33.6	34	34.4	%
		As Percentage to REGN, (60°C w/103AT) Falling	35.1	35.5	35.9	%
		Percentage to REGN (55°C w/103AT) Rising. Above 55°C	37.3	37.7	38.1	%
		Percentage to REGN (55°C w/103AT) Falling	38.6	39	39.4	%
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency		1.32	1.5	1.68	MHz
D_{MAX}	Maximum PWM Duty Cycle			97		%
I_{HSFET_OCP}	Cycle-by-cycle peak current threshold		4.5	5.0		A
BOOST MODE CONVERTER						
V_{BST_BAT}	Battery voltage exiting boost mode		2.7	2.8	2.9	V
V_{BST_RANGE}	Boost vout range		4.6		9.52	V
V_{BST_ACC}	Boost mode voltage regulation accuracy IVBUS = 0~1.2A, BOOST_V = 5.15V,		5	5.15	5.3	V
I_{BST_RANGE}	Typical boost mode current regulation		0.5		2.4	A
$I_{BST_OCP_Q1}$	Boost mode RBFET current limit	BOOST_LIM = 0.5 A	0.5	0.65	0.75	A
		BOOST_LIM = 1.2 A	1.2	1.6	1.8	A
$I_{BST_LSFET_OCP}$	Cycle-by-cycle peak current threshold		4.5	4.8		A

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Electrical Characteristics(continued)

VBUS=4.0 to 13.5V, VBAT=3.8V, TJ=25℃, L=1μH for typical values (unless otherwise noted)

V_{BST_OVP}	Boost mode over voltage threshold on PMID			11		%
I_{BYPASS_RCP}	Bypass Mode reverse current (from PMID to BAT) threshold			500		mA
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, IREGN = 10mA	4.58	4.7	4.8	V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5V, VREGN = 3.8V	17			mA
ADC MEASUREMENT RANGE AND LSB						
IBUS_ADC	ADC Bus Current Reading (both forward and OTG)	Range	-2.4		3.2	A
		LSB		2		mA
VBUS_ADC	ADC VBUS Voltage Reading	Range	0		15	V
		LSB		5		mV
VPMID_ADC	ADC PMID Voltage Reading	Range	0		15	V
		LSB		5		mV
VBAT_ADC	ADC BAT Voltage Reading	Range	0		6	V
		LSB		2		mV
VSYS_ADC	ADC SYS Voltage Reading	Range	0		6	V
		LSB		2		mV
IBAT_ADC	ADC BAT Current Reading	Range	-5		4	A
		LSB		4		mA
TS_ADC	ADC TS Voltage Reading	Range as a percent of REGN (–40℃ to 85℃ for 103AT)	0		90	%
		LSB		0.0961		%
TDIE_ADC	ADC Die Temperature Reading	Range	-40		150	℃
		LSB		0.5		℃
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL	Pull up rail 1.2V	1.0			V
V_{IL}	Input low threshold level	Pull up rail 1.2V			0.4	V
V_{OL}	Output low threshold level	Sink current = 5mA			0.4	V
Timing Requirements						
VBUS / VBAT POWER UP						
t_{VBUS_OV}	VBUS OVP Reaction-time			130		ns
BATTERY CHARGER						
t_{TERM_DGL}	Deglitch time for charge termination			30		ms
t_{RECHG_DGL}	Deglitch time for recharge threshold			30		ms

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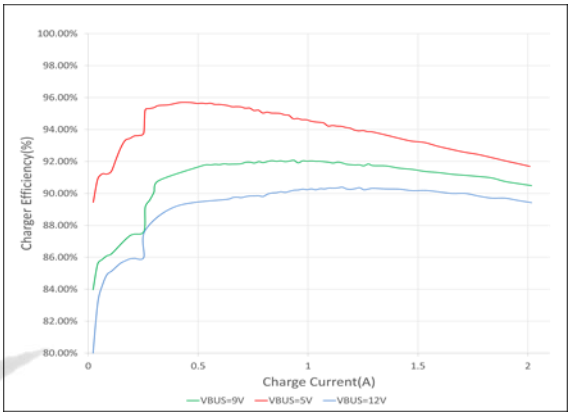
Electrical Characteristics(continued)

VBUS=4.0 to 13.5V, VBAT=3.8V, TJ=25℃, L=1μH for typical values (unless otherwise noted)

t_{SAFETY}	Charge safety timer accuracy, CHG_TIMER = 20hr		17	20	24	hr
t_{SAFETY}	Charge safety timer accuracy, CHG_TIMER = 10hr		8	10	12	hr
QON/ Timing						
t_{SHIP_MODE}	QON low time to turn on BATFET and exit shipmode	default	0.9	1.1	1.3	s
				35		ms
t_{QON_RST}	QON low time before BATFET full system reset		8	10	12	s
t_{BATFET_RST}	BATFET off time during full system reset		250		400	ms
t_{BATFET_DLY}	Delay time before BATFET turn off in ship mode			10	15	s

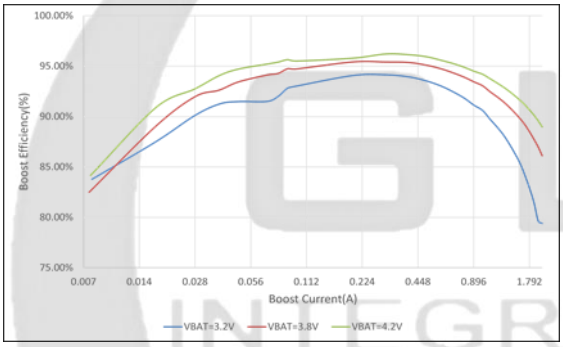
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Typical Characteristics



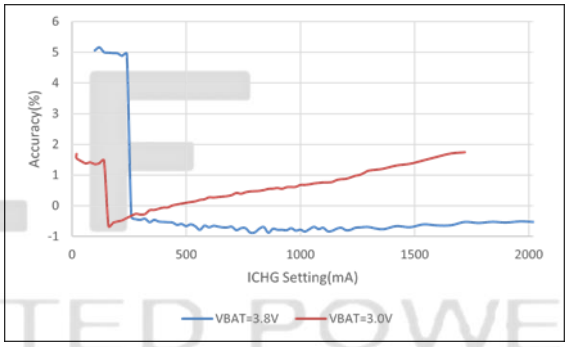
VBAT = 3.8V DCR = 14mΩ

Figure 0-1 Charge Efficiency vs. Charge Current



VOTG = 5.15V DCR = 14mΩ

Figure 0-2 Boost Mode Efficiency vs. Boost Output Current



VBUS = 5V

Figure 0-3 Charge Current Accuracy vs. ICHG Setting

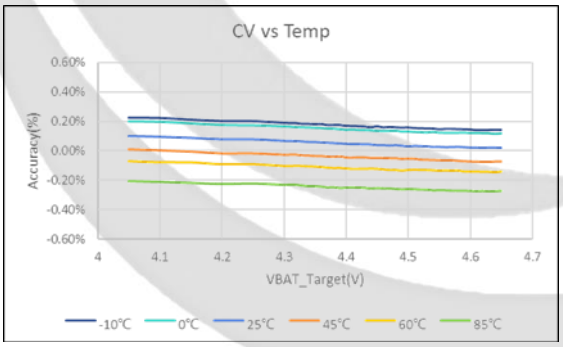


Figure 0-4 Charge Voltage Accuracy vs. VREG Setting

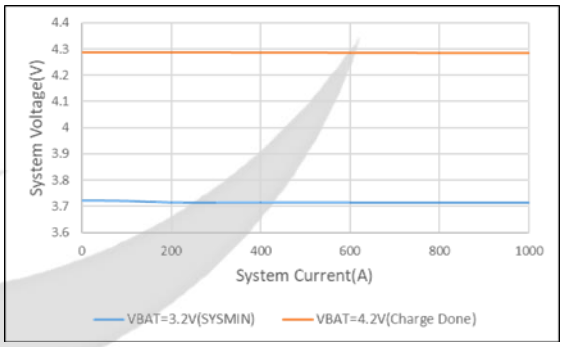


Figure 0-5 System Load Regulation for SYSMIN and Charge Done

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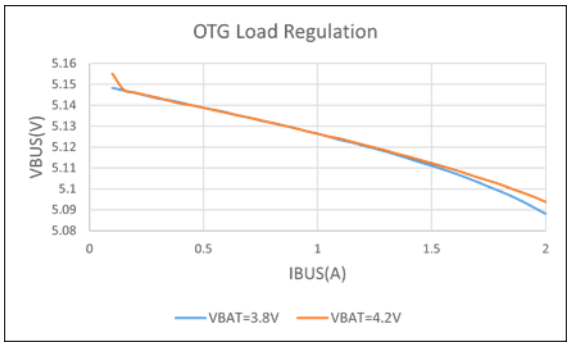


Figure 0-6 OTG Load Regulation

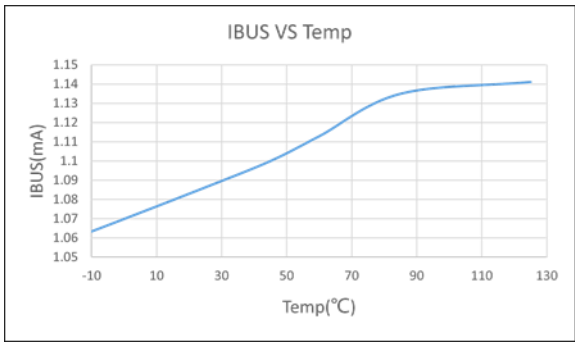


Figure 0-7 IBUS vs. Temp

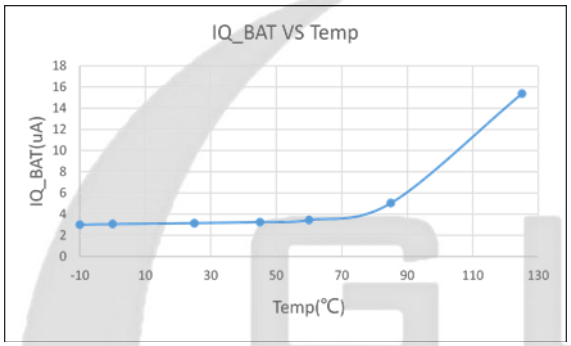


Figure 0-8 IQ_BAT vs. Temp

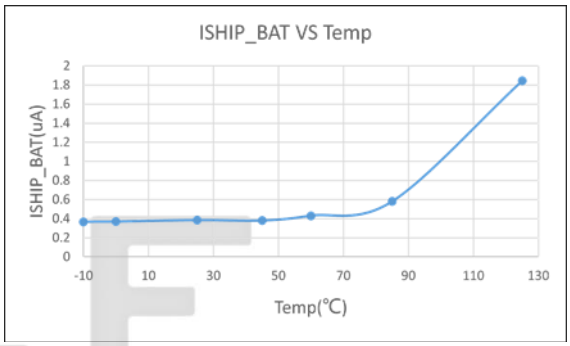
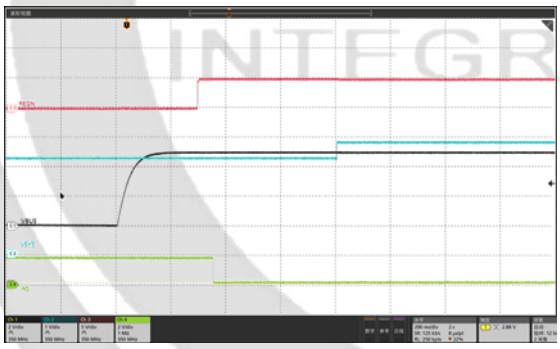
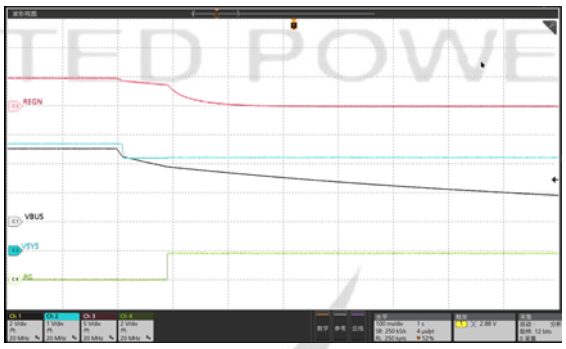


Figure 0-9 ISHIP_BAT vs. Temp



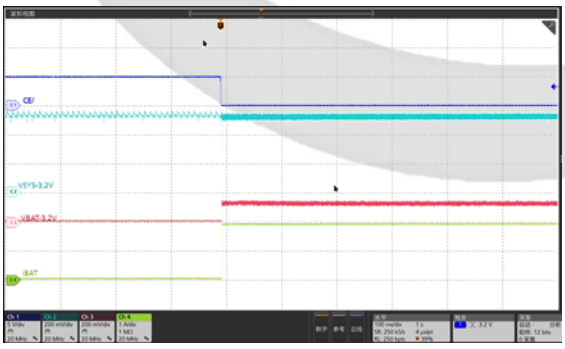
VBUS=5V V_{BAT}=3.2V I_{CHG}=1A

Figure 0-10 Power-Up with Charge Enable



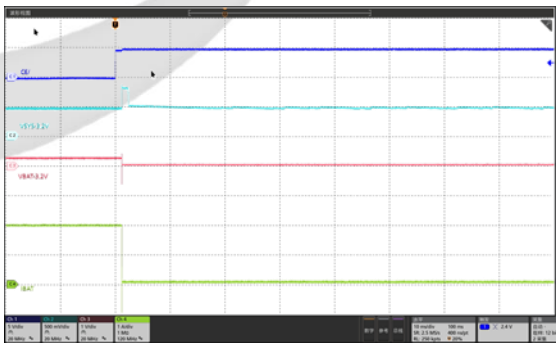
VBUS=5V V_{BAT}=3.2V I_{CHG}=1A

Figure 0-11 Power-Down



V_{BUS}=5V V_{BAT}=3.2V I_{BAT}=2A

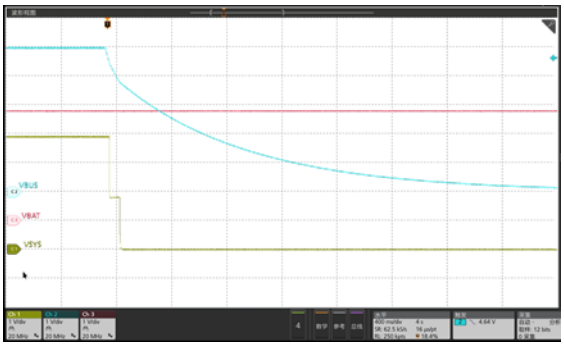
Figure 0-12 Charge Enable



V_{BUS}=5V V_{BAT}=3.2V I_{BAT}=2A

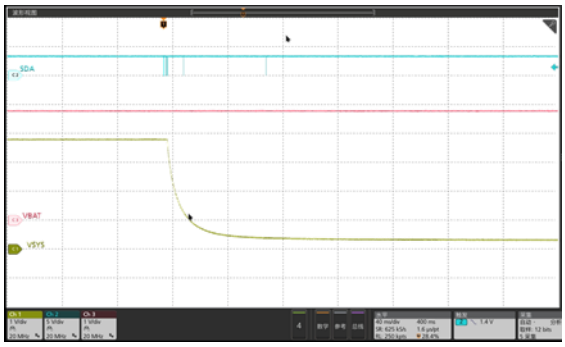
Figure 0-13 Charge Disable

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V_{BUS}=5V V_{BAT}=3.8V

Figure 0-14 BATFET_DIS=1 VBUS Plug Out Enter Ship Mode



V_{BAT}=3.8V

Figure 0-15 BATFET_DIS CMD Enter Ship Mode

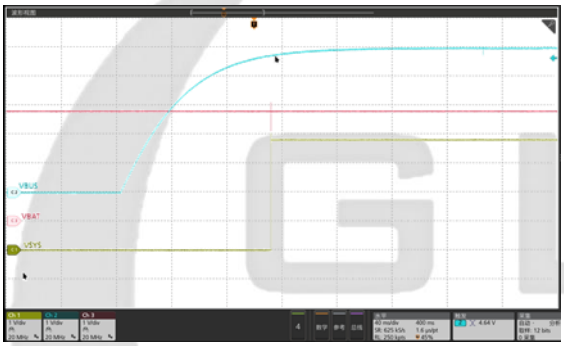


Figure 0-16 VBUS Plug In Exist From Ship Mode

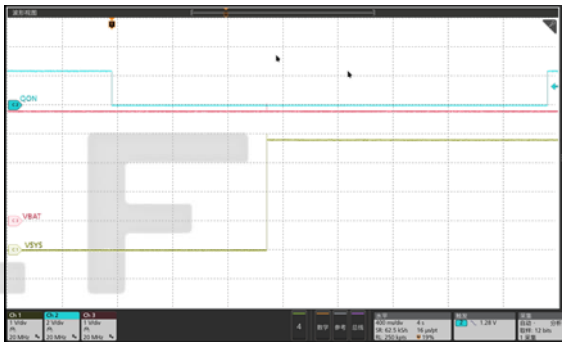
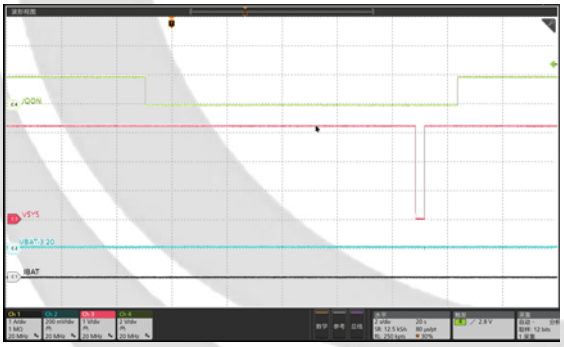
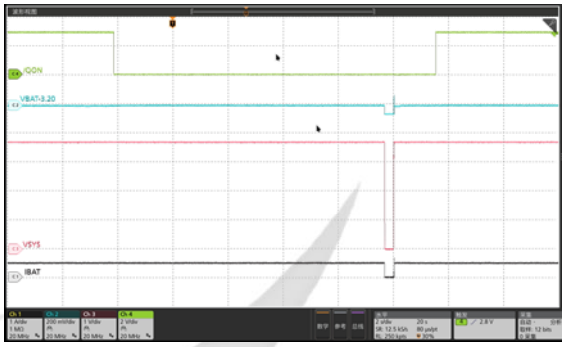


Figure 0-17 QON/ be low 1.1s Wake Up



VBUS=0V V_{BAT}=3.2V I_{BAT}=0mA

Figure 0-18 System Reset by QON/ without VBUS Present



VBUS=5V V_{BAT}=3.2V I_{BAT}=480mA

Figure 0-19 System Reset by QON/ with VBUS Present

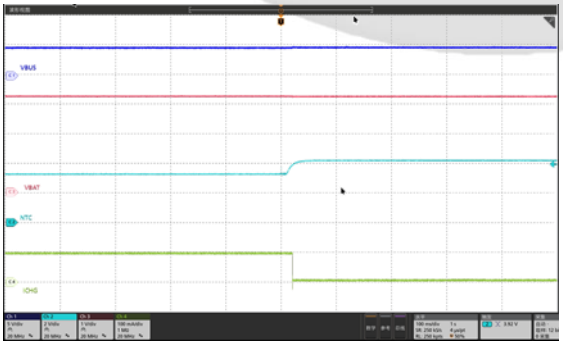


Figure 0-20 NTC COLD ENTRY

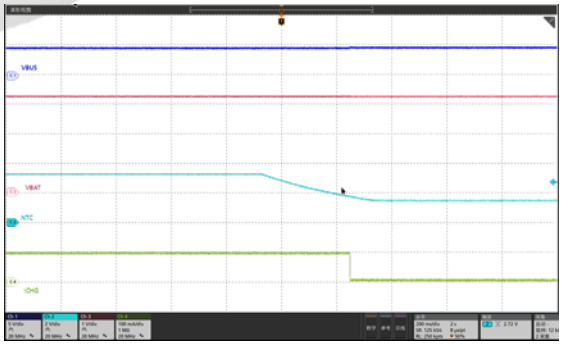
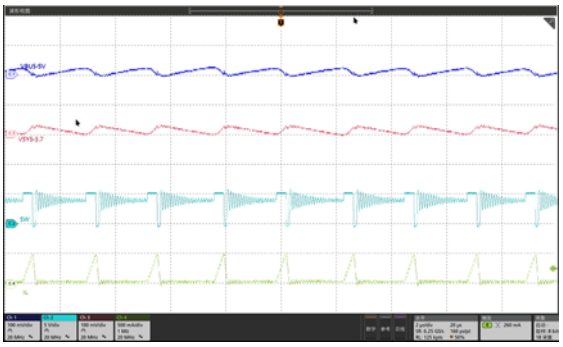


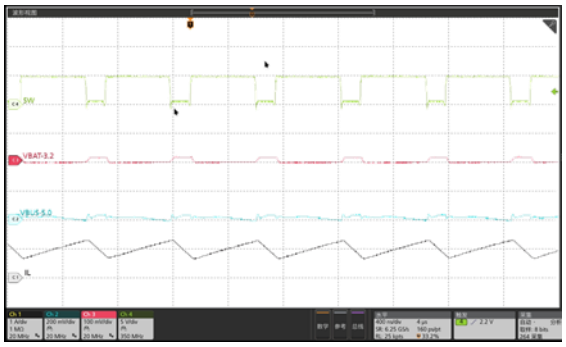
Figure 0-21 NTC HOT ENTRY

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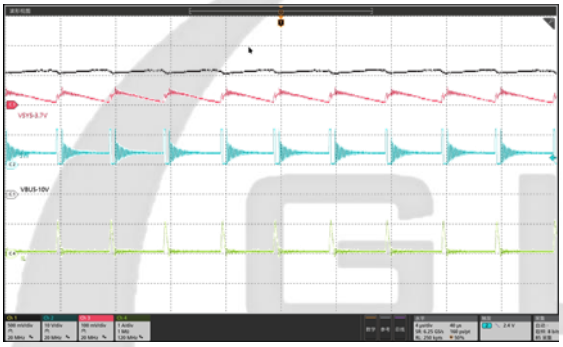
VBUS=5V V_{BAT}=3.2V I_{SYS}=50mA Charge Disable

Figure 0-22 PFM Switching in Buck Mode



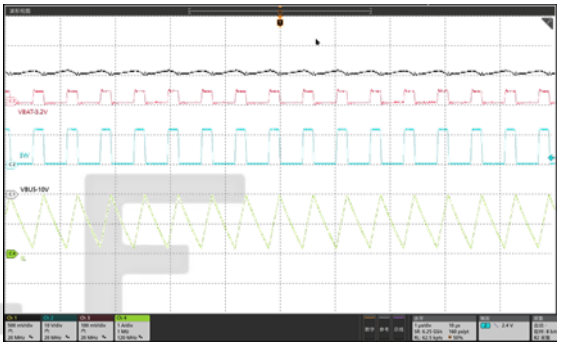
VBUS=5V V_{BAT}=3.2V I_{CHG}=1A

Figure 0-23 PWM Switching in Buck Mode



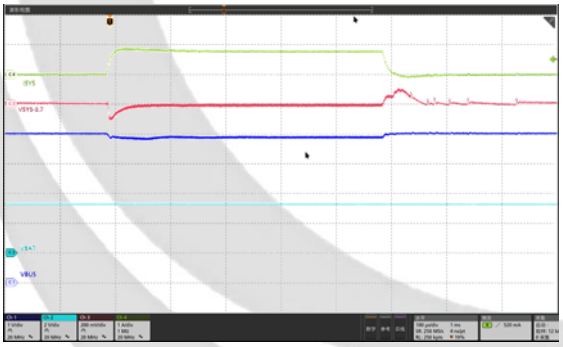
VBUS=12V V_{BAT}=3.2V I_{SYS}=50mA Charge Disable

Figure 0-24 PFM Switching in Buck Mode



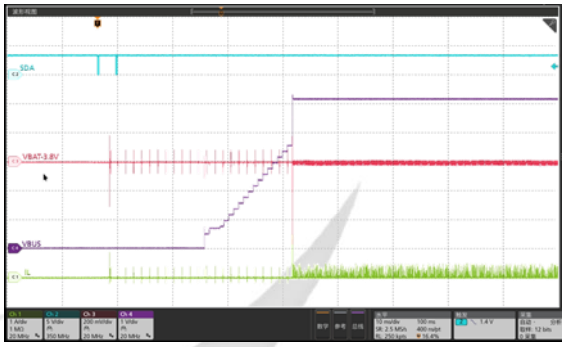
VBUS=12V V_{BAT}=3.2V I_{CHG}=1A

Figure 0-25 PWM Switching in Buck Mode



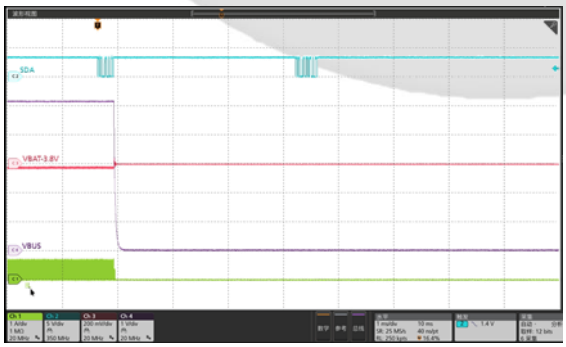
VBUS=5V V_{BAT}=3.2V I_{SYS} from 0A to 1A

Figure 0-26 System Load Transient



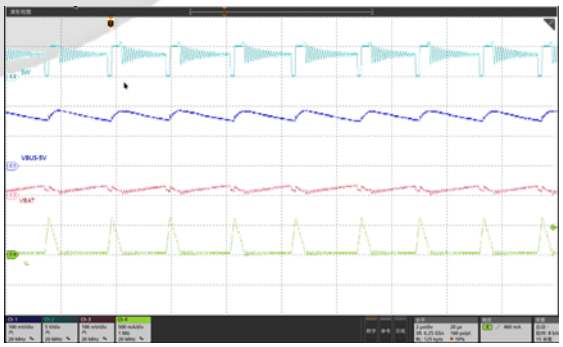
V_{BAT}=3.8V V_{BOOST}=5.15V

Figure 0-27 Boost Mode Power Up



V_{BAT}=3.8V V_{BOOST}=5.15V I_{BOOST}=200mA

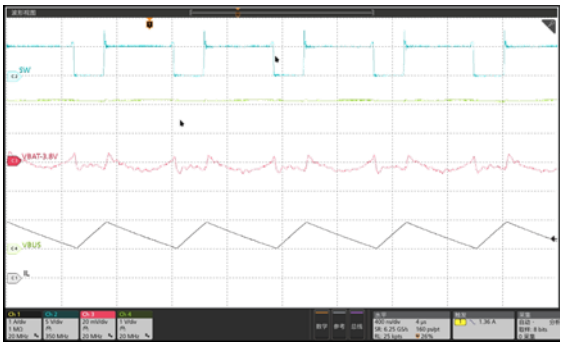
Figure 0-28 Boost Mode Power Down



V_{BAT}=3.8V V_{BOOST}=5.15V I_{BOOST}=50mA

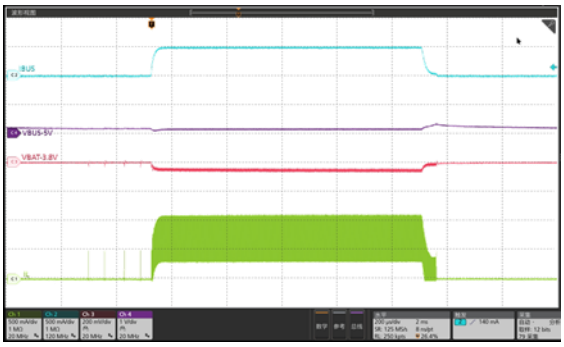
Figure 0-29 PFM Switching in Boost Mode

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V_{BAT}=3.8V V_{BOOST}=5.15V I_{BOOST}=1A

Figure 0-30 PWM Switching in Boost Mode



V_{BAT}=3.8V V_{BOOST}=5.15V I_{BOOST} from 0A to 0.5A

Figure 0-31 Boost Mode Load Transient

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Functional Description

Block Diagram

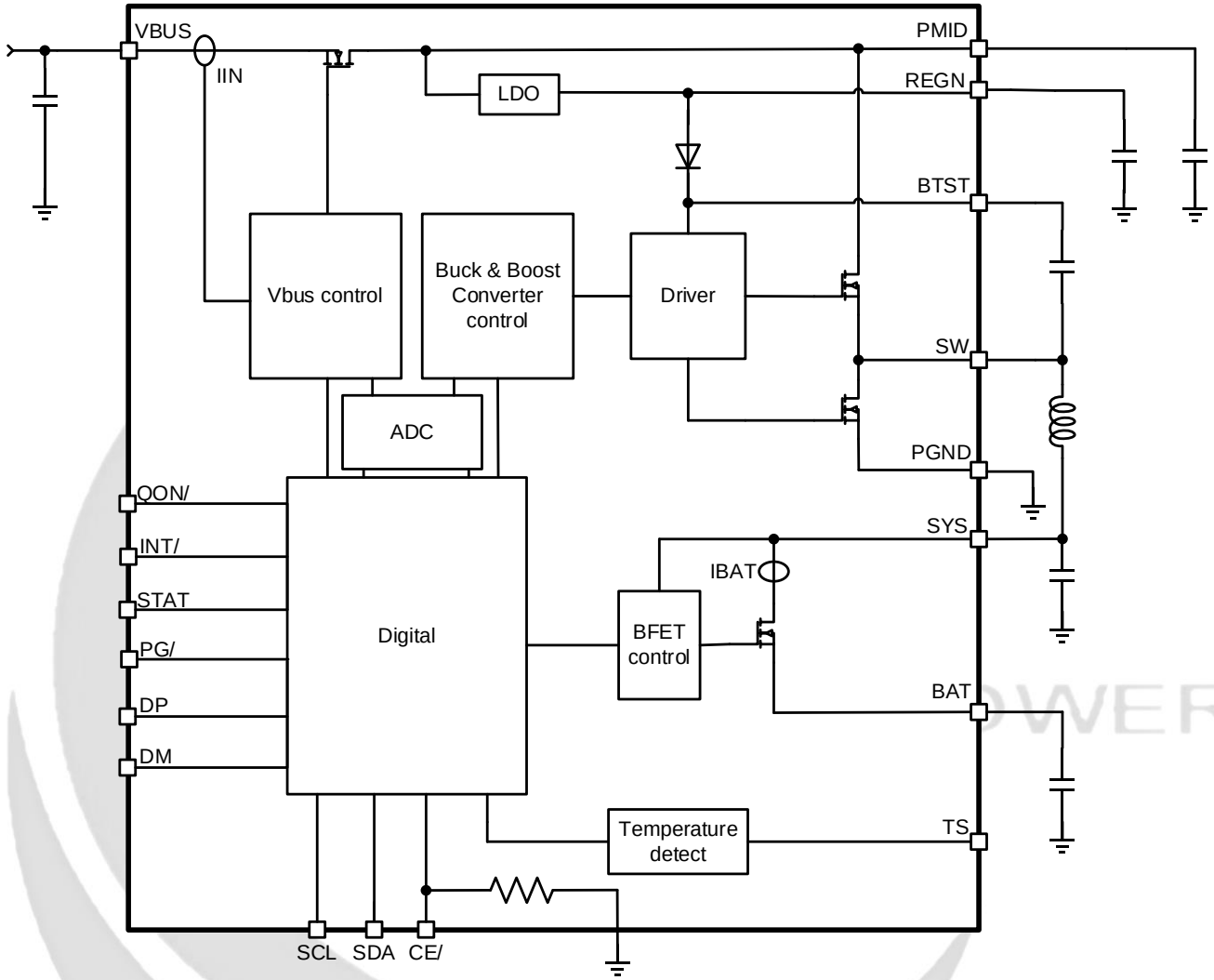


Figure 0-1 Block Diagram

Power-On-Reset

When VBUS or BAT rises above its UVLO level (VBUS > V_{VBUS_UVLOZ} or VBAT > V_{BAT_UVLOZ}), all registers are reset to their POR values and the I2C interface enables for communication. A non-maskable INT/ pulse is generated, and the host can access all of the registers.

Device Power Up from Battery

When the device is powered up from battery only, the BATFET turns on to the system if battery voltage is above UVLO threshold ($V_{BAT_UVLO_RISE}$). The REGN LDO output remains off to minimize the quiescent current. The discharge current through BATFET is continuously monitored. If the current is larger than $I_{SYS_OCP_Q4}$, the BATFET is turned off, BATFET_DIS is set to 1, and the device enters to ship mode.

Device Power Up from Input Source

When an input source is plugged in and VBUS voltage is above $V_{VBUS_PRESENT}$, the device will turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is

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started. and charge to the battery if the charge conditions are met. The buck converter start-up sequence is as listed:

1. VBUS ≥V_{BAT}+V_{SLEEPZ}, if input voltage is not high enough, the device will keep in standby mode and system is powered from battery.
2. Power up REGN LDO and turn on RBFET after about 220mS delay.
3. Poor source qualification.
4. Input source type detection is based on DP / DM to set default input current limit, refer to input source type detection section.
5. Input voltage limit threshold setting
6. Power up buck converter.

REGN LDO Power Up

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

1. VBUS above $V_{VBUS_PRESENT}$
2. VBUS above V_{BAT} + V_{SLEEPZ}
3. EN_HIZ = 0
4. Above conditions are satisfied during 220ms delay

If any one of the above conditions is not valid, the REGN LDO and the converter power stage remain off with the converter disabled. In this state, the battery supplies power to the system.

Poor Source Qualification

After the REGN LDO powers up, the device checks the current capability of the input source. The input source must meet both of the following requirements to start the buck converter:

1. VBUS voltage above $V_{VBUS_PRESENT}$.
2. VBUS voltage above $V_{VBUS_PRESENT}$ when sinking 20mA for 50ms.

Once the input source passes poor source detection, the status register bit VBUS_PG_STAT is set to 1 and the INT/ pin is pulsed to signal to the host. If the device fails the poor source detection, it will not repeat poor source qualification. It will re-start when VBUS is Above $V_{VBUS_PRESENT}$.

The buck converter will not start up if poor source detection is not passed. Also, when VBUS OVP happens, PMID will not sink 20mA for 50ms on VBUS.

Input Source Type Detection

After the REGN LDO is powered, the adapter has been qualified as a good source, Then the device runs input source detection through DP/DM lines to detect USB Battery Charging Specification 1.2(BC1.2) input source (SDP/CDP/DCP) and non-standard adapters.

The USB BC1.2 is able to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). The detection algorithm runs automatically each time that VBUS is plugged in, updating the IINDPM according to Table 7-1. When the Data Contact Detection (DCD) timer of 420ms is expired, the non-standard adapter detection is applied to set the input current limit.

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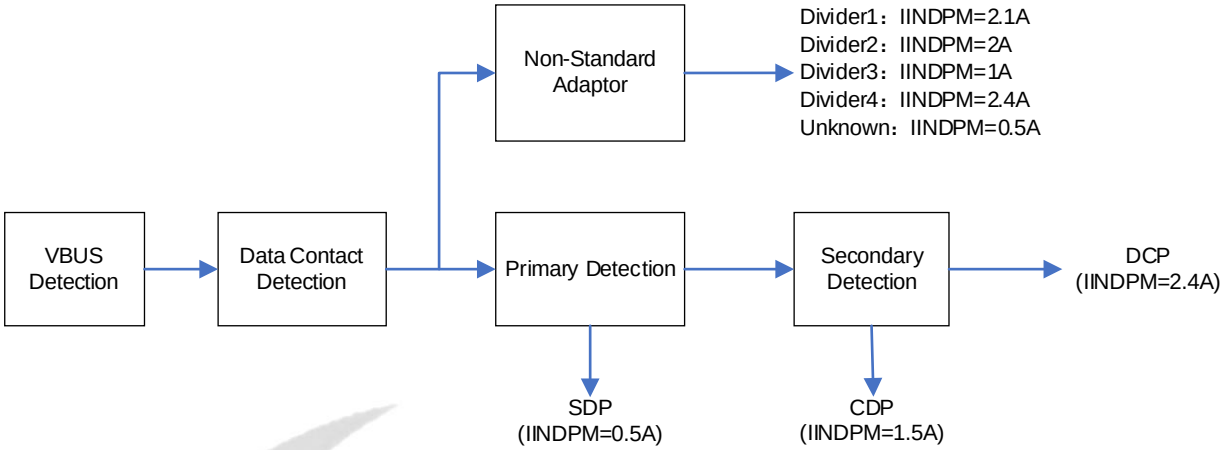


Figure 0-2 DP/DM Detection Flow

The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the DP/DM pins. Detection the voltage applied on each pin and determine the input current limit according to Table 7-2.

Table 0-1 Input Current Limit Setting from DP/DM Detection

DP/DM Detection	Input Current Limit
USB SDP	500mA
USB CDP	1.5A
USB DCP	2.4A

Table 0-2 Non-Standard Adapter Detection

Non-Standard Adapter	DP Threshold	DM Threshold	Input Current Limit
Divider 1	Within V_{DP/DM_2P8}	Within V_{DP/DM_2P0}	2.1A
Divider 2	Within V_{DP/DM_1P2}	Within V_{DP/DM_1P2}	2A
Divider 3	Within V_{DP/DM_2P0}	Within V_{DP/DM_2P8}	1A
Divider 4	Within V_{DP/DM_2P8}	Within V_{DP/DM_2P8}	2.4A
Unknown	Others		0.5A

Input Voltage Limit Threshold Setting

The GLF70106 support a wide range of input voltage limit. VINDPM default setting is 4.5V. The GLF70106 also support dynamic VINDPM tracking, which tracks the battery voltage to ensure a sufficient margin between input and battery voltages for proper operation of the buck converter. This function is enabled via the VINDPM_BAT_TRACK register bit. When programmed, the actual input voltage limit is the higher between the VINDPM register and VINDPM_BAT_TRACK.

Power Up Buck Converter

After the input current and voltage limits are set, the converter is enabled and the HSFET and LSFET start switching. The system voltage is powered from the converter instead of the battery. If battery charging is disabled, the BATFET turns off. Otherwise, the BATFET stays on to charge the battery.

When the SYS voltage is below V_{BAT_SHORT}, the input current is limited to the lower of 200mA or IINDPM register setting. Buck supports PFM mode by default while it works in PWM mode during fast charging when system voltage is higher than VSYS_MIN+200mV.

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Power Path Management

Narrow VDC architecture

The GLF70106 integrates Narrow VDC architecture (NVDC) power path management with BATFET separating system from battery. It turns off BATFET and the system is powered by input source (VBUS) only during charge termination.

The BATFET can operate in linear mode (LDO mode), so the system is regulated above the minimum system voltage (VSYS_MIN+200mV) even with a fully depleted battery. The minimum system voltage is set by VSYS_MIN register setting, default 3.5V. When charging is disabled or terminated, the system is regulated at VBAT+80mV if the battery voltage is above minimum system voltage (VSYS_MIN+200mV).

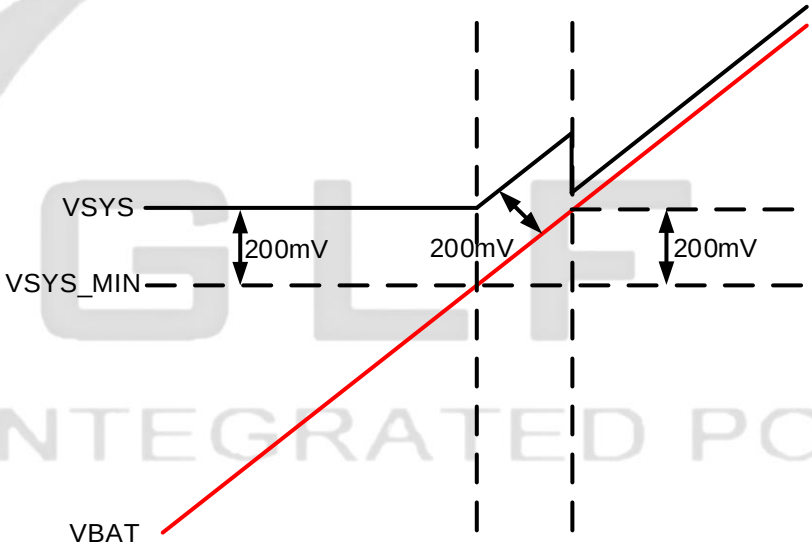


Figure 0-3 System Voltage vs Battery Voltage

Dynamic Power Management

To meet the USB maximum current limit and avoid overloading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. This power path management can reduce the charging current to avoid input source overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). When the charge current is reduced to zero, but the input source is still not enough to support system load, and the system voltage starts to drop, then the device will enter the supplement mode automatically, the BATFET turns on and the system is supplied from both battery and input source.

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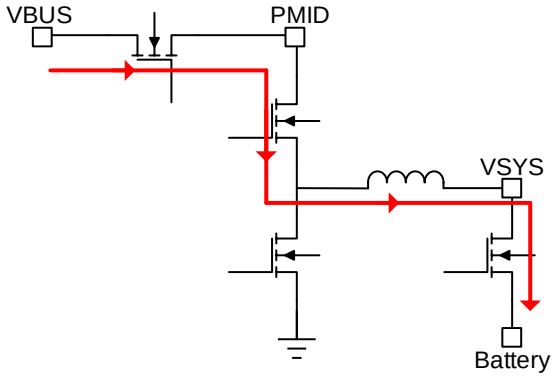


Figure 0-4 Charge Mode

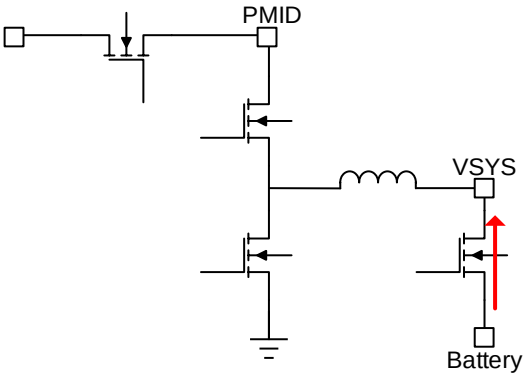


Figure 0-5 Discharge Mode

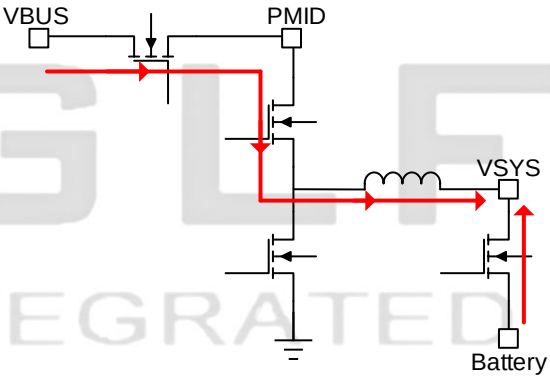


Figure 0-6 Supplement Mode

HI-Z Mode

The GLF70106 supports HIZ mode via setting EN_HIZ bit to 1. The system is powered from battery and the buck converter stops working even the VBUS is good. It will clear boost enable bit if the HIZ bit is set. In only battery mode, EN_HIZ bit will reset ADC_EN bit and disable ADC function. In charging mode, EN_HIZ bit won't reset ADC_EN bit. The device will exit HIZ mode by:

1. Clear the HIZ bit in register.
2. Adapter Plug-in.
3. Watchdog timeout.
4. REG_RST operation.

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Charge Mode

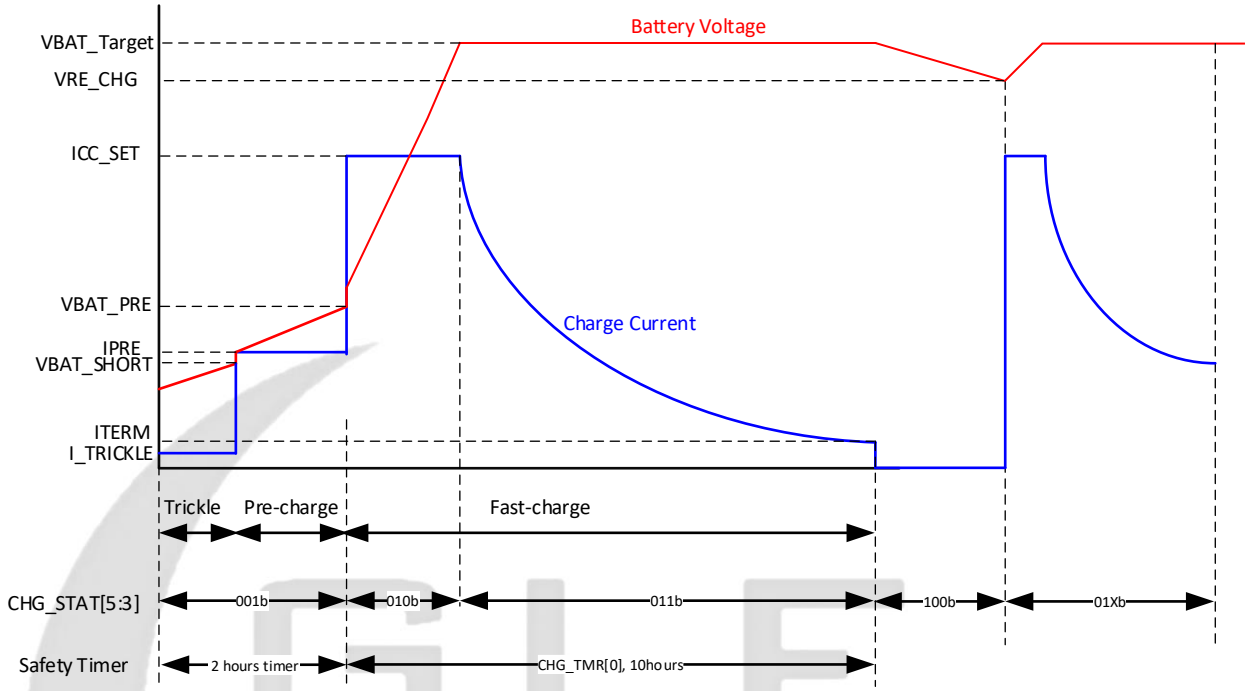


Figure 0-7. Battery charging profile

The GLF70106 charges the battery in five phases: trickle charge, pre-charge, constant current charge, constant voltage charge. The host can configure charge current and charge voltage by I2C interface, the device will check the battery voltage and regulates current and voltage accordingly.

Table 0-3 Charging Parameters

VBAT	Charging Current	Default Setting	Register	CHG_STAT
$<V_{BAT_SHORT}$	I_{BAT_SHORT}	25mA	REG14[6]	001
$>V_{BAT_SHORT}$ $<V_{BATPRE}$	I_{PRECHG}	10mA	REG10[3:0]	001
$>V_{BATPRE}$	I_{CHG}	100mA	REG02[6:0]	010

A charge cycle starts when the following conditions are valid:

1. BUCK converter starts.
2. Charging is enabled (CHG_EN bit=1 and CE/ is low).
3. No thermistor fault on TS. The battery is at normal temperature or at warm / cool temperature while JEITA charge current is not 0mA or TS_DIS=1.
4. No safety timer fault.
5. BATFET is not forced to turn off (BATFET_DIS=0).

The device terminates a charge cycle when the current is below termination current in constant voltage phases. In DPM or thermal regulation modes or EN_TERM bit is not set, termination is disabled.

The GLF70106 has a safety timer. The safety time is 2 hours/0.5 hour for pre-charge phase and 10 hours (20 hours optional) for fast charge phase. When the safety timer expires, charging suspends and STAT pin is blinking. During IINDPM / VINDPM / thermal regulation or JEITA cool / warm when fast charge current is reduced, the safety timer counts at half clock rate, this feature can be disabled by writing 0 to TMR2X_EN bit. The timer can be reset by following cases:

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1. Restarting the charging cycle (CHG_EN bit)
2. VBUS Plug-in Toggle
3. EN_HIZ Toggle
4. REG_RST operation

Thermal regulation is also integrated in the GLF70106. The device monitors the junction temperature to avoid overheating the chip. When the junction temperature exceeds thermal regulation limit (110℃ or 90℃), the device lowers down the charge current and THERM_STAT bit is set.

OTG Mode

The GLF70106 integrates boost converter to deliver power from the battery to other portable devi cesthrough VBUS pin. The output voltage is regulated at 4.6V/ 4.75V/5.0V/5.15V/5.3/5.45V/5.6V/6. 0V/6.48V/7.0V/7.52V/8.0V/8.48V/8.96V/9.52V (programmable) and output current is up to 0.5A/1.2A/ 1.5A/2.4A(programmable). Boost is enabled if the conditions below are valid:

1. EN_OTG_BST =1
2. Battery voltage is above V_{BST_BAT}. EN_OTG_BST bit is cleared if VBAT is below V_{BST_BAT}
3. VBUS is less than $V_{VBUS_PRESENT}$ or $V_{BAT}+V_{SLEEP}$
4. Temperature is within acceptable range ($V_{BHOT_RISE}<V_{TS}<V_{BCOLD_FALL}$) or TS_DIS=1

The boost supports PFM mode by default and host can disable PFM mode by PFM_DIS bit.

If RBFET_FORCE_ON bit=0, the device will not turn on RBFET in boost mode, and boost output on PMID pin.

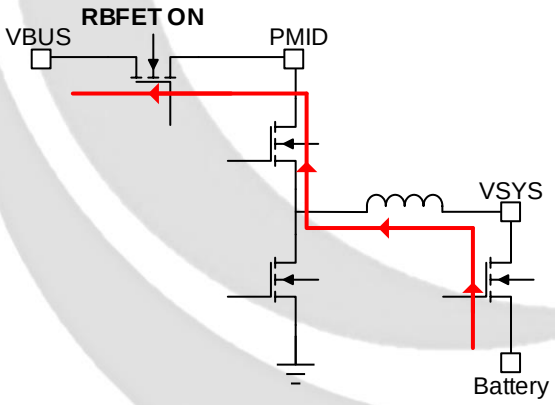


Figure 0-8 OTG Mode

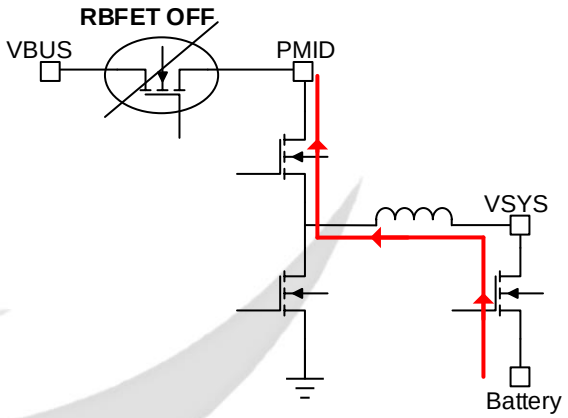


Figure 0-9 PMID Boost Mode

Bypass OTG Mode

GLF70106 reverse operation supports bypass mode, which connects battery directly to the PMID pin via BATFET and HSFET. During bypass mode, VBUS_STAT is not set to 111.The device will enter Bypass mode if the conditions below are valid:

1. RBFET_FORCE_ON = 0
2. EN_OTG_BYPASS = 1
3. VBAT > V_{BST_BAT}, EN_OTG_BYPASS bit is self-cleared if VBAT is below V_{BST_BAT}
4. VBUS is less than $V_{VBUS_PRESENT}$ or $V_{BAT}+V_{SLEEP}$

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The device will exit Bypass mode if any of the following conditions are valid:

1. EN_OTG_BYPASS = 0
2. Adapter Plug-in
3. RCP fault
4. T_{SHUT} happens
5. HIZ bit set

GLF70106 support bypass mode on PMID output only when EN_OTG_BYPASS bit is set. In this mode, High side mos will always on, and PMID=VBAT. Once bypass is set, RBFET_FORCE_ON bit can't be set to 1 again unless exit this mode.

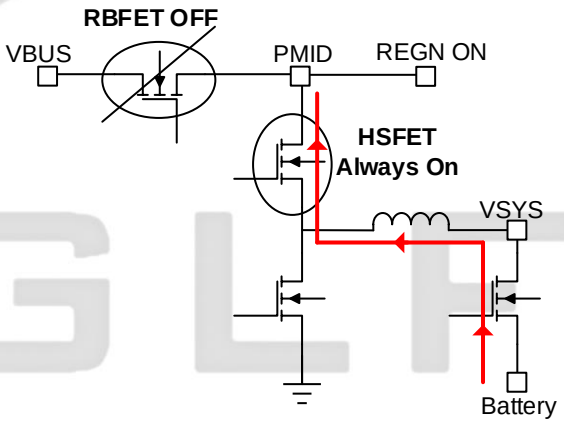


Figure 0-10 Bypass OTG Mode

Ship Mode, System Reset and QON/ Pin

When the host sets the BATFET_DIS bit, the charger can turn off the BATFET immediately or delay by t_{BATFET_DLY}. In the ship mode, the quiescent current is down to I_{SHIP_BAT}. I2C is not available in ship mode. The device will exit ship mode when one of the events below are valid:

1. Adapter Plug-in.
2. Set REG_RST bit to reset BATFET_DIS bit during delay time.
3. A logic high to low transition on QON/ pin with t_{SHIP_MODE} debounce time when QON_WK_EN is set to "1". Host can set debounce time (1.1s/35ms) by register QON_WK_Time.

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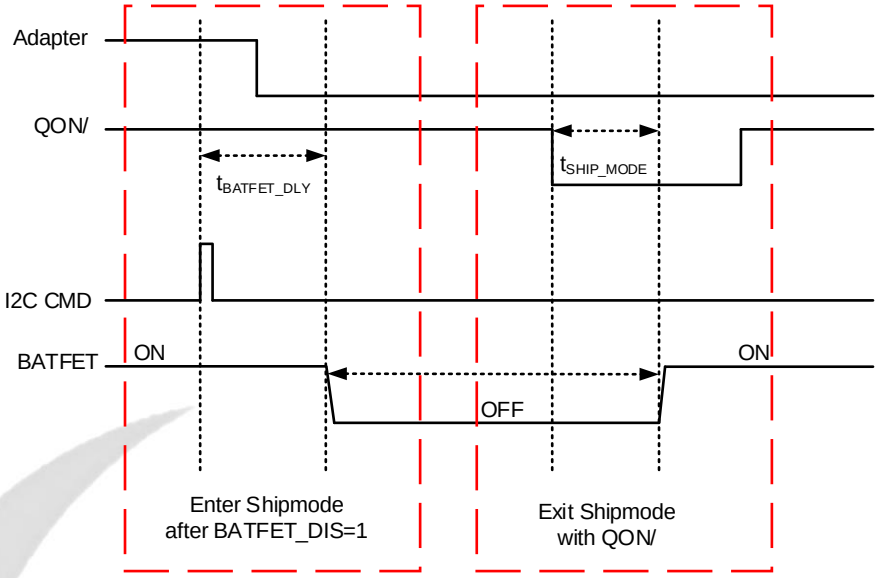


Figure 0-11 Enter and Exit Ship Mode

The GLF70106 supports full system reset, this feature can be used to apply a power-on reset to the system. During full system reset, BATFET turns off for t_{BATFET_RST} and automatically turns on afterward. When the QON/ pin is driven to logic low for t_{QON_RST}, full system reset process starts. It can be disabled by setting BATFET_RST_EN bit to 0. When adaptor is present, full system reset still can be enabled if BATFET_RST_WVUS=1. In this case, the device first gets into HIZ mode to turn off the converter after t_{QON_RST} when QON/ pin is pushed to low and then power cycle BATFET.

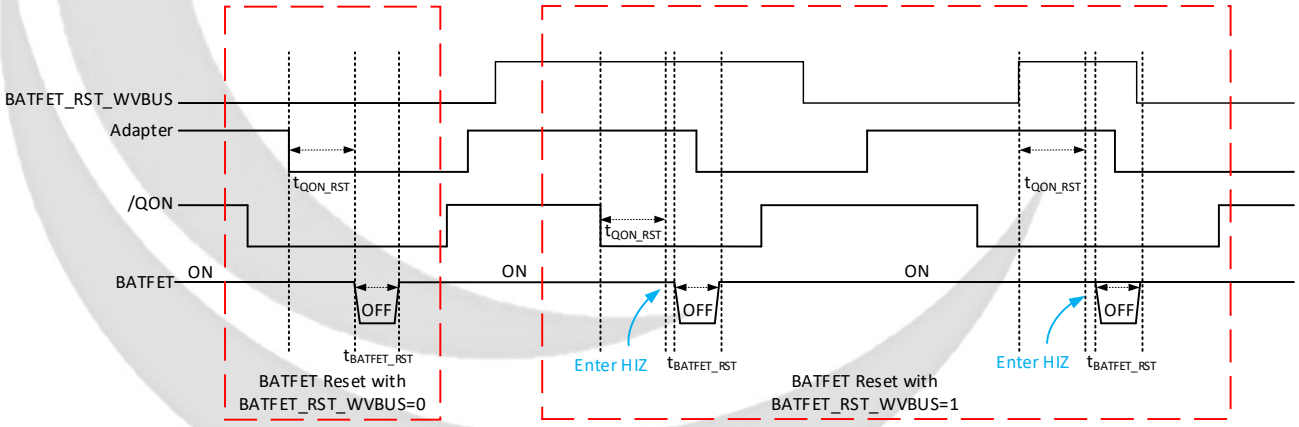


Figure 0-12 System Power Reset Timing

The registers can be reset by following events:

1. The registers with WD reset type can be reset when watch dog timer expires
2. Set REG_RST bit

Thermistor Qualification

The GLF70106 provides a thermistor input for battery temperature monitoring and JEITA. When the temperature is not within acceptable range, the device suspends charging or reduces the charging current or suspends boost.

During charging mode, four temperature levels will be sensed by the voltage on TS pin. The cold range is

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below T1, the cool range is between T1-T2, the normal range is between T2-T3, the warm range is between T3-T5 and the hot range is above T5. The threshold of T1、T2、T3 and T5 can be configured by registers. Due to the sensor negative resistance, a higher temperature results in a lower voltage on TS pin. The GLF70106 exceeds the JEITA requirement by its flexible charge parameter settings. At cool or warm temperatures, the current setting can be reduced to 50% or 25% or 0%. At warm temperature range, the charge voltage can be set to VBATREG-200mV. When charger does not need to monitor the NTC, host sets TS_DIS bit to 1 to ignore the TS pin condition during charging and boost mode. NTC_FAULT bits are 000 when TS_DIS bit is set.

A 103AT-2 type thermistor with resistor divider (31.14KΩ and 5.3KΩ) is recommended for use with the GLF70106.

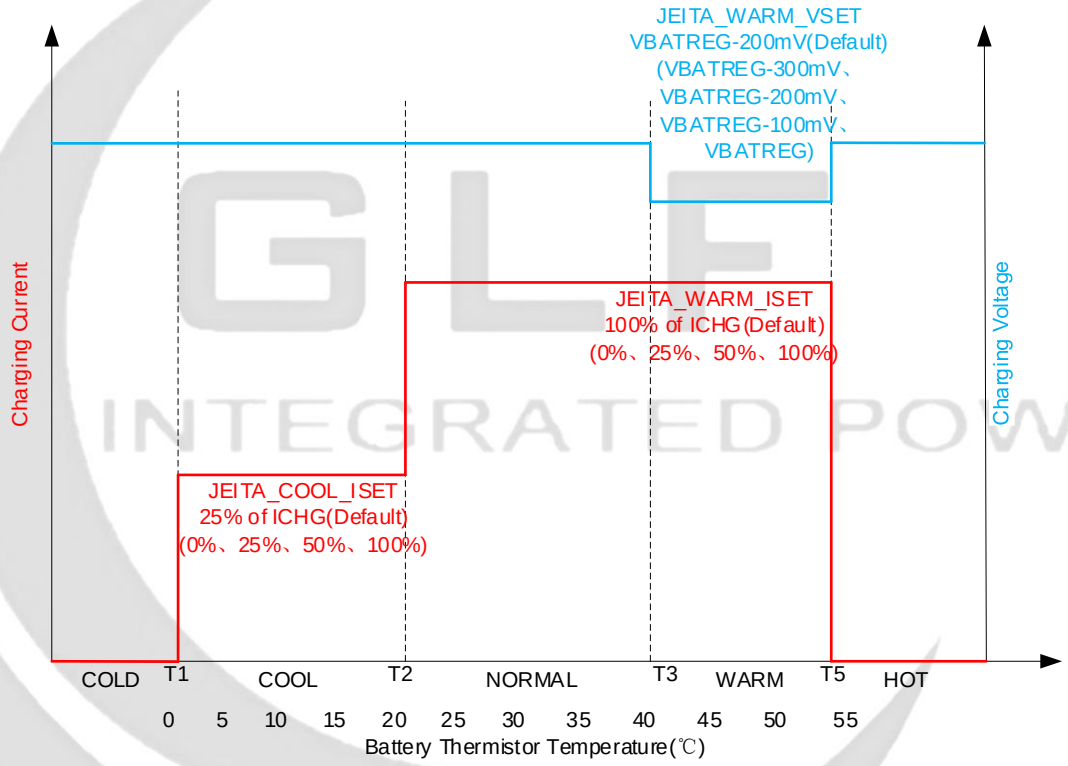


Figure 0-13 TS Charging Values

Status Output Pin (PG/, STAT, INT/)

PG/, STAT and INT/ are open-drain pins.

The PG/ pin goes LOW to indicate a good input source when:

1. V_{VBUS} is above V_{VBUS_UVLOZ}.
2. V_{VBUS} is above $V_{BAT}+V_{SLEEPZ}$ (not in sleep).
3. V_{VBUS} is below V_{BUSOV} threshold.
4. V_{VBUS} is above $V_{VBUS_PRESENT}$ when PMID sink 15mA is applied (not a poor source).

The device indicates charging state on the STAT pin when STAT_CTRL=00. The host can configure STAT pin output state by STAT_CTRL.

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Table 0-4 Charging State

Charging State	STAT Indicator
Charging in progress	LOW
Charging termination	HIZ
Charging disabled	HIZ
Charging suspended (input over-voltage, TS fault, safety timer fault)	Blinking at 1Hz

The INT/ pin is active low and sends an active low,256-us pulse to inform host about a new charger status update or a fault. The following events will generate an INT/ pulse:

1. Good input source detected.
2. Input source removed.
3. Input source type detected.
4. Charge state transition.
5. Charge termination.
6. Any fault event in fault registers.
7. VINDPM / IINDPM events detected.

The device latches the flag in flag registers when fault change occurs until the host reads the registers. Before the host reads, the device would not send an INT/ pulse caused by the same events.

ADC

The GLF70106 provide an integrated 12-bit/11-bit/10-bit/9-bit(programmable) ADC for the host to monitor various system parameters. The higher resolution, the lower the conversion rate.

To enable the ADC, the ADC_EN bit must be set to ‘1’. The ADC is disabled by default (ADC_EN = 0) to conserve power. The ADC is allowed to operate if either VBUS > VPRESENT or VBAT > $V_{BST_BAT_MIN}$ is valid. If ADC_EN is set to ‘1’ before VBUS or VBAT reach their respective valid thresholds, then ADC_EN stays '0'. In charging mode, the host can enable the ADC during HIZ mode by setting ADC_EN = 1.

The ADC_DONE bit is set when a conversion is complete in one-shot mode only. In one-shot mode, the ADC_EN bit is set to 0 at the completion of the conversion, at the same time as the ADC_DONE bit is set and produce INT/ pulse.

In continuous mode, the ADC_EN bit remains at 1 until the user disables the ADC by setting it to 0. During continuous mode, The ADC_Working_STAT bit is used to indicate whether the ADC is performing a conversion, the ADC_DONE bit has no meaning and remain at 0.

Once ADC is enabled, REGN will turn on. To save power consumption, it is strongly recommended to use the one-shot mode in the application. Note, boost mode or only battery standby mode, HIZ bit set will reset ADC_EN bit.

In only Battery mode, ADC_EN bit set, REGN and Buck HS_MOS will turn on, PMID will be equal to VBAT. As shown in the diagram below:

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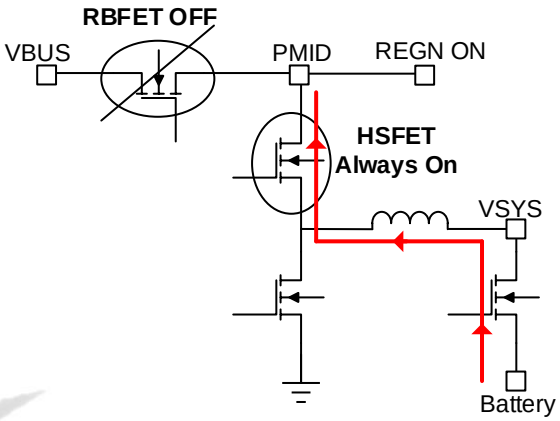


Figure 0-14 ADC_EN Bit Set

In charging mode, the IVBAT charging&discharging current ADC value will be 0 when entering supplement mode.

Protections

The protection features of the GLF70106 are described below:

1. Input Source Over-Voltage Protection (VBUS OVP)

Converter switching will stop when VBUS voltage exceeds $V_{BUSOV.}$ Over-voltage limit that is programmable by VBUS_OVP in Reg00, default 14.2V. Converter will resume its normal operation when the voltage is below to V_{BUSOV} falling threshold. Once VBUS ovp happens, poor source current will discharge the VBUS voltage.

2. System Under-Voltage Protection (SYSUVP)

When the SYS voltage is below V_{BAT_SHORT}, the input current is limited to the lower of 200mA or IINDPM register setting.

3. System Over-Voltage Protection (SYSOVP)

When the system voltage is higher than (VBAT_REG + 180mV) * 1.04, or when the BATFET is operating in LDO mode and the VSYS voltage is higher than (VSYS_MIN+200mV)*1.07, the converter stops switching and pulls the 16mA discharge current.

4. Forward Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak over current protection in the switching MOSFETs. In forward mode, if the current through HSFET exceeds I_{HSFET_OCP}, the converter will immediately turn off the high-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

5. Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. The charger device stops switching when battery over voltage occurs and I_{BAT_LOAD} current pull to discharge.

6. Battery Under-Voltage Protection (BATUVP)

When battery is discharged below V_{BAT_UVLO}, the BATFET will turn off to protect battery from over discharge.

7. Battery Over-Current Protection (BATOCP)

The BATOCP threshold is set by BATFET_OCP in Reg19. If BATFET_OCP = 0, Once IBAT > 8A for a

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20us debounce, the device will latch off BATFET and enter ship mode. If BATFET_OCP = 1, Once 9.5A< IBAT < 12A for at least 20ms debounce, or IBAT > 12A for a 20us debounce , the device will latch off BATFET and enter ship mode.

8. Bypass Mode Reverse-Current Protection (RCP)

In bypass mode, GLF70106 monitors IHSFET for reverse-current into the battery. If current from PMID to the battery exceeds I_{BYPASS_RCP} last for about 2ms, EN_OTG_BYPASS will set to 0, and HSFET will turn off in order to exit bypass OTG mode and the device enters standby mode.

9. Boost Mode Over-voltage Protection

If the PMID voltage exceeds V_{BST_OVP}, the converter will turn off the switching cycle, and the OTG_FAULT_STAT register will be set to 1. Boost OVP will not reset EN_OTG_BST bit.

10. Boost Mode Battery Over-Current Protection

Once IBAT > $I_{SYS_OCP_Q4}$, the device will latch off BATFET and enter ship mode.

11. Boost Mode RBFET Current Limit Protection

Default the RBFET_FORCE_ON=1 and set OTG output, RBFET current will be limited once IBUS > $I_{BST_OCP_Q1}$. The EN_OTG_BST register still keep 1, and set Reg1D[3] Iotg_regulation bit. the GLF70106 will enter current limit regulation.

12. Boost Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak over current protection in the switching MOSFETs. In Boost mode, if the current through LSFET exceeds $I_{BST_LSFET_OCP}$, the converter will immediately turn off the low-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

13. Thermal Shutdown Protection (Tshut)

In boost or charge mode, the converter turns off and EN_OTG_BST bit is set to 0 when IC junction temperature exceeds T_{SHUT}(150deg), recovery about 115deg.

Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When POR, the charger is in default mode, WDT_FAULT_STAT bit is HIGH, WD_FLAG is 0. When the charger is in host mode, WDT_FAULT_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 2-hour trickle/pre-charging safety timer and the 10-hour fast charging safety timer. At the end of the 2-hour or 10-hour timer expired, the charging is stopped and the buck converter continues to operate to supply system load.

A write to any I2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires or disable watchdog timer by setting WDT_SET bits = 00.

When the watchdog expires, the device returns to default mode. A number of other fields are reset to their POR default values as shown in the register maps. When watchdog timer expires, WDT_FAULT_STAT

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and WD_FLAG is set to 1, and an INT is asserted low to alert the host.

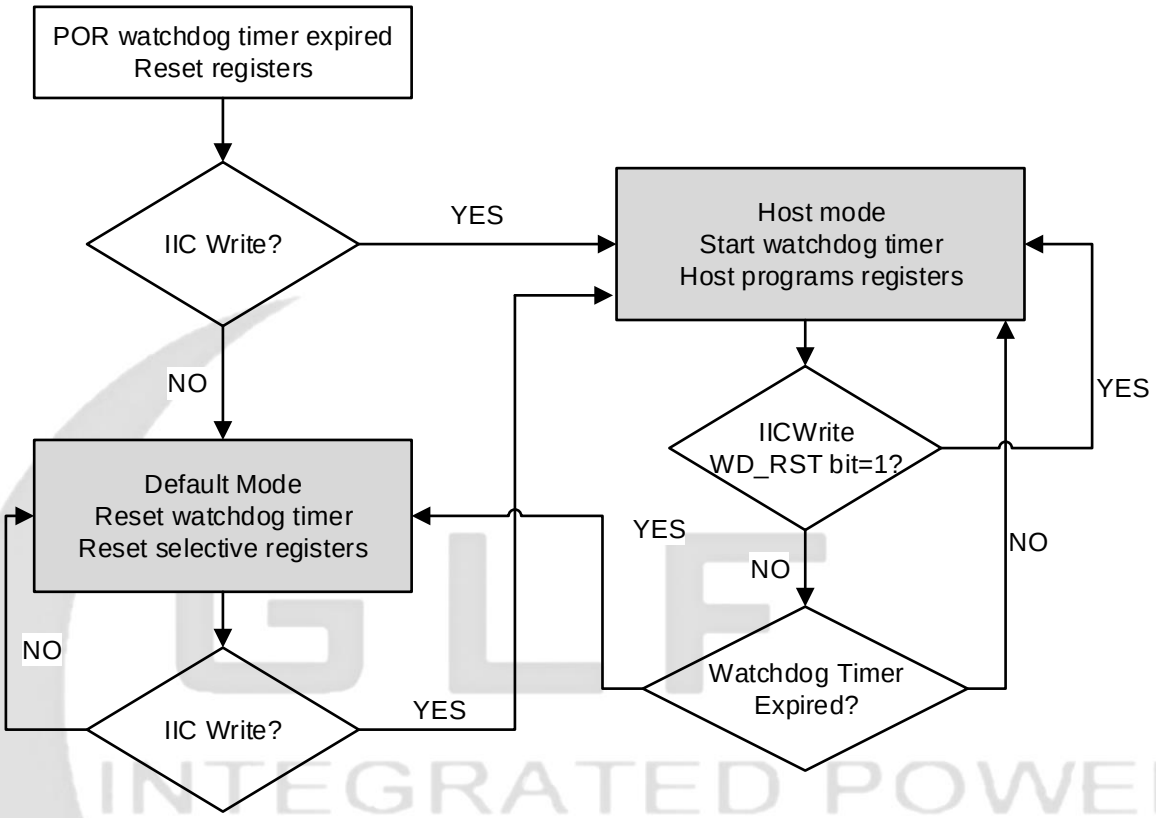


Figure 0-15 Watchdog Timer Flow Chart

I2C interface

The GLF70106 uses I2C compatible interface for flexible charging parameter programming and device status reporting. I2C slave address of the GLF70106 is 0x6B (1101 011B+R/W bit).

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

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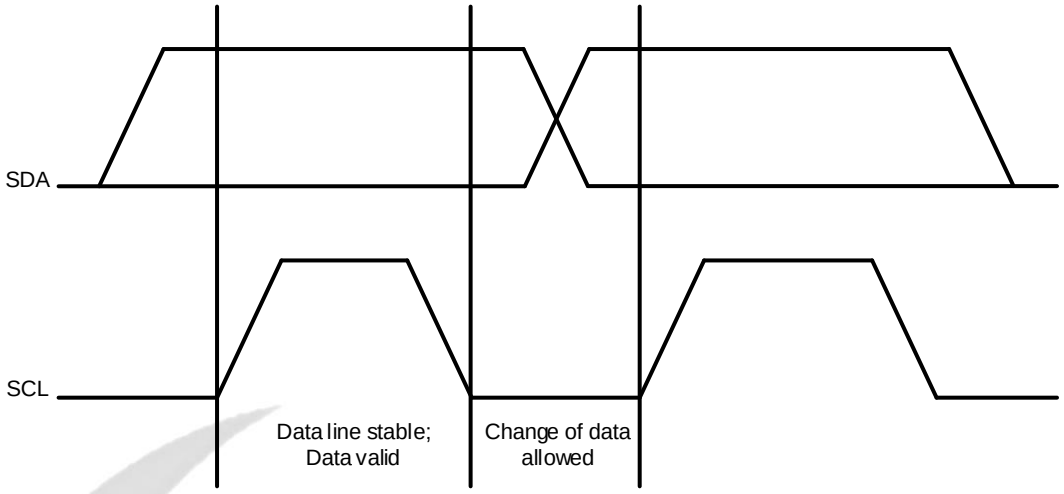


Figure 0-16 Bit transfer on the IIC bus

START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is busy after the START condition, and free after the STOP condition.

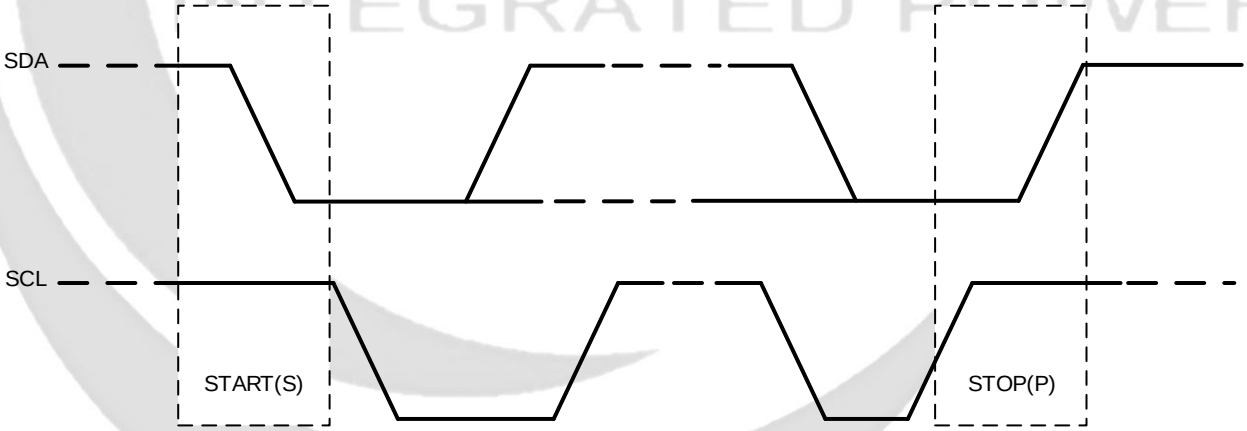


Figure 0-17 START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the host into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases the SCL line.

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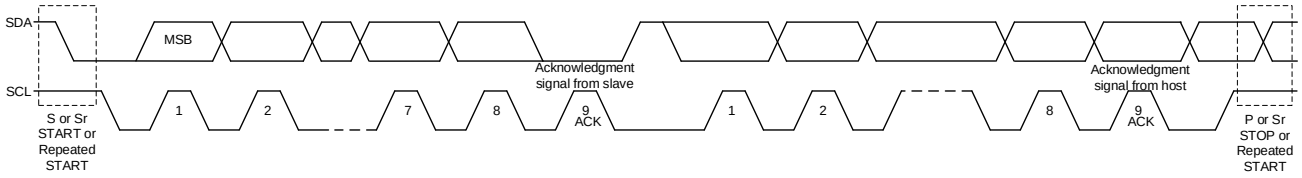


Figure 0-18 Data Transfer on the IIC bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the slave to signal the host that the byte was successfully received and another byte may be sent. During data is transferred, the host can either be the transmitter or the receiver. No matter when, the host generates all clock pulses, including the acknowledge 9th clock pulse.

The host releases the SDA line during the acknowledge clock pulse so the slave can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this 9th clock pulse, this is defined as the Not Acknowledge signal. The host can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

Slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is 7 bits long, followed by an eighth bit as a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

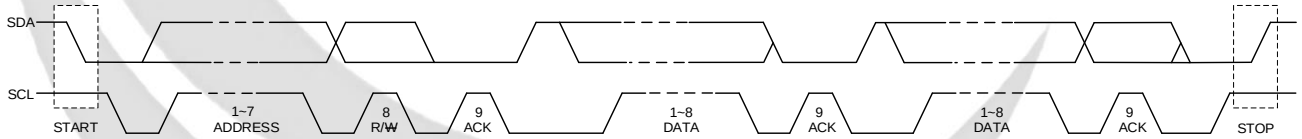


Figure 0-19 Complete data transfer

Single Write and Read

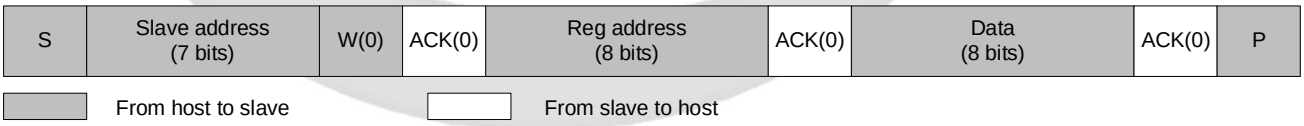


Figure 0-20 Single Write

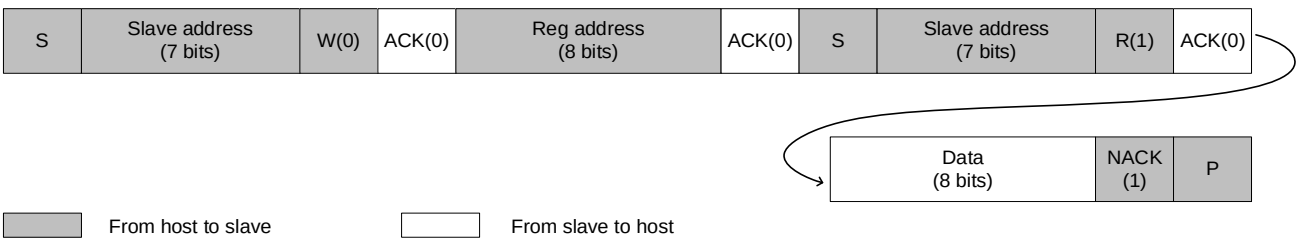


Figure 0-21 Single Write

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The GLF70106 accepts only single-write and single-read operations. If the register address is not defined, the charger IC send back NACK and go back to the idle state.

Register Maps

Register Type	
Type	**Description**
RO	Read only
R/W	Read/Write
W1C	Write 1 bit will be cleared by self
RC	Read Clear
Reset Type	
Reset Type	**Description**
REG_RST	Reset by REG_RST bit
WD	Reset by watchdog timer expires
Plug-in	Reset by adapter Plug-in
ADC_DATA_RST	Reset by ADC_DATA_RST bit

Reg00

Address: 00h Reset: 20h

Bit	Field	Description	Reset	Type	Default
7	Thermal_DIS	Charger thermal loop regulation enable bit 0: enable 1: disable	REG_RST/WD	R/W	0
6	WARM_CHGDONE	Warm charge done control 0: Charging termination disabled at warm temperature 1: Charging termination enabled at warm temperature	REG_RST	R/W	0
5	COOL_CHGDONE	Cool charge done control 0: Charging termination disabled at cool temperature 1- Charging termination enabled at cool temperature	REG_RST	R/W	1
4	NTC_Mode_SEL	NTC not control charger only report states when JEITA set 0: control charger and report states 1: only report states and interrupts	REG_RST	R/W	0
3	NTC_Type	Charger mode NTC type selection 0: JEITA 1: Standard	REG_RST	R/W	0
2:1	VBUS_OVP	VBUS OVP threshold set 00: 14.2V 01: 11V 10: 6.4V 11: 6.0V	REG_RST	R/W	00
0	EN_OTG_BYPASS	OTG bypass mode enable control 0: Disable 1: Enable	REG_RST/WD	R/W	0

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Reg02

Address: 02h Reset: 05h

Bit	Field	Description	Reset	Type	Default
7	ICC_ SCALE	ICC, IPRE and ITERM scale setting 0: 1 times, ICC range from 0 to 2020mA ITERM range from 10mA to 240mA 1: 1.5 times, ICC range from 0 to 3030mA ITERM range from 15mA to 360mA If the bit sets, the ITERM will be scaled synchronously.	REG_RST	R/W	0
6:0	ICC_SET	Fast charging mode current set: Range from 20mA to 2020mA. 000000: 20mA 000001~1000001(65): N*20mA 000001: 20mA ..... 1000001: 1300mA If code ⩾1000010(66), step=60mA 1300 + (N-65)*60mA 1000010: 1360mA 1000011:1420mA 1000100:1480mA 1000101:1540mA 1000110:1600mA 1000111:1660mA 1001000:1720mA 1001001:1780mA 1001010:1840mA 1001011:1900mA 1001100:1960mA 1001101:2020mA ⩾1001101 will be clamped 1001101 Default: 100mA	REG_RST/ WD	R/W	0000101

Reg04

Address: 04h Reset: 10h

Bit	Field	Description	Reset	Type	Default
7:2	VBAT_REG	Battery voltage regulation Range from 3.5 to 4.65V 000000:4.0v 000000-000110(50mv step): 4.0V + N*50mV, 50mv step 000111-101001(10mv step): 00111: 4.31V 01000: 4.32V 01001:4.33V 01010:4.34V 01011:4.35V 01100:4.36V 01101:4.37V 01110:4.38V 01111:4.39V 010000: 4.40V 010001:4.41V	REG_RST/ WD	R/W	000100

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		..... 101001:4.65V 101010:3.5V 101011:3.55V 101100:3.60V 101101:3.65V 101110:3.70V 101111:3.75V 110000:3.80V 110001:3.85V 110010:3.90V 110011:3.95V			
1	RSV				0
0	VBAT_PRE	Pre charge battery voltage set 0: 3.0V 1:3.1V	REG_RST/ WD	R/W	0

Reg06

Address: 06h Reset: 57h

Bit	Field	Description	Reset	Type	Default
7:6	BOOSTILIM	Boost mode current limit 00: 0.5A 01: 1.2A 10: 1.5A 11: 2.4A	REG_RST/ WD	R/W	01
5	BST_VOUT_MSB	Bst_vout_MSB Plus R12[7:5] makes 3bits encoding OTG output voltage	REG_RST	R/W	0
4:0	IINDPM_SET	IINDPM set: 100mA + 100mA* N	REG_RST	R/W	10111

Reg08

Address: 08h Reset: 06h

Bit	Field	Description	Reset	Type	Default
7:4					
3:0	VINDPM	VIN DPM voltage set, offset=3.9V Range: 3.9V(0000) to 5.4V(1111) VINDPM = 3.9V + N*100mV 0000: 3.9V 0001: 4.0V 0010: 4.1V	REG_RST	R/W	0110

Reg10

Address: 10h Reset: A3h

Bit	Field	Description	Reset	Type	Default
7:5	VSYS_MIN	Min VSYS Regulation Set 000:2.6V 001:2.8V 010:3.0V 011:3.2V 100:3.4V 101:3.5V 110:3.6V 111:3.7V	REG_RST	R/W	101
4	RSV				
3:0	IPRECHG	Pre charge mode current set Range from 10mA to 240mA. 0000:10mA IPRE= N*20mA, if code≥1100, IPRE will clamp to 240mA While ICC_SCALE=1, IPRECHG clamp to 300mA	REG_RST/ WD	R/W	0011

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Reg12

Address:12h Reset: 60h

Bit	Field	Description	Reset	Type	Default
7:5	BST_VOUT	Boost regulation voltage setting: R06[5]+R12[7:5], 4 bits encoding If R06[5]=0 0000: 4.60V 0001: 4.75V 0010: 5.0V 0011: 5.15V 0100: 5.30V 0101:5.45V 0110: 5.60V 0111: 5.60V If R06[5]=1 1000: 6.00V 1001: 6.48V 1010: 7.00V 1011: 7.52V 1100: 8.00V 1101: 8.48V 1110: 8.96V 1111: 9.52V	REG_RST	R/W	0011
4	RSV				
3:0	ITERM	Terminal current set: Range from 10mA to 240mA. 0000:10mA(N=0) ITERM=N*20mA(N > 1), if code⩾1100, ITERM will clamp to 240mA,	REG_RST/ WD	R/W	0000

Reg14

Address: 14h Reset: 0Ah

Bit	Field	Description	Reset	Type	Default
7	RBFETFULLON	0: RBFET not fully on when IINDPM ⩽ 500mA 1: RBFET always fully on	REG_RST/ WD	R/W	0
6	TC_CURRENT	Trickle current set 0: 25mA 1: 5mA	REG_RST/ WD	R/W	0
5:4	RSV				
3	EN_TERM	End of charge enable set 0: disable charge done 1: enable charge done	REG_RST/ WD	R/W	1
2:1	VINDPM_BAT_ TRACK	Sets VINDPM to track VBAT Actual VINDPM value is higher of R06 setting and VINDPM_BAT_TRACK 00: VIN set by R08(default) 01: VBAT+200mV 10: VBAT+250mV 11: VBAT+300mV	REG_RST	R/W	01
0	VRECHG	Recharge voltage set 0-120mV 1-210mV	REG_RST/ WD	R/W	0

Reg15

Address: 15h Reset: 4Ch

Bit	Field	Description	Reset	Type	Default
7	DIS_STAT	Disable the STAT pin output 0: enable 1: disable	REG_RST	R/W	0
6	BC1.2_EN	BC1.2 auto detection enable ctrl 0: disable 1: enable	REG_RST	R/W	1
5	IINDET_EN	Force input current type detection 0: not excute input current limit detection	REG_RST/ WD	W1C	0

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		1: Force input current limit detection when VBUS is present			
4	EN_DCP_BIAS	Enable 600mV bias on DP PIN when DCP is detected by BC1.2(VBUS_STAT=011) 0: DCP is detected, DP/DM floating 1: DCP is detected, DP driver 0.6V	REG_RST/ WD	R/W	0
3	TMR2X_EN	Safety timer double during DPM/Thermal 0: disable 1: enable	By REG	R/W	1
2	EN_TIMER	Charger safety timer enable set 0: disable 1: enable	REG_RST/ WD	R/W	1
1	PRE_CHG_TMR	Pre-charge safety timer setting: 0: 2hrs 1: 0.5hrs	REG_RST	R/W	0
0	CHG_TMR	Fast charge safety timer setting: 0: 10hrs 1: 20hrs	REG_RST	R/W	0

Reg16

Address: 16h Reset: 23h

Bit	Field	Description	Reset	Type	Default
7	FORCE_VBAT_DSG	Force battery discharge current 0: not force 1: force a discharge current on VBAT	REG_RST/ WD	R/W	0
6	EN_OTG_BST	OTG mode enable control 0: Disable 1: Enable	REG_RST/ WD	R/W	0
5	CHG_EN	Charger enable control bit 0: Charger disable 1: Charger enable, GLF70106 will turn on BATFET to charge the battery when the bit is set and CE/ pin is low and no fault.	REG_RST/ WD	R/W	1
4	EN_HIZ	HIZ mode enable in buck mode. 0: Disable 1: Enable	REG_RST/ WD/Plug-in	R/W	0
3	FORCE_PMID_DSG	Force PMID discharge current 0: Disable 1: Enable	REG_RST/ WD	R/W	0
2	WDT_RST	0: normal 1: WDT_RST	W1C	R/W	0
1:0	WDT_SET	Watch dog timer set 00: disable 01:40s 10:80s 11:160s	REG_RST/ WD	R/W	11

Reg17

Address: 17h Reset: 40h

Bit	Field	Description	Reset	Type	Default
7	REG_RST	Reset registers to default values 0: Not reset 1: Reset		W1C	0
6	THERMAL_REG	Thermal regulation set 0: 90deg 1: 110deg	REG_RST	R/W	1

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5:4	ADC_SAMPLE	ADC sample rate 00: 12 bits 01: 11 bits 10: 10 bits 11: 9 bits	REG_RST	R/W	00
3	CHG_SW_SLEW_RATE_SET	Charger SW node slew rate ctrl 0: normal 1: fast	REG_RST	R/W	0
2	BST_SW_SLEW_RATE_SET	Boost SW node slew rate ctrl 0: normal 1: fast	REG_RST	R/W	0
1	ADC_EN	ADC enable control 0: disable 1: enable	REG_RST/ WD	R/W	0
0	ADC_Mode	ADC conversion mode control 0:Continuous mode 1:One shot mode	REG_RST	R/W	0

Reg18

Address: 18h Reset: 04h

Bit	Field	Description	Reset	Type	Default
7	RSV				0
6	ADC_DATA_RST	ADC data reset when adc_en =0 0:not reset 1:reset	W1C		0
5	PFM_DIS	0: PFM Enable 1: PFM DIS	REG_RST	R/W	0
4	RSV				
3	BATFET_RST_WVBUS	BATFET full system reset with or without adapter present. 0: BATFET will not execute full system reset when adapter is present on VBUS 1: BATFET will excute full system reset when adapter is present on VBUS		R/W	0
2	BATFET_DLY	Delay from BATFET_DIS. 0: Turn off BATFET immediately when BATFET_DIS bit is set. 1: Turn off BATFET after t_{BATFET_DLY} (typ 10s) when BATFET_DIS bit is set.	REG_RST	R/W	1
1	BATFET_DIS	BATFET Q4 ON/OFF control. Set this bit to 1 to enter ship mode. To reset the device with adapter present, the host shall set BATFET_RST_WVBUS to 1 and then BATFET_DIS to 1. 0 – Turn on Q4. (default) 1 – Turn off Q4 after t_{BATFET_DLY} delay time	REG_RST /Plug-in	R/W	0
0	CD_debounce	Charge done debounce 0: 250ms 1:35ms		RWF	0

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Reg19

Address: 19h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:3	RSV				
2	BATFET_OCP	BATFET OCP set 0: 8.0A 1:12.0A	REG_RST	R/W	0
1	FORCE_VSYS_DSG	Force a VSYS discharge current 0: disable 1:enable	REG_RST/WD	R/W	0
0	RSV				

Reg1A

Address: 1Ah Reset: 0Dh

Bit	Field	Description	Reset	Type	Default
7	TS_DIS	0: NTC enable 1: NTC disable	REG_RST	R/W	0
6:5	OTG_NTC_HOT_SET	00: 55deg 01: 60 10: 65 11:disable	REG_RST	R/W	00
4	OTG_NTC_COLD_SET	0:-20deg 1:-10deg	REG_RST	R/W	0
3:2	NTC_WARM_ISET	ICC&IPRE setting during warm temp region 00: charger suspend 01: 25% of ICC 10: 50% of ICC 11: Keep ICC	REG_RST	R/W	11
1:0	NTC_COOL_ISET	ICC&IPRE setting during cool temp region 00: charger suspend 01: 25% of ICC 10: 50% of ICC 11: Keep ICC	REG_RST	R/W	01

Reg1B

Address: 1Bh Reset: D5h

Bit	Field	Description	Reset	Type	Default
7	CHG_NTC_COLD_SET	Charger mode NTC cold temp set 0: -5deg 1: 0deg	REG_RST	R/W	1
6	CHG_NTC_HOT_SET	Charger mode NTC hot temp set 0: 50deg 1 60deg	REG_RST	R/W	1
5:4	CHG_NTC_COOL_SET	Charger mode NTC cool temp set 00: 5deg 01:10deg 10: 15deg 11: 20deg	REG_RST	R/W	01
3:2	NTC_WARM_SET	Charger mode NTC warm temp set 00:40deg 01:45deg 10: 50deg 11: 55deg	REG_RST	R/W	01
1:0	NTC_WARM_VSET	VBATREG set during NTC warm temp 00: VBATREG-300mv 01: VBATREG-200mv 10: VBATREG-100mv 11: VBATREG 4.1V	REG_RST	R/W	01

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Reg1D

Address: 1Dh Reset: 01h

Bit	Field	Description	Reset	Type	Default
7	RSV				
6	ADC_Working_STAT	ADC conversion status 0: conversion not complete 1: conversion complete		RO	0
5	THERM_STAT	Thermal regulation status 0: not in thermal regulation status 1: in thermal regulation status		RO	0
4	VSYS_STAT	VSYS regulation status 0: not in min_vsys regulation 1: in min_vsys regulation		RO	0
3	IINDPM_STAT	0: not in IINDPM or IOTG regulation 1: in IINDPM or IOTG regulation		RO	0
2	VINDPM_STAT	0: not in VINDPM 1: in VINDPM		RO	0
1	RSV				
0	WDT_FAULT_STAT	Watch dog timer out or not 0: WDT not fault 1: WDT fault		RO	1

Reg1E

Address: 1Eh Reset: 00h

Bit	Field	Description	Reset	Type	Default
7	JEITA_Chg_Done	Charge done state during JEITA region 0: not charge done 1: charge done		RO	0
6	VBUS_PG_STAT	VBUS power good status 0: not good 1: VBUS power good		RO	0
5:3	CHG_STAT	Charging status 000: not charge 001: trickle or pre-charge 010: CC charge 011: CV charge 100:charge done		RO	000
2:0	VBUS_STAT	VBUS status 000: No input(BC1.2 disable or no input) 001: SDP 010: CDP 011: DCP 101: unknown(500mA) 110: Non-standard adapter(1A/2A/2.1A/2.4A) 111: OTG	-	RO	000

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Reg1F

Address: 1Fh Reset: 00h

Bit	Field	Description	Reset	Type	Default
7	BAT_FAULT_STAT	0: normal 1: battery ovp		RO	0
6	VSYS_FAULT_STAT	VSYS ovp during charger mode 0: normal 1: vsys ovp		RO	0
5	OTG_FAULT_STAT	0: normal 1: boost fault (VBAT too low/Boost OCP/Boost OVP/RCP)		RO	0
4:3	CHG_FAULT	00: normal 01: input fault (VBUS OVP) 10: thermal shut down 11: charge safety timer out		RO	00
2:0	NTC_FAULT	000: normal 001: cold or OTG_cold 010: hot or OTG_hot 011: cool 100: warm 101-111: RSV		RO	00

Reg20-Flag

Address: 20h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7	ADC_DONE	ADC convert done when one-shot mode		RC	
6	BC1.2_DET_DONE	BC1.2detection finished pending bit		RC	
5	Thermal_FLAG	thermal regulation interrupt pending bit		RC	
4	QON FLAG	QON 60ms /1.5s press event		RC	
3	IINDPM_FLAG	IINDPM or IOTG regulation interrupt pending bit		RC	
2	VINDPM_FLAG	VINDPM regulation interrupt pending bit		RC	
1	OTG_VBUS_FLAG	VBUS plug in pending bit when RBFET off during OTG		RC	
0	WD_FLAG	Watchdog timer out pending bit		RC	

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Reg22-Flag

Address: 22h Reset: C0h

Bit	Field	Description	Reset	Type	Default
7	RSV				
6	BAT_OVP_FLAG	Battery over voltage pending bit		RC	
5	RSV				
4	OTG_FAULT_FLAG	Boost fault: VBAT too low/Boost OCP/Boost OVP/RCP OTG fault pending bit		RC	
3	Input fault	OVP or not qualify poor source pending bit			
2	TSHUT_FLAG	Die over temp pending flag		RC	
1	Safety_TMR_OUT_FLAG	Charger timer out pending bit		RC	
0	NTC_FAULT_FLAG	NTC pending flag 0: normal 1: NTC status transition was detected		RC	

Reg23-MASK

Address: 23h Reset: 03h

Bit	Field	Description	Reset	Type	Default
7	CHG_MASK	Charger status transition INT mask bit 0: not mask 1: mask	REG_RST	R/W	0
6	RSV				
5	THERMAL_MASK	Charger thermal loop INT mask bit 0: not mask 1: mask	REG_RST	R/W	0
4	RSV				
3	VINDPM_INT_MASK	VINDPM interrupt mask bit 0: not mask, Enter VINDPM produce INT pulse 1: mask, Enter VINDPM not produce INT pulse	REG_RST	R/W	0
2	IINDPM_INT_MASK	IINDPM interrupt mask bit 0: not mask, Enter IINDPM produce INT pulse 1: mask, Enter IINDPM not produce INT pulse	REG_RST	R/W	0
1	SHORTPRESS_INT	QON/ short press int enable ctrl 0: not mask, Disable short key press interrupt 1: mask, Enable short key press interrupt	REG_RST	R/W	1
0	LONGPRESS_INT	QON/ long press int enable ctrl 0: not mask, Disable long key press interrupt 1: mask, Enable long key press interrupt	REG_RST	R/W	1

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Reg24: Revision&Chip ID

Address: 24h Reset: 44h

Bit	Field	Description	Reset	Type	Default
7:5	Revision	Revision information		RO	010
4:3	RSV				00
2:1	Chip_ID	GLF70106 ID		RO	10
0	Slaver_Addr	Slaver address set 0: 7'h6B 1: 7'h66		RO	0

Reg25

Address: 25h Reset: 04h

Bit	Field	Description	Reset	Type	Default
7:6	RSV				
5:4	STAT_CTRL	STAT pin control 00: Charger state 01: HIZ 10: LOW 11: 1Hz 50% blinking	REG_RST	R/W	00
3	CE/_DIS	CE/ PIN control charger enable 0: Charging enable is controlled by CE/ PIN 1: Charging enable is not controlled by CE/ PIN	REG_RST	R/W	0
2	QON_WK_EN	QON press to wake up from ship mode 0: disable QON wake up 1: enable QON wake up	REG_RST	R/W	1
1	Cold Reset	VSYS reset by software command 0: no action 1: VSYS reset	-	W1C	0
0	QON_WK_Time	QON wake up ship mode timing set 0: 1.1s 1: 35ms	REG_RST/WD	R/W	0

Reg26

Address: 26h Reset: 05h

Bit	Field	Description	Reset	Type	Default
7	VBUSRST_EN	VBUS plug in to reset VSYS 0: Disable full system reset trigger by VBUS insertion 1: Enable full system reset trigger by VBUS insertion	REG_RST	R/W	0
6:5	RSV				
4	WDT_VSYS_RST	0: only reset registers when WDT time out 1: VSYS and Registers reset when WDT time out	REG_RST	R/W	0
3	IINDPM_VINDPM_DIS	IINDPM/VINDPM disable control 0: enable 1: disable	REG_RST	R/W	0
2	BATFET_RST_EN	Enable BATFET full system reset. 0: Disable BATFET reset function 1: Enable BATFET reset function	REG_RST/WD	R/W	1
1	RSV				0
0	RBFET_FORCE_ON	0: Turn off RBFET boost mode 1: Turn on RBFET boost mode		R/W	1

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Reg27_ADC_CHAL

Address: 27h Reset: FFh

Bit	Field	Description	Reset	Type	Default
7	VBAT_Channel	VBAT_Channel enable control 0: disable 1:enable	REG_RST	RW	1
6	NTC_Channel	NTC_Channel enable control 0: disable 1:enable	REG_RST	RW	1
5	VBUS_Channel	VBUS_Channel enable control 0: disable 1:enable	REG_RST	RW	1
4	IBAT_Channel	IBAT_Channel enable control 0: disable 1:enable	REG_RST	RW	1
3	IBUS_Channel	IBUS_Channel enable control 0: disable 1:enable	REG_RST	RW	1
2	VSYS_Channel	VSYS_Channel enable control 0: disable 1:enable	REG_RST	RW	1
1	TDIE_Channel	TDIE_Channel enable control 0: disable 1:enable	REG_RST	RW	1
0	PMID_Channel	PMID_Channel enable control 0: disable 1:enable	REG_RST	RW	1

Reg28_VBAT_ADC_Low

Address: 28h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:0	VBAT_ADC_LOW	VBAT ADC reading VBAT_ADC[7:0] LSB: 2mV Range: 0mV ~ 6000mV	ADC_DATA_RST		

Reg29_VBAT_ADC_High

Address: 29h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:4	RSV				
3:0	VBAT_ADC_High	VBAT_ADC[11:8]	ADC_DATA_RST		

Reg2A_NTC_ADC_Low

Address: 2Ah Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:0	NTC_ADC_Low	TS ADC reading as TS pin voltage in percentage of REGN. NTC_ADC[7:0] LSB: 0.0961% Range: 0% ~ 90%	ADC_DATA_RST		

Reg2B_NTC_ADC_High

Address: 2Bh Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:4	RSV				
3:0	NTC_ADC_High	NTC_ADC[11:8]	ADC_DATA_RST		

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Reg2C_VBUS_ADC_Low

Address: 2Ch Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:0	VBUS_ADC_Low	VBUS ADC reading VBUS_ADC[7:0] LSB: 5mV Range: 0mV ~ 15000mV	ADC_DATA_RST		

Reg2D_VBUS_ADC_High

Address: 2Dh Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:4	RSV				
3:0	VBUS_ADC_High	VBUS_ADC[11:8]	ADC_DATA_RST		

Reg2E_IBAT_ADC_Low

Address: 2Eh Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:0	IBAT_ADC_Low	IBAT ADC reading Reported in 2 's Complement. The IBAT ADC reports positive value for the battery charging current, and negative value for the battery discharging current. IBAT_ADC[7:0] LSB: 4mA Range: -5000mA ~ 4000mA	ADC_DATA_RST		

Reg2F_IBAT_ADC_High

Address: 2Fh Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:4	RSV				
3	Signed bit	0:charge 1:discharge	ADC_DATA_RST		
2:0	IBAT_ADC_High	IBAT_ADC[10:8]	ADC_DATA_RST		

Reg30_IBUS_ADC_Low

Address: 30h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:0	IBUS_ADC_Low	IBUS ADC reading Reported in 2 's Complement. When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value. IBUS_ADC[7:0] LSB: 2mA Range: -2400mA ~ 3200mA	ADC_DATA_RST		

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Reg31_IBUS_ADC_High

Address: 31h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:4	RSV				
3	Signed bit	0: Current is flowing from VBUS to PMID 1: Current is flowing from PMID to VBUS	ADC_DATA_RST		
2:0	IBUS_ADC_High	IBUS_ADC[10:8]	ADC_DATA_RST		

Reg32_VSYS_ADC_Low

Address: 32h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:0	VSYS_ADC_Low	VSYS ADC reading VSYS_ADC[7:0] LSB: 2mV Range: 0mV ~ 6000mV	ADC_DATA_RST		

Reg33_VSYS_ADC_High

Address: 33h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:4	RSV				
3:0	VSYS_ADC_High	VSYS_ADC[11:8]	ADC_DATA_RST		

Reg34_TDIE_ADC_Low

Address: 34h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:0	TDIE_ADC_Low	TDIE ADC reading TDIE_ADC[7:0] LSB: 0.5℃ Range: -40℃ ~ 150℃	ADC_DATA_RST		

Reg35_TDIE_ADC_High

Address: 35h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:4	RSV				
3	Signed bit	0: above 0℃ 1: below 0℃			
2:0	TDIE_ADC_High	TDIE_ADC[10:8]	ADC_DATA_RST		

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Reg36_PMID_ADC_Low

Address: 36h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:0	PMID_ADC_Low	VPMID ADC reading PMID_ADC[7:0] LSB: 5mV Range: 0mV ~ 15000mV	ADC_DATA_RST		

Reg37_PMID_ADC_High

Address: 37h Reset: 00h

Bit	Field	Description	Reset	Type	Default
7:4	RSV				
3:0	PMID_ADC_High	PMID_ADC[11:8]	ADC_DATA_RST		

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Application and Implementation

System Example

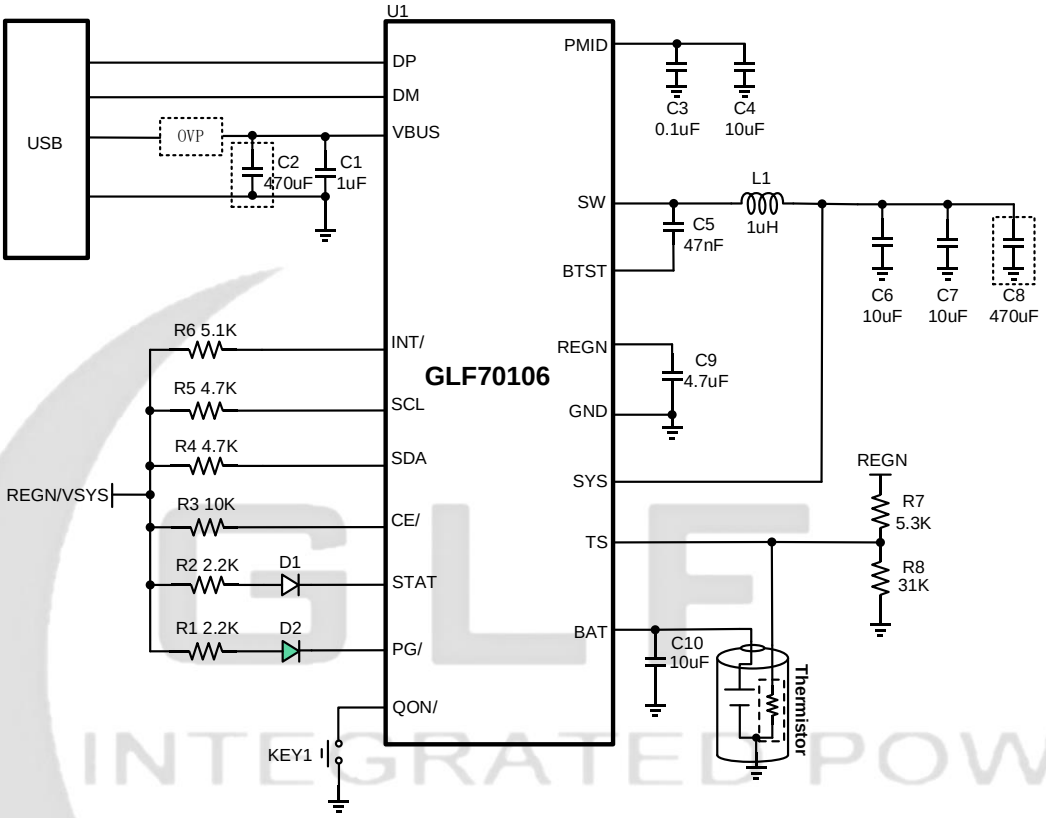


Figure 0-1. System Example

Bill of Materials

Components	Device type	Device description	Manufacturer	Parameter	Quantity
C1	Capacitor	MLCC/0603/1μF/X5R/20%/35V	Samsung	1μF/35V	1
C2/C8	Capacitor	Optional, 470μF/20%/50V		470μF	1
C3	Capacitor	MLCC/0603/0.1μF/X7R/10%/25V	Samsung	0.1μF/25V	1
C4	Capacitor	MLCC/0603/10μF/X5R/20%/25V	Samsung	10μF/25V	1
C5	Capacitor	MLCC/0603/47nF/X5R/20%/50V	Samsung	47nF/50V	1
C6/C7/C10	Capacitor	MLCC/0603/10μF/X5R/20%/10V	Samsung	10μF/10V	1
C9	Capacitor	MLCC/0603/4.7μF/X5R/20%/10V	Samsung	4.7μF/10V	1
L1	Inductor	1μH,Tolerance ±20%,Saturation rated current > 4.7A	MuRata	1μH	1
R1/R2	Resistor	0603/2.2K/±1%		2.2K	1
R3	Resistor	0603/10K/±1%		10K	1
R4/R5	Resistor	0603/4.7K/±1%		4.7K	1
R6	Resistor	0603/5.1K/±1%		5.1K	1
R7	Resistor	0603/5.3K/±1%		5.3K	1
R8	Resistor	0603/31K/±1%		31K	1
U1	IC	QFN 2.5*3	ThinkFuture	GLF70106	1

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Package Outline and Layout

Package Outline

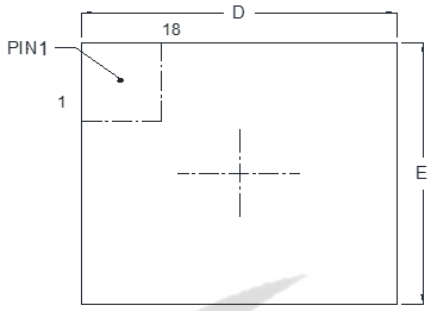


Figure 0-1. Top View

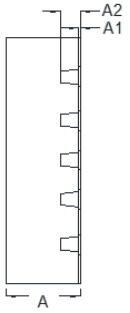


Figure 0-2. Side View

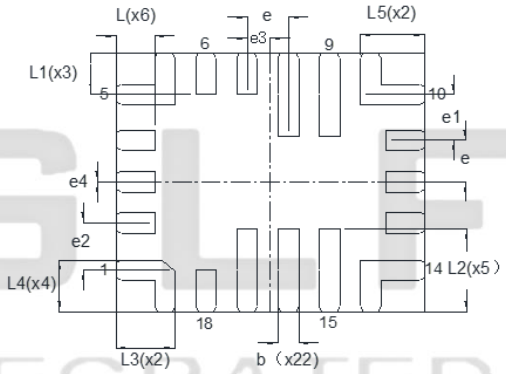


Figure 0-3. Bottom View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF.		0.008 REF.	
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.400	2.600	0.094	0.102
e	0.400 BSC.		0.016 BSC.	
e1	0.443 BSC.		0.017 BSC.	
e2	0.457 BSC.		0.018 BSC.	
e3	0.225 BSC.		0.009 BSC.	
e4	0.007 BSC.		0.0003 BSC.	
L	0.325	0.425	0.013	0.017
L1	0.350	0.450	0.014	0.018
L2	0.750	0.850	0.030	0.033
L3	0.475	0.675	0.019	0.027
L4	0.400	0.600	0.016	0.024
L5	0.575	0.675	0.023	0.027

All specs and applications shown above subject to change without prior notice.

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Layout

Layout Guidelines

The switching node rise and fall times should be minimized for lowest switching loss. Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane. See Figure 0-5.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane. See Figure 0-6.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane. See Figure 0-5.
4. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
5. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
6. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there is enough thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.

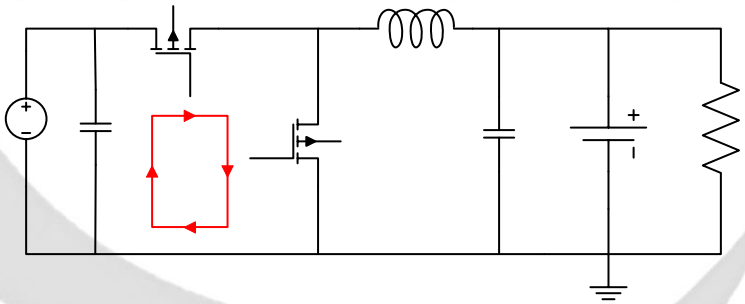


Figure 0-4 High Frequency Current Path

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Layout Example

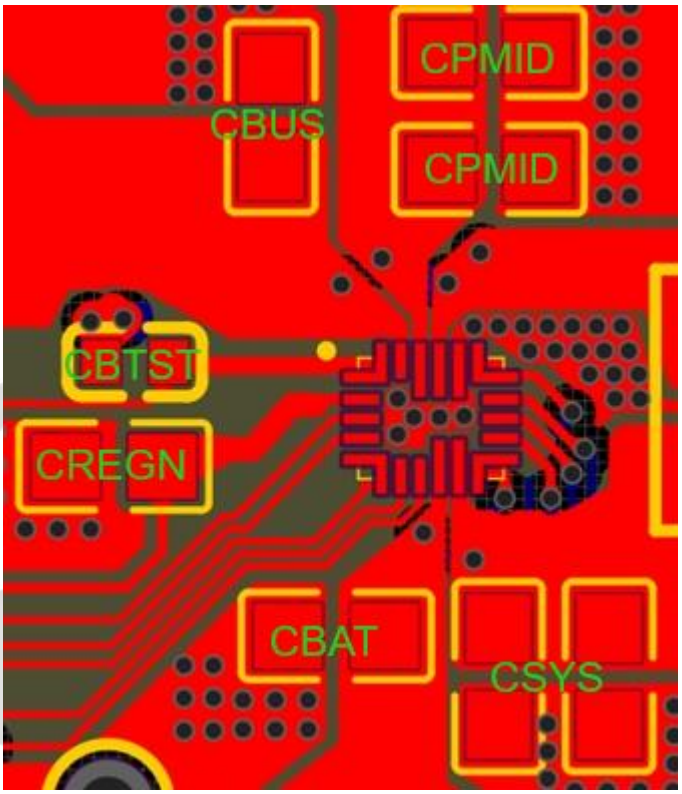


Figure 0-5 Layout Example: PMID Capacitor; BAT Capacitor; VSYS Capacitor

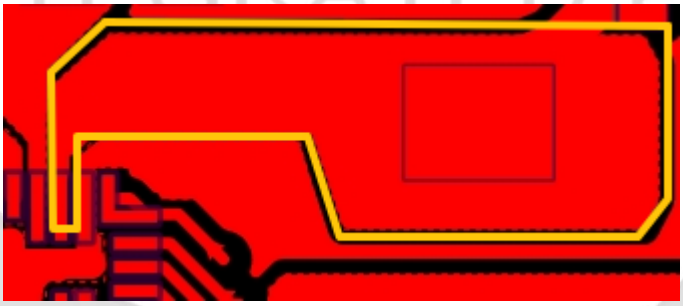


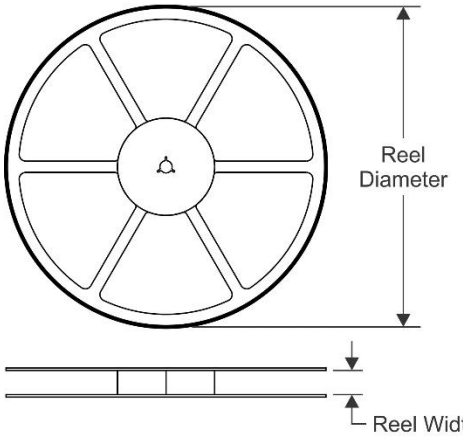
Figure 0-6 Layout Example: SW Node

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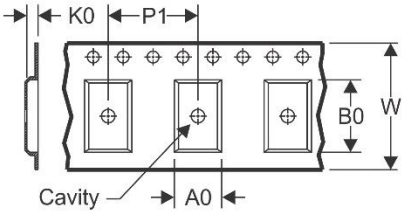
Packaging and Ordering Information

Tape and Reel Information

REEL DIMENSIONS

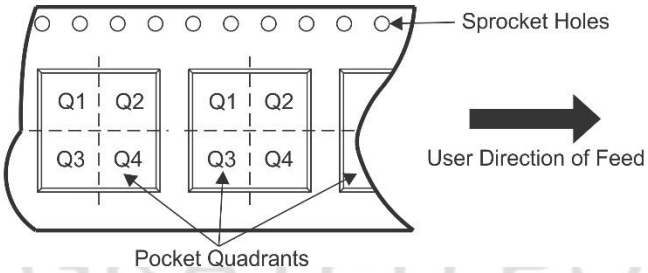


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
GLF70106	QFN	2.5x3	18	5000	330	12	3.3	2.8	1.1	8	12	Q1

Package Quantity Information

Device	Package Type	Moisture Sensitivity Level	Qty per plate	Qty per box	Qty per trunk
GLF70106-Q53	QFN 2.5x3	3	5000	5000	40000

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