1 Features

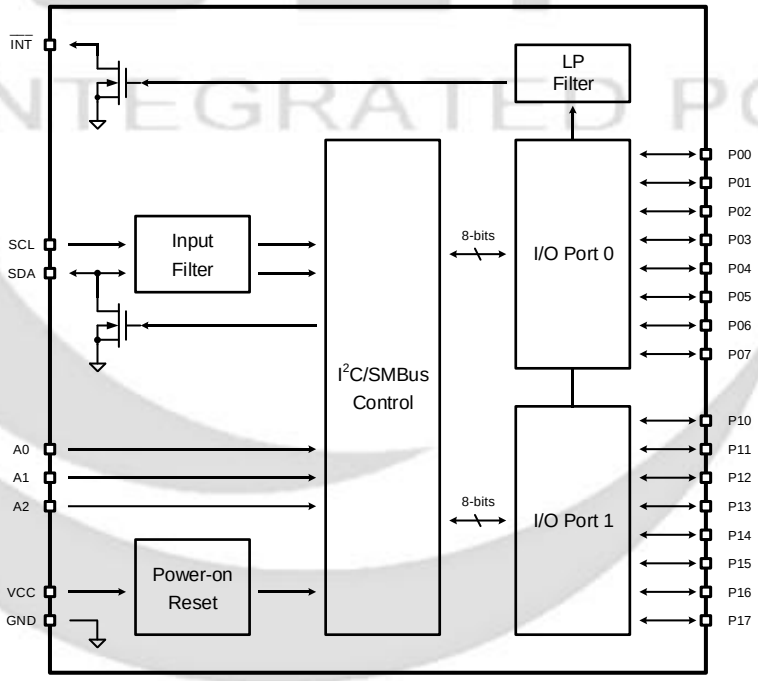
- Supply Range: 1.6V~5.5V
- Temperature Range: -55°C ~ +125°C
- Standby Current: 0.5μA
- High-Current Drive Capability
- Open-Drain Active-Low Interrupt Output

2 Applications

- Servers
- Routers
- Communication Cabinet
- Industrial Automation
- Products with GPIO-Limited Processors

3 Description

The GLF77535 provides general purpose parallel input and output (GPIO) expansion. Port data is transmitted through the standard I2C protocal, which can support up to 1MHz communication rate (and up to 2MHz when high-speed mode is enabled). The GLF77535 features a 16-bit totem-pole I/O ports (P07-P00, P17-P10), which can directly drive LEDs. Each bit of a GPIO port can be individually configured as an input or output. At power on, the I/Os are configured as inputs.



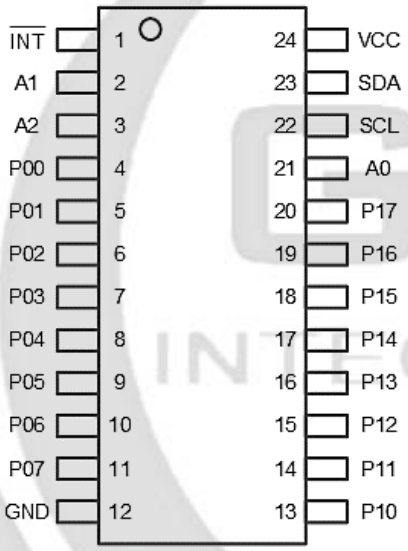
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4 Order Information

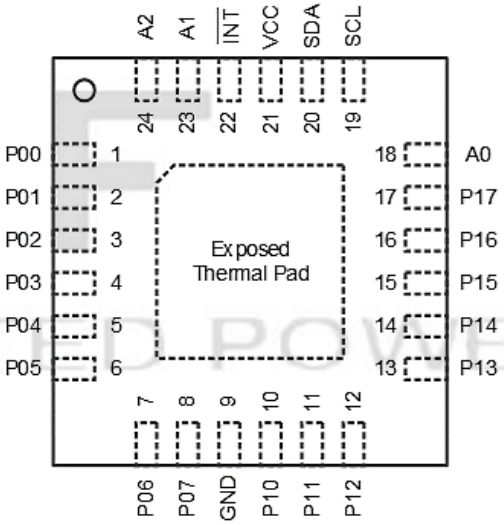
ORDER CODE	PACKAGE	QUANTITY	PACKING
GLF77535-P23	TSSOP-24L	4000	Tape&Reel
GLF77535-Q43	QFN4x4-24L	4000	Tape&Reel

5 Pin Configuration

GLF77535-P23
Top View



GLF77535-Q43
Top View



PIN			DESCRIPTION
NAME	TSSOP	QFN	
A0	21	18	Address input 0. Connect directly to VCC or GND.
A1	2	23	Address input 1. Connect directly to VCC or GND.
A2	3	24	Address input 2. Connect directly to VCC or GND.
GND	12	9	Ground.
INT	1	22	Interrupt open-drain output. Connect to VCC through a pull-up resistor.
P00 ~ P07	4 ~ 11	1 ~ 8	P-port I/O. At power on, all I/Os are configured as inputs.
P10 ~ P17	13 ~ 20	10 ~ 17	P-port I/O. At power on, all I/Os are configured as inputs.
SCL	22	19	Serial clock bus. Connect to VCC through a pull-up resistor.
SDA	23	20	Serial data bus. Connect to VCC through a pull-up resistor.
VCC	24	21	Supply voltage.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Voltage	- 0.5	6	V
Storage Temperature	- 65	150	°C
Input-output Clamp Current		± 20	mA
Continuous Output Current		± 50	mA
Continuous Current through GND		- 250	mA
Continuous Current through VCC		+ 160	mA

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.

6.2 ESD Ratings

		VALUE	UNIT
Electrostatic Discharge	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	± 8000	V
Latch-up	Latch-Up, per JESD 78, Class IA	± 200	mA
Charged-Device Model	Charged-Device Model (CDM), per ANSI/OESDA/JEDEC JS-002-2022	± 1500	V

6.3 Electrical Characteristic

Over temperature range of -55~+125°C and supply range of 1.6~5.5V, unless otherwise noted. Typical values at +25°C and 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage, V_{CC}		1.6	3.3	5.5	V
Operating Temperature, T_A		- 55		125	°C
Quiescent Current, I_{CC}			0.5	5	μA
P-port High-level Output Voltage, V_{OH}	I_{OH} = -8mA, V_{CC} = 3V		2		V
	I_{OH} = -8mA, V_{CC} = 4.75V		4.2		V
	I_{OH} = -10mA, V_{CC} = 3V		1.8		V
	I_{OH} = -10mA, V_{CC} = 4.75V		4.2		V
P-port Low-Level Output Current, I_{OL}	V_{OL} = 0.5V, V_{CC} = 1.6V~5.5V	8			mA
	V_{OL} = 0.7V, V_{CC} = 1.6V~5.5V	10			mA
SDA Low-level Output Current, I_{OL}	V_{OL} = 0.4V, V_{CC} = 1.6V~5.5V	3			mA
INT Low-level Output Current, I_{OL}	V_{OL} = 0.4V, V_{CC} = 1.6V~5.5V	3			mA
Input Current, I_I	V_I = V_{CC} or GND			± 1	μA

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7 Detailed Description

7.1 Port Structure

A simplified cicuirt diagram of P-port I/Os is shown in **Figure 1.**

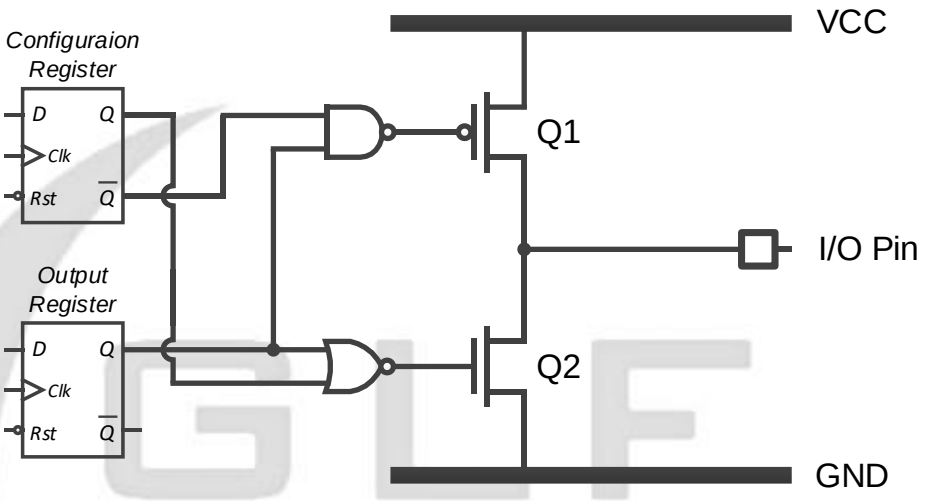


Figure 1. Simplified Circuit Diagram of P-port I/Os

When an I/O is configured as an input, FETs Q1 and Q2 are off, which create a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5V.

When an I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the *Output Port* register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

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7.2 Register Map

The GLF77535 register file consists of two sets of symmetric registers that control ports 0 and 1, respectively, in bytes. Each set comprises four 8-bit registers where each bit corresponds to a specific I/O pin; for instance, bit 0 at port 0 corresponds to P00 and so forth**. Table 1** lists the pointer address of the register map.

Table 1. Pointer Address and Register Map

POINTER	REGISTER NAME	ATTRIBUTION	DEFAULT VALUE
0x00	Input Port 0	R only	0xFF
0x01	Input Port 1	R only	0xFF
0x02	Output Port 0	R/W	0xFF
0x03	Output Port 1	R/W	0xFF
0x04	Polarity Inversion Port 0	R/W	0x00
0x05	Polarity Inversion Port 1	R/W	0x00
0x06	Configuration Port 0	R/W	0xFF
0x07	Configuration Port 1	R/W	0xFF

The *Input Port X* registers reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the *Configuration Port X* register. It only acts on read operation. Writes to these registers have no effect. The power-on default value of this register is all 1.

The *Output Port X* registers reflect the outgoing logic levels of the pins defined as outputs by the *Configuration Port X* register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

The *Polarity Inversion Port X* registers allow the user to invert the polarity of the *Input Port X* register data. If a bit in this register is set to 1, the *Input Port X* register data polarity is inverted. If a bit in this register is cleared to 0, the *Input Port X* register data polarity is retained.

The *Configuration Port X* registers configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

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7.3 Serial Interface

7.3.1 Bus Overview

I2C/SMBus is a two-wire serial communication interface supporting multi-master and multi-slave. The device that initiates the communication is called the *master*, and the device controlled by the master is called the *slave*. The master is responsible for generating the serial clock (SCL) and controlling the bus access.

Data transfer is sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA while SCL is high is interpreted as a START or STOP conditions. Parameters for Figure 2 are defined in Table 2.

Table 2. Timing Diagram Requirements

SYMBOL	PARAMETER	FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	1	400	1	2000	kHz
$t_{SU:STA}$	Repeated START condition setup time	0.6	-	0.26	-	us
$t_{HD:STA}$	Repeated START condition hold time	0.6	-	0.26	-	us
$t_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	us
t_{BUF}	Bus free time between STOP and START	1.3	-	0.5	-	us
$t_{SU:DAT}$	Data setup time	0.1	-	0.05	-	us
$t_{HD:DAT}$	Data hold time	0	-	0	-	us
t_{HIG}	SCL clock high period	0.6	-	0.26	-	us
t_{LOW}	SCL clock low period	1.3	-	0.5	-	us
t_R	Clock and data rise time	-	300	-	120	ns
t_F	Clock and data fall time	-	300	-	120	ns

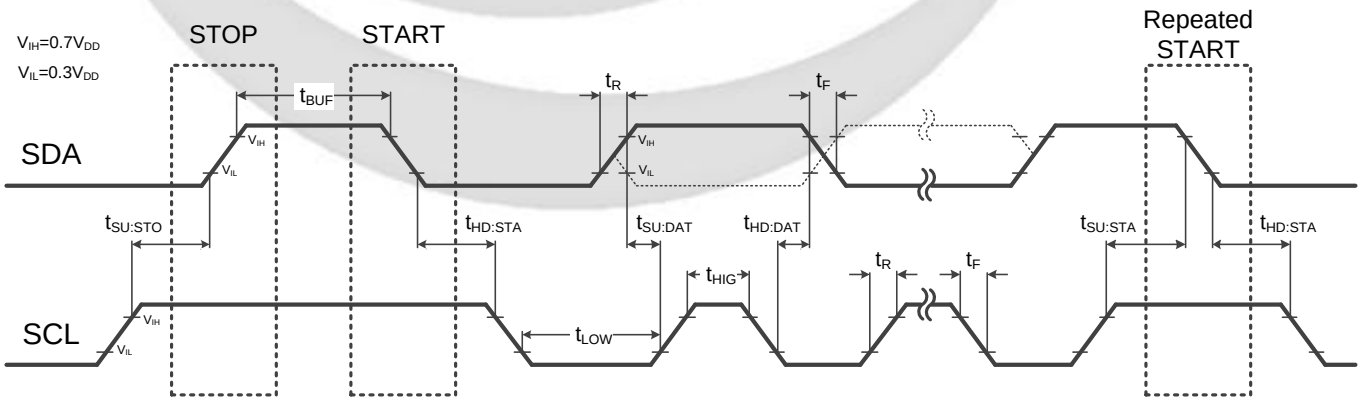


Figure 2. Two-Wire Timing Diagram

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7.3.2 Serial Bus Address

The GLF77535 features three address pins that allow up to eight devices to be addressed on a single bus. Table 2 describes the pin logic levels and the corresponding address values. It is crucial for the logic level of the address pin to remain consistent throughout communication in order to avoid potential failures. The address pin must be connected either to VCC or GND and should not be left in a suspended state.

The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing either a read or write operation. All data bytes are transmitted MSB first.

Table 3. Address Pin Connection and Slave Address

A2	A1	A0	DEVICE TWO-WIRE ADDRESS
GND	GND	GND	0x40 (write), 0x41 (read)
GND	GND	VCC	0x42 (write), 0x43 (read)
GND	VCC	GND	0x44 (write), 0x45 (read)
GND	VCC	VCC	0x46 (write), 0x47 (read)
VCC	GND	GND	0x48 (write), 0x49 (read)
VCC	GND	VCC	0x4A (write), 0x4B (read)
VCC	VCC	GND	0x4C (write), 0x4D (read)
VCC	VCC	VCC	0x4E (write), 0x4F (read)

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7.3.3 Writing and Reading Operation

If the R/W bit is 0b, the first byte sent by the host after the slave address byte is recognized as a pointer. The GLF77535 uses the pointer to specify the target register of the current read or write operation. The data byte follows the pointer byte and represents the data to be written to the specified register. The specific bus timing is shown in Figure 3 and consists of start condition, address byte, pointer byte, data byte and stop condition. The GLF77535 pulls down the SDA bus at the ninth clock pulse to indicate that the byte has been received and is ready to receive a new byte.

The GLF77535 features a pointer automatic shift function. After each register access is completed, the pointer points to the other register of the same type. For example, after the current byte is written to the *Output Port 0* register, the next byte is written to the *Output Port 1* register, the next byte is written back to the *Output Port 0* register, and so on. The specific bus timing is shown in Figure 4.

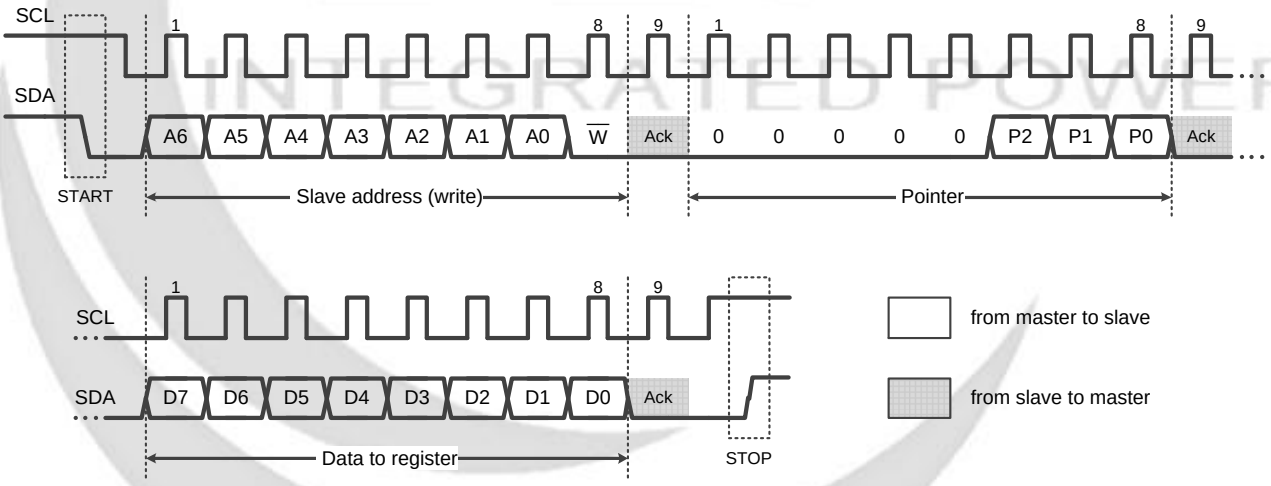


Figure 3. Two-Wire Timing Diagram for Write One Byte

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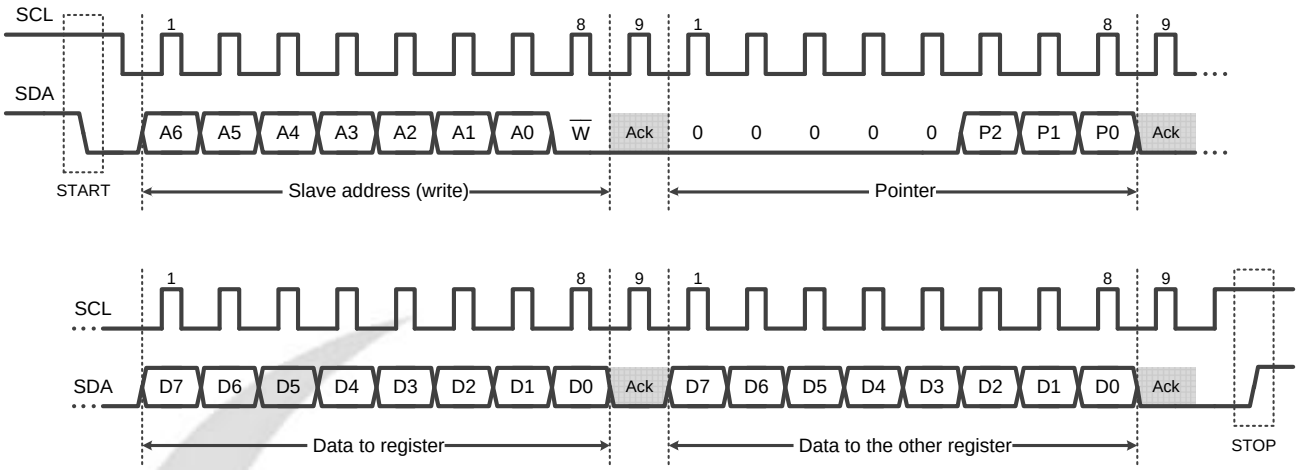


Figure 4. Two-Wire Timing Diagram for Write Two Bytes

If the R/W bit is 1b, then the host can start reading data bytes after the slave address byte. The content of the data is determined by the pointer. Therefore, in the read operation, the host needs to modify the pointer first, and then restart a round of communication to read the target data. The specific bus timing is shown in Figure 5.

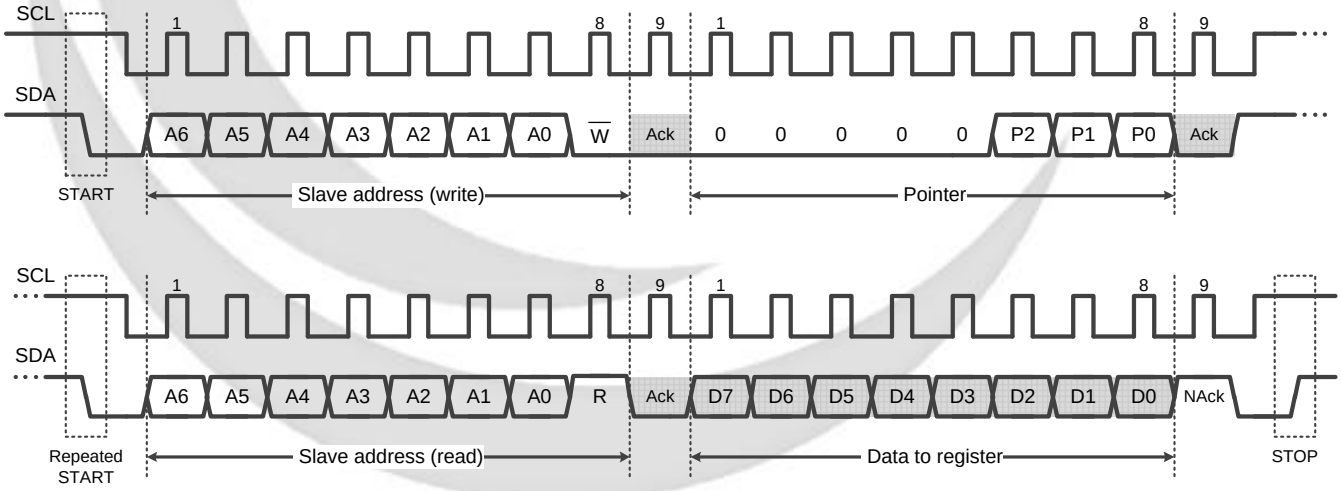


Figure 5. Two-Wire Timing Diagram for Read One Byte

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Read operations support multi-byte access. The specific bus timing is shown in Figure 6.

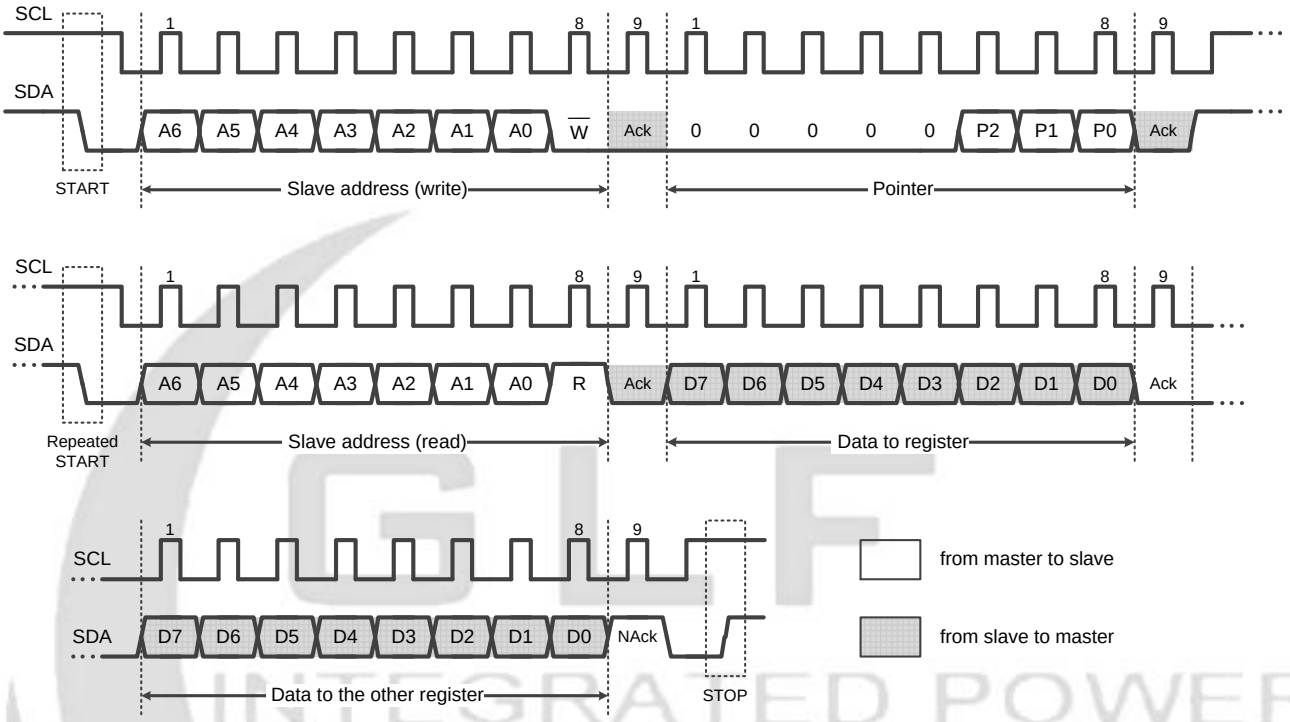


Figure 6. Two-Wire Timing Diagram for Read Two Bytes

7.3.4 Port Control

The GLF77535 controls the output of an I/O pin assuming that the pin has been configured in output mode. The impact of the *Output Port X* register on the control of the I/O ports is illustrated in Figure 7. The GLF77535 flushes the received data to the I/O pins at the rising edge of SCL for each Ack of data bytes.

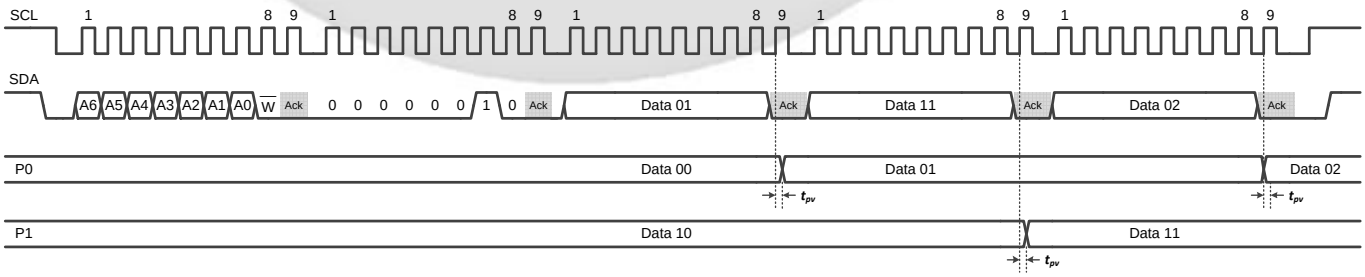


Figure 7. Write to Output Port X Registers

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The GLF77535 is capable of acquiring the logic level of the I/O pin in both input and output configurations. The impact of reading the input register on the interrupt signal can be observed in Figures 8 and 9. During each Ack of data bytes, The GLF77535 samples the logic level of the I/O pin into the input register at the rising edge of SCL, subsequently clearing the interrupt.

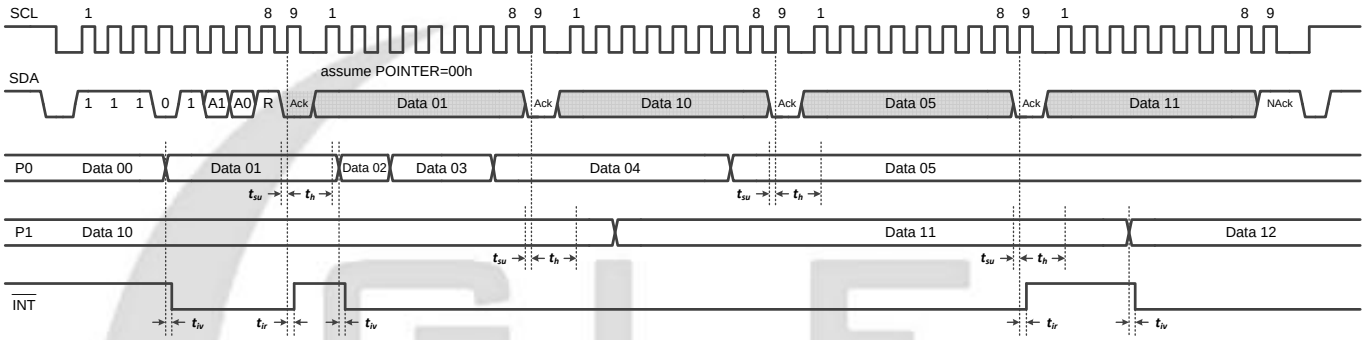


Figure 8. Read Input Port Registers, Scenario 1

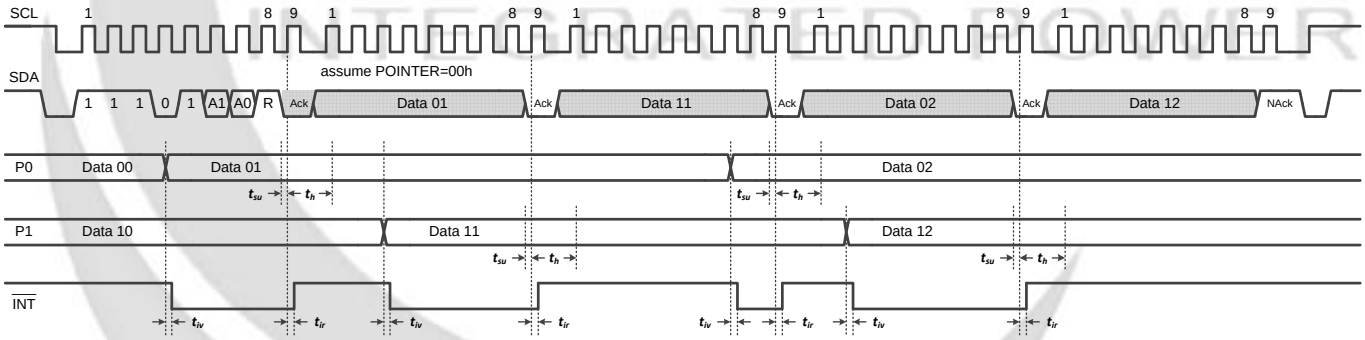


Figure 9. Read Input Port Registers, Scenario 2

Table 4. Switching Characteristics

SYMBOL	PARAMETER	FROM	TO	MIN	TYP	MAX	UNIT
t_{pv}	Outpu Data Valid Time	SCL	GPIO			1	us
t_{su}	Input Data Setupt	GPIO	SCL		1		us
t_h	Input Data Hold Time	GPIO	SCL		1		us
t_{iv}	Interrupt Valid Time	GPIO	INT			4	us
t_{ir}	Interrupt Reset Delay	SCL	INT			4	us

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7.3.5 High-Speed (Hs) Mode

For the I^2C bus to operate at frequencies above 1 MHz, the master device must issue an Hs-mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. The GLF77535 does not acknowledge this byte, but switches the input filters on the SDA and SCL pins and the output filters on the SDA pin to operate in Hs-mode, thus allowing transfers at up to 2 MHz. After the Hs-mode master code has been issued, the master transmits an I^2C slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, The GLF77535 switches the input and output filters back to fast-mode operation.

7.4 Interrupt Output

The GLF77535 features an open-drain output interrupt pin that can be directly connected to the microprocessor's interrupt input. By transmitting an interrupt signal, the chip can actively notify the microprocessor of any changes in logic level on the remote I/O pin.

There are two crucial aspects to consider regarding the establishment and removal of interrupt signals :

- The interrupt signal will only be triggered by a change in the logic level of the I/O pin configured as input.
- The interrupt signal is not latched. If the I/O pin logic level is restored to its previous sampled state, the interrupt signal will be immediately cleared.

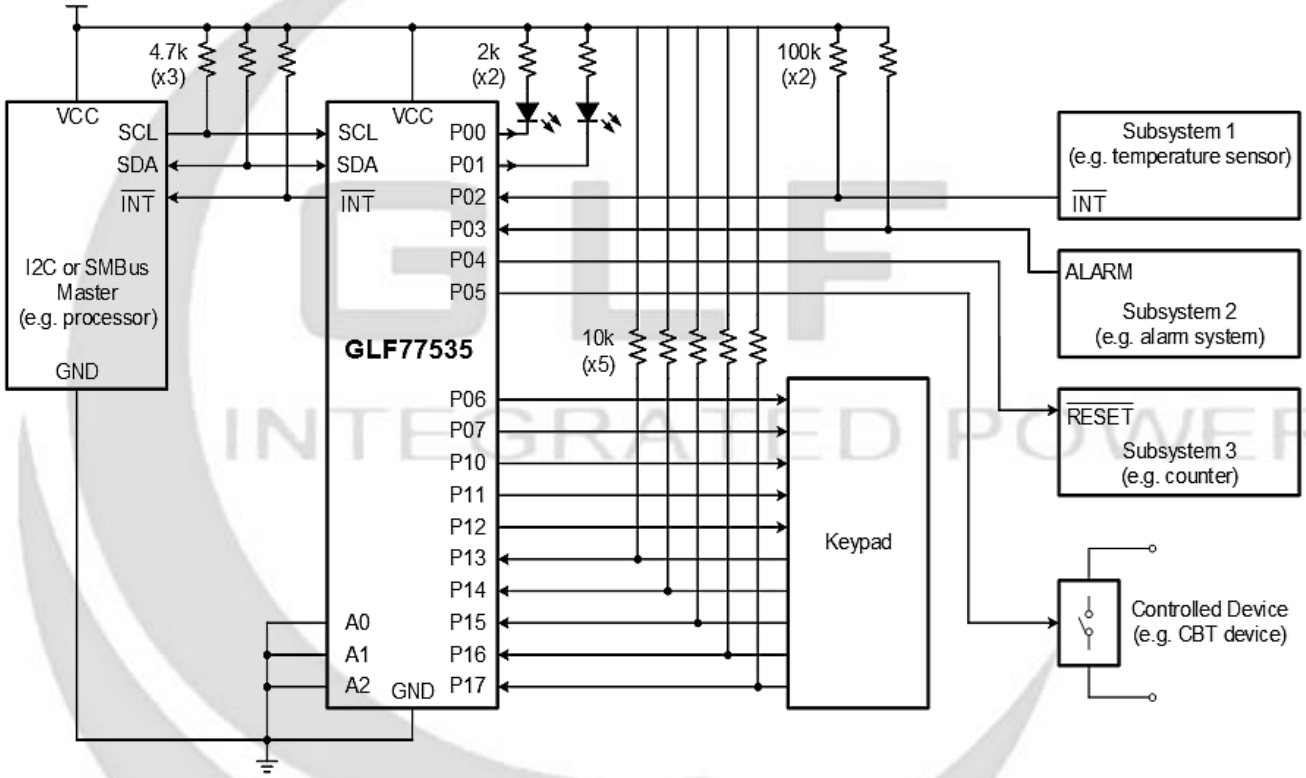
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8 Application and Implementation

NOTE

The following contents are notes and suggestions for the use of GLF77535 family, and GLF does not warrant its accuracy or completeness. Customers are responsible for determing suitability of components for their purpose, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application



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8.2 Quick Feature Guide

Table 5. Selection Table

DEVICE	TYPE	I/O	ADDRESS	BUILT-IN	RESET INPUT
GLF77574	Quasi bi-dir.	8	0100 xxxb		
GLF77534	Totem-pole	8	0100 xxxb		
GLF77538	Totem-pole	8	1110 0xxb		√
GLF77554	Totem-pole	8	0100 xxxb	√	
GLF77535	Totem-pole	16	0100 xxxb		
GLF77539	Totem-pole	16	1110 1xxb		√
GLF77555	Totem-pole	16	0100 xxxb	√	

8.3 High Current-Drive Load Application

The I/O pins of the GLF77535 are capable of driving with a minimum perfusion current of 10mA. Additionally, it is possible to connect multiple I/O pins together through short-wiring in order to enhance the current-driven capability. As illustrated in Figure 10, individual current limiting resistors are necessary for each I/O pin and proper synchronization of switches is required to prevent any potential damage to the chip.

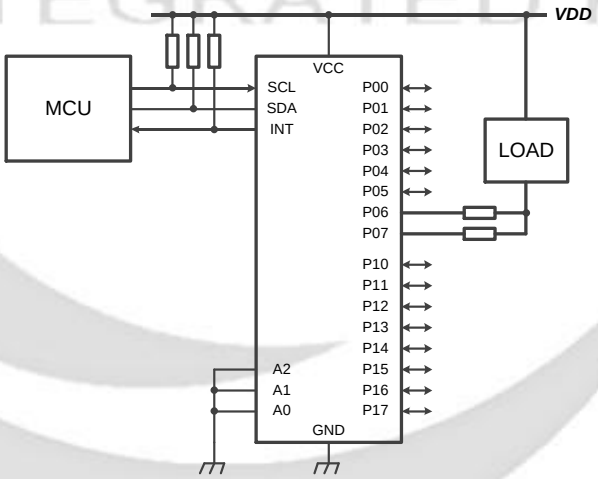
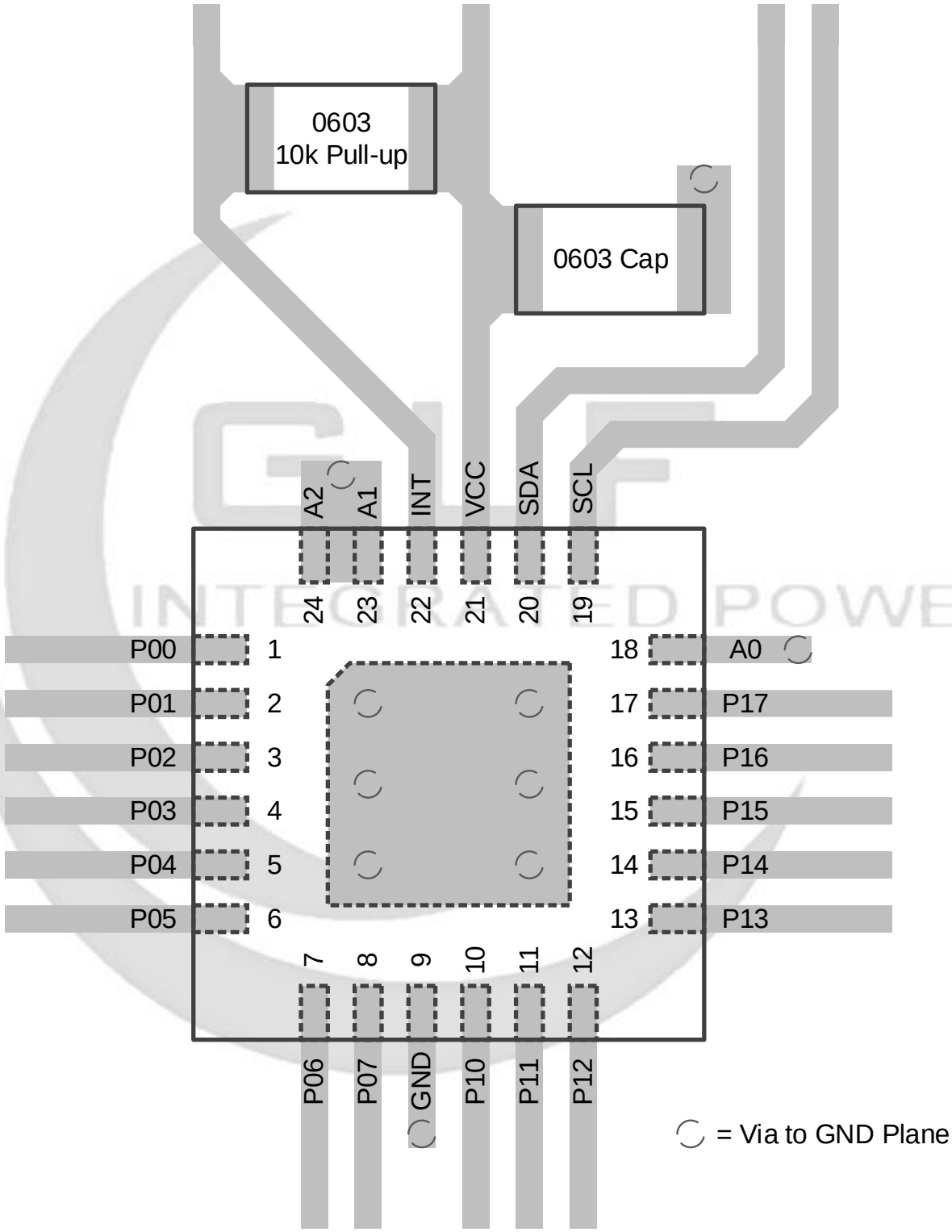


Figure 10. High Current-Drive Load Application

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8.4 Layout Example

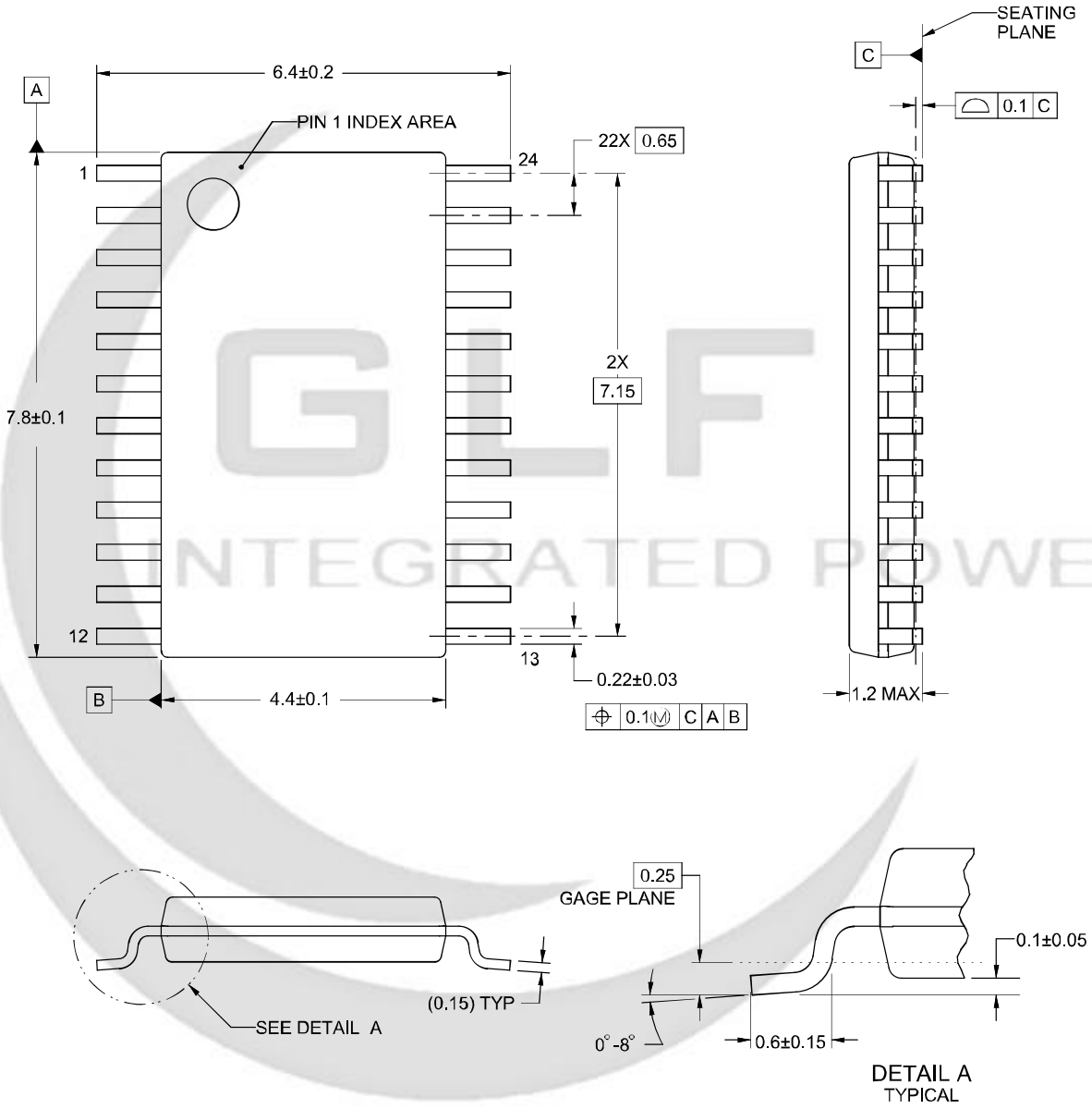


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9 Packaging Information

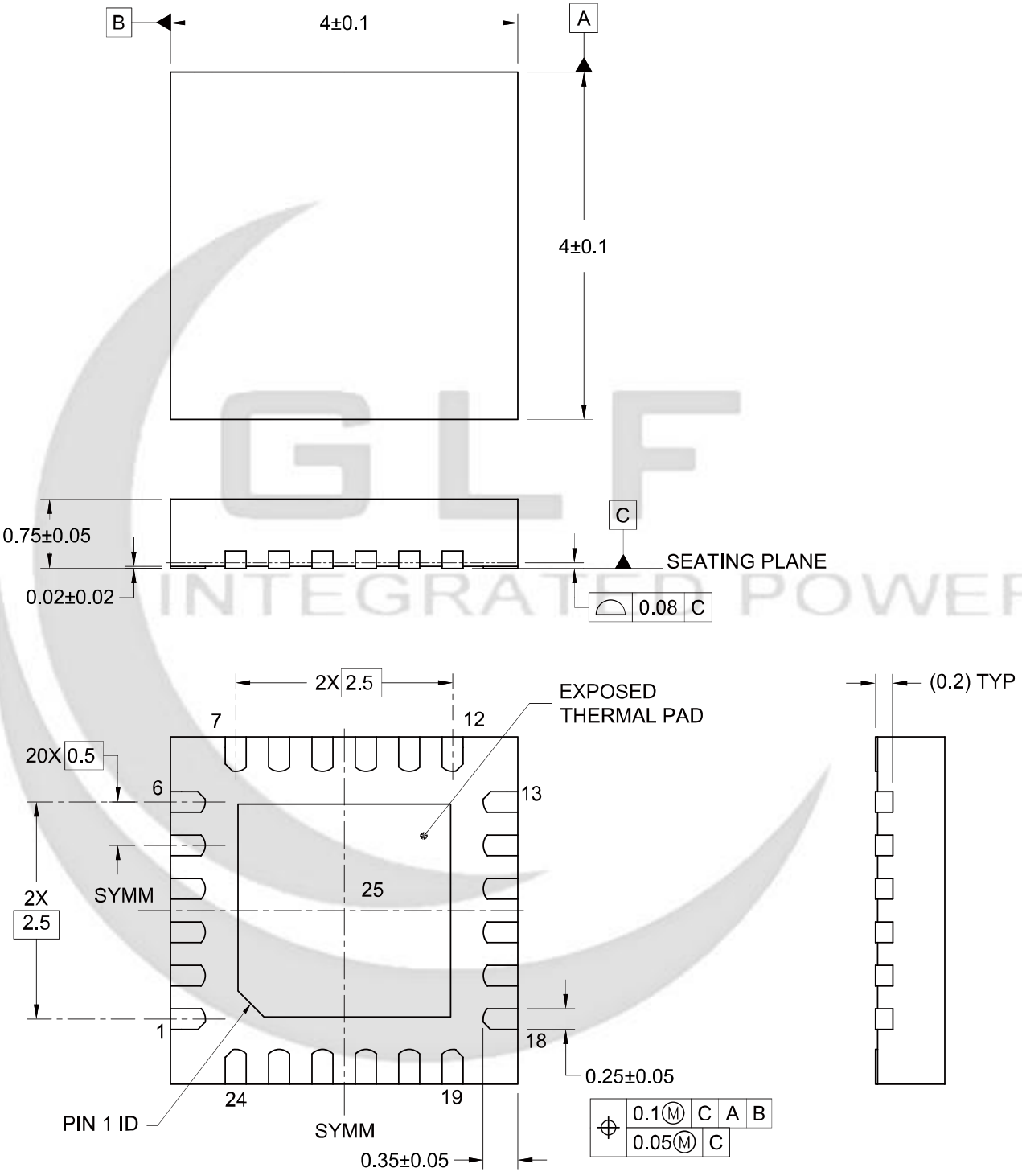
All dimensions mentioned below are in millimeters.

9.1 Package Outline (TSSOP-24L)



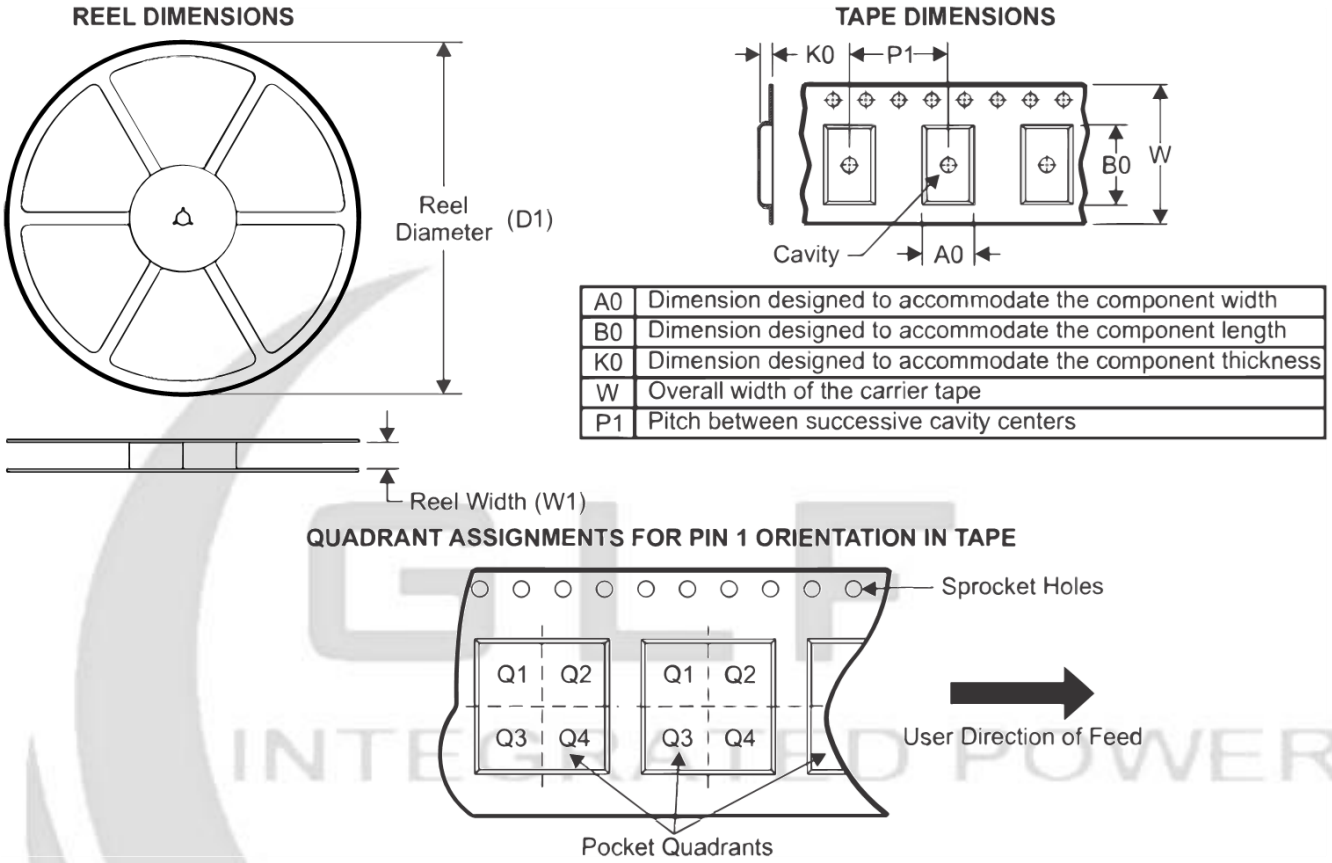
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9.2 Package Outline (QFN4x4-24L)



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9.3 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

PACKAGE	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1
TSSOP-24L	330	16.4	6.80	8.30	1.60	8.00	16.00	Q1
QFN4x4-24L	329	12.4	4.30	4.30	1.10	8.00	12.00	Q1

Note: All dimensions mentioned above are in millimeters.

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